

# MOSFET – P-Channel, Logic Level, POWERTRENCH®

## FDS4435A

### General Description

This P-Channel Logic Level MOSFET is produced using ON Semiconductor's advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge superior switching performance.

These devices are well suited for notebook computer applications: load switching and power management, battery charging circuits, and DC/DC conversion.

### Features

- -9 A, -30 V.  $R_{DS(ON)} = 0.017 \Omega @ V_{GS} = -10 \text{ V}$   
 $R_{DS(ON)} = 0.025 \Omega @ V_{GS} = -4.5 \text{ V}$
- Low Gate Charge (21 nC Typical).
- High Performance Trench Technology for Extremely Low  $R_{DS(ON)}$
- High Power and Current Handling Capability
- This Device is Pb-Free and RoHS Compliant

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DS}$	Drain-Source Voltage	-30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current – Continuous (Note 1a) – Pulsed	-9 -50	A
$P_D$	Power Dissipation (Note 1a) for Single Operation (Note 1b) (Note 1c)	2.5 1.2 1	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

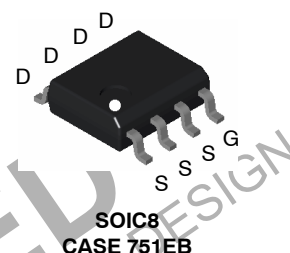
### THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	25	$^\circ\text{C/W}$



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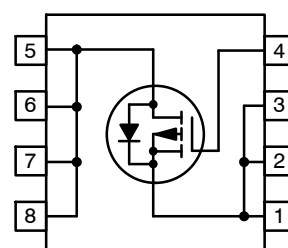


### MARKING DIAGRAM



FDS4435A = Specific Device Code  
A = Assembly Site  
L = Wafer Lot Number  
YW = Assembly Start Week

### ELECTRICAL CONNECTION



### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-30	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	-26	-	mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$ $T_J = 125^\circ\text{C}$	-	-	-1	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	-	-	-100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	100	nA

**ON CHARACTERISTICS**

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1	-1.7	-2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	4.2	-	mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -9\text{ A}$ $T_J = 125^\circ\text{C}$	-	0.015	0.017	$\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -7\text{ A}$	-	0.023	0.025	
$g_{FS}$	Forward Transconductance	$V_{DS} = -10\text{ V}, I_D = -9\text{ A}$	-	25	-	S

**DYNAMIC CHARACTERISTICS**

$C_{iss}$	Input Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}$ $f = 1.0\text{ MHz}$	-	2010	-	pF
$C_{oss}$	Output Capacitance		-	590	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	260	-	pF

**SWITCHING CHARACTERISTICS**

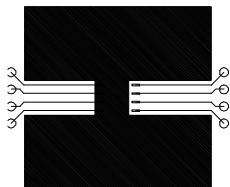
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15\text{ V}, I_D = -1\text{ A}$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\text{ }\Omega$	-	12	22	ns
$t_r$	Turn-On Rise Time		-	15	27	ns
$t_{d(off)}$	Turn-Off Delay Time		-	100	140	ns
$t_f$	Turn-Off Fall Time		-	55	80	ns
$Q_g$	Total Gate Charge	$V_{DS} = -15\text{ V}, I_D = -9\text{ A}$ $V_{GS} = -5\text{ V}$	-	21	30	nC
$Q_{gs}$	Gate-Source Charge		-	6	-	nC
$Q_{gd}$	Gate-Drain Charge		-	8	-	nC

**DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS**

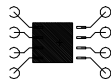
$I_S$	Maximum Continuous Drain-Source Diode Forward Current		-	-	-2.1	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -2.1\text{ A}$ (Note 2)	-	-0.75	-1.2	V
$t_{rr}$	Source-Drain Reverse Recovery Time	$I_F = -10\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{S}$	-	36	80	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

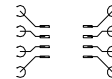
1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $50^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz. Copper.



b)  $105^\circ\text{C/W}$  when mounted on a  $0.04\text{ in}^2$  pad of 2 oz. copper.



c)  $125^\circ\text{C/W}$  when mounted on a minimum pad.

2. Pulse Test Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$

## TYPICAL CHARACTERISTICS

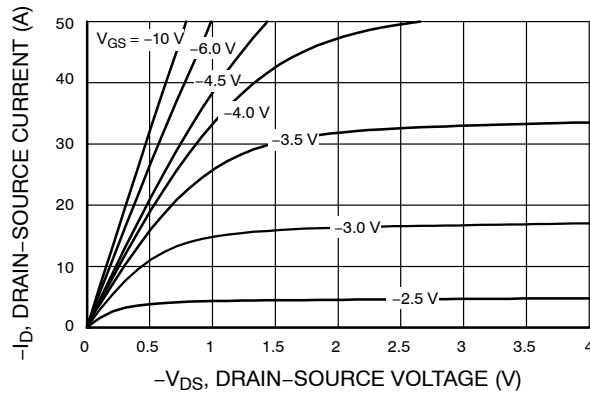


Figure 1. On-Region Characteristics

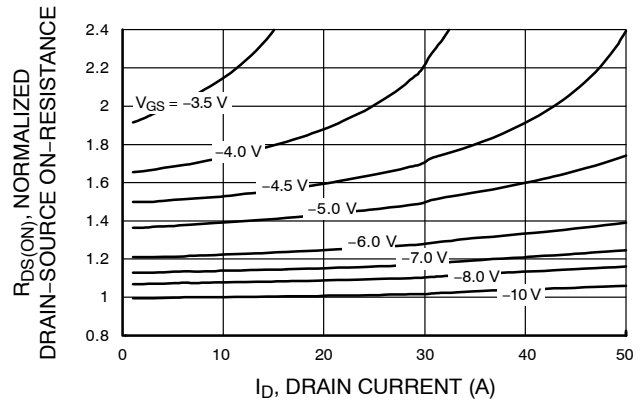


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

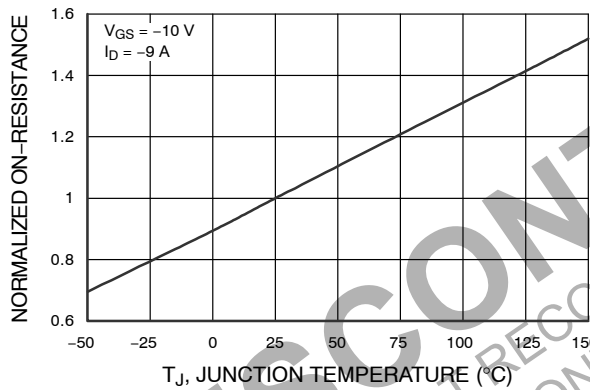


Figure 3. On-Resistance Variation with Temperature

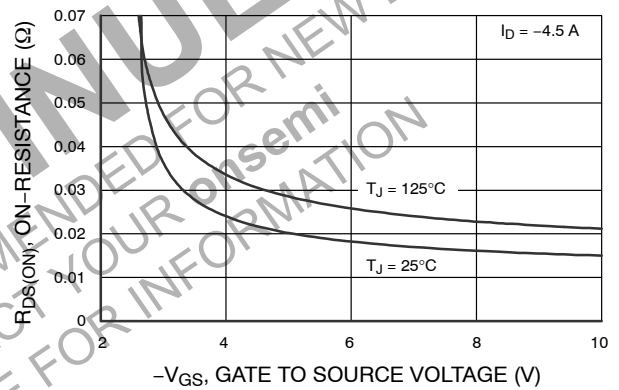


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

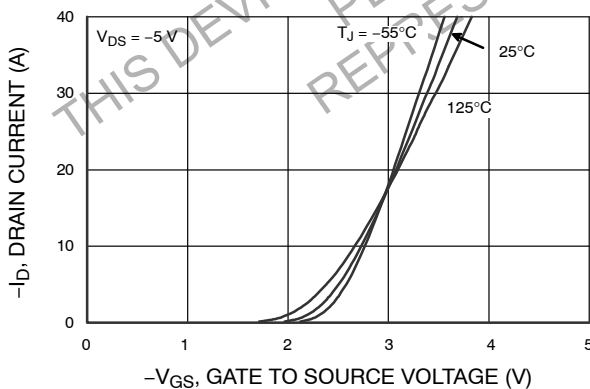


Figure 5. Transfer Characteristics

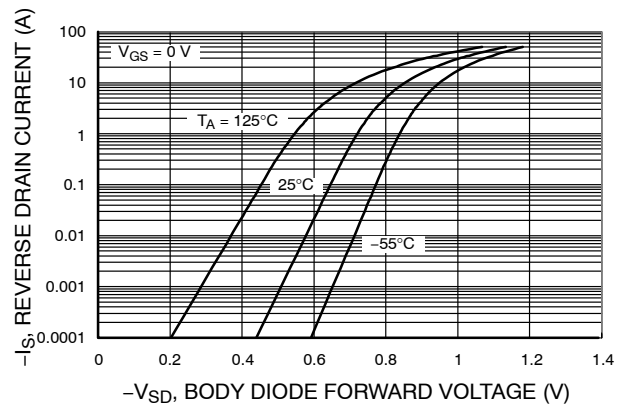


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

## TYPICAL CHARACTERISTICS (continued)

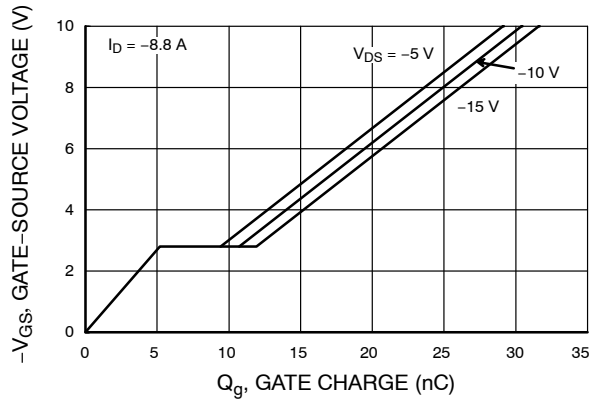


Figure 7. Gate-Charge Characteristics

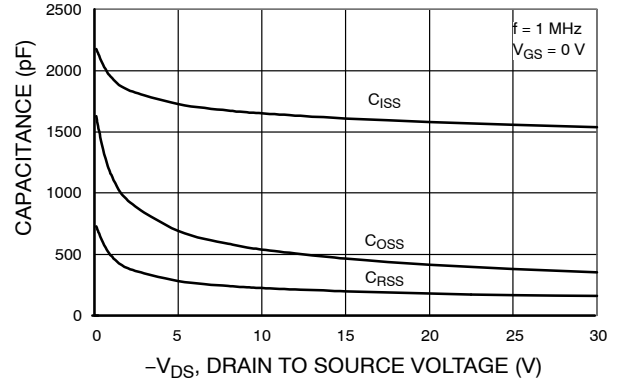


Figure 8. Capacitance Characteristics

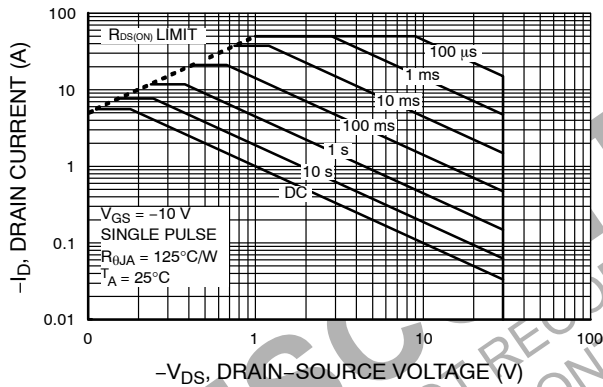


Figure 9. Maximum Safe Operating Area

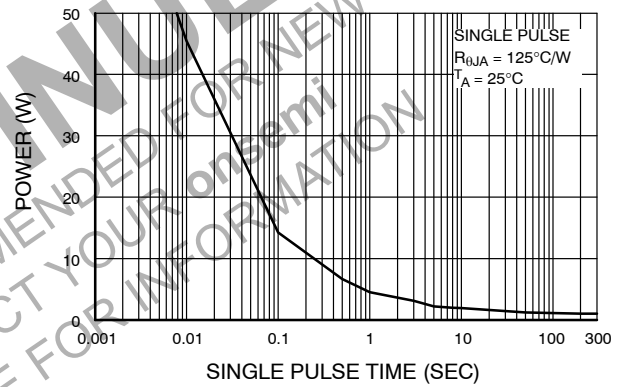


Figure 10. Single Pulse Maximum Power Dissipation

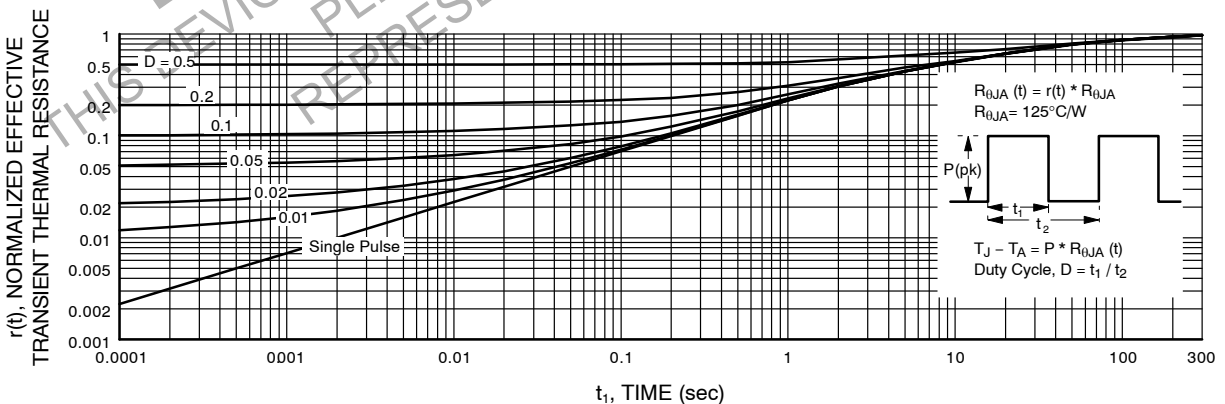


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1c.

Transient thermal response will change depending on the circuit board design.

## FDS4435A

### ORDERING INFORMATION

Device Marking	Device	Package Type	Reel Size	Tape Width	Shipping <sup>†</sup>
FDS4435A	FDS4435A	SOIC8 (Pb-Free)	13"	12 mm	2500 / Tape & Reel

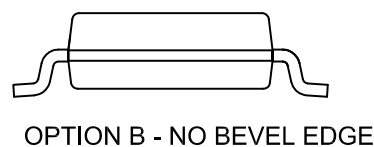
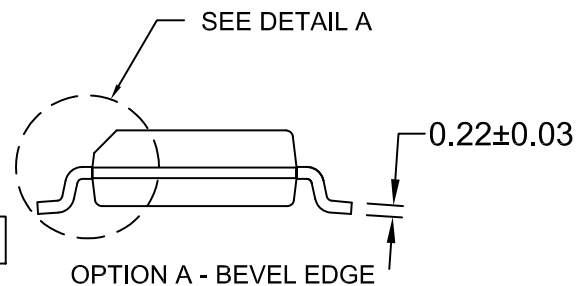
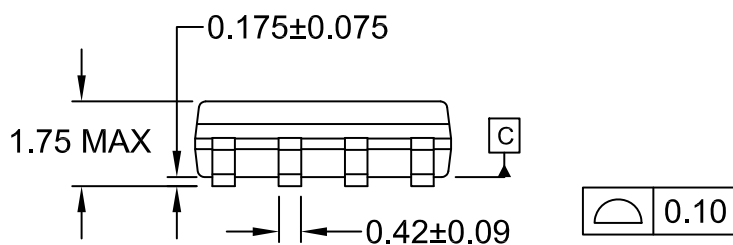
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**DISCONTINUED**  
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**SOIC8**  
**CASE 751EB**  
**ISSUE A**

DATE 24 AUG 2017



**NOTES:**

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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