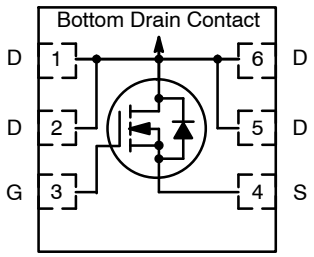
MOSFET – Single, N-Channel, POWERTRENCH®

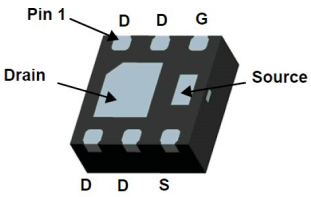
80 V, 6 A, 36.5 mΩ

FDMA037N08LC

V_{DS}	$R_{DS(on)}$ MAX	$I_{D\ MAX}$
80 V	36.5 mΩ @ 10 V	6 A

Single N−Channel





MicroFET 2X2 (Bottom View)

WDFN6 2x2, 0.65P
CASE 511DB

Description

This device has been designed to provide maximum efficiency and thermal performance for synchronous buck converters. The low $R_{DS(on)}$ and gate charge provide excellent switching performance.

Features

- PTNG MOSFET Technology
- Max $R_{DS(on)}$ = 36.5 mΩ at V_{GS} = 10 V, I_D = 4 A
- Max $R_{DS(on)}$ = 56.9 mΩ at V_{GS} = 4.5 V, I_D = 3 A
- 5 V Drive Capable
- 50% Lower Q_{rr} than Other MOSFET Suppliers
- Lower Switching Noise/EMI
- Low Profile − 0.8 mm Maximum in the New Package MicroFET™ 2x2 mm
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- DC−DC Buck Converters

MARKING DIAGRAM

&Z	= Assembly Plant Code
&2	= Numeric Date Code
&K	= Lot Code
037L	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

MOSFET MAXIMUM RATINGS (T_A = 25°C, Unless otherwise specified)

Symbol	Parameter		Ratings	Unit
V_{DS}	Drain to Source Voltage		80	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Continuous	T_A = 25°C (Note 1a)	6	A
	Pulsed		55	
P_D	Power Dissipation	T_A = 25°C (Note 1a)	2.4	W
	Power Dissipation	T_A = 25°C (Note 1b)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Shipping (Qty / Packing)†
037L	FDMA037N08LC	WDFN6 2x2, 0.65P (MicroFET) (Pb−Free/Halogen Free)	7″	8 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	80	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	69	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 64 V, V_{GS} = 0 V	–	–	−1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±1	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 20 μA	1.0	1.3	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 20 μA, referenced to 25°C	–	−5	–	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 4 A	–	30.9	36.5	mΩ
		V_{GS} = 4.5 V, I_D = 3 A	–	42.1	56.9	
		V_{GS} = 10 V, I_D = 4 A, T_J = 125°C	–	51.4	61	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 4 A	–	15	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz	–	425	595	pF
C_{oss}	Output Capacitance		–	110	155	pF
C_{rss}	Reverse Transfer Capacitance		–	6.0	8.3	pF

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

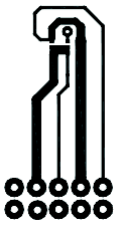
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−on Delay Time	V_{DD} = 40 V, I_D = 4 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	4.9	10	ns
t_r	Rise Time		–	1.3	10	
$t_{d(off)}$	Turn−off Delay Time		–	14	24	
t_f	Fall Time		–	1.7	10	
Q_g	Total Gate Charge	V_{GS} = 0V to 10 V, V_{DD} = 40 V, I_D = 4 A	–	6.5	9.0	nC
Q_g	Total Gate Charge	V_{GS} = 0V to 4.5 V, V_{DD} = 40 V, I_D = 4 A	–	3.2	4.5	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 40 V, I_D = 4 A	–	0.9	–	nC
Q_{gd}	Gate to Drain ”Miller” Charge	V_{DD} = 40 V, I_D = 4 A	–	0.9	–	nC
Q_{oss}	Output Charge	V_{DD} = 40 V, V_{GS} = 0 V	–	6.4	–	nC
Q_{sync}	Total Gate Charge Sync	V_{DS} = 0 V, I_D = 4 A	–	5.9	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A (Note 2)	–	0.8	1.2	V
		V_{GS} = 0 V, I_S = 4 A (Note 2)	–	0.8	1.3	V
t_{rr}	Reverse Recovery Time	I_F = 2 A, di/dt = 300 A/μs	–	10	20	ns
Q_{rr}	Reverse Recovery Charge		–	9	14	nC
t_{rr}	Reverse Recovery Time	I_F = 2 A, di/dt = 1000 A/μs	–	8	16	ns
Q_{rr}	Reverse Recovery Charge		–	26	51	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user’s board design.

a) 52°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 145°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS (T_J = 25°C UNLESS OTHERWISE NOTED)

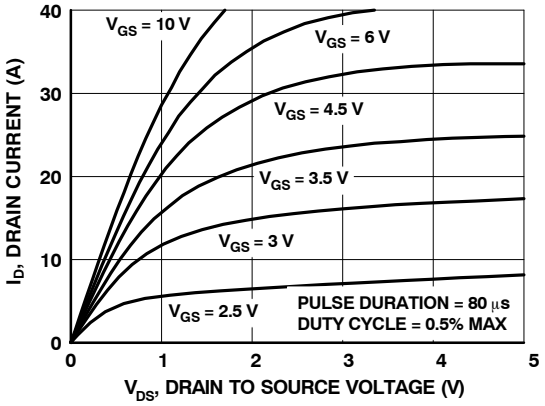


Figure 1. On Region Characteristics

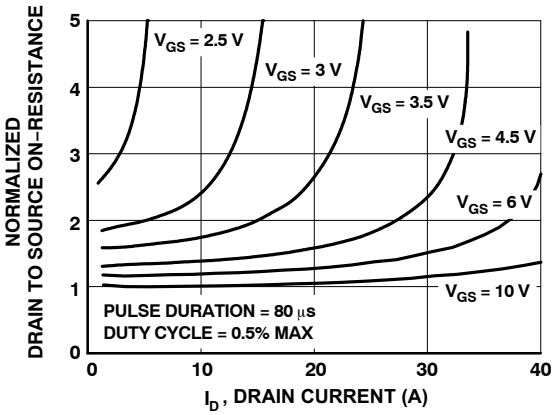


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

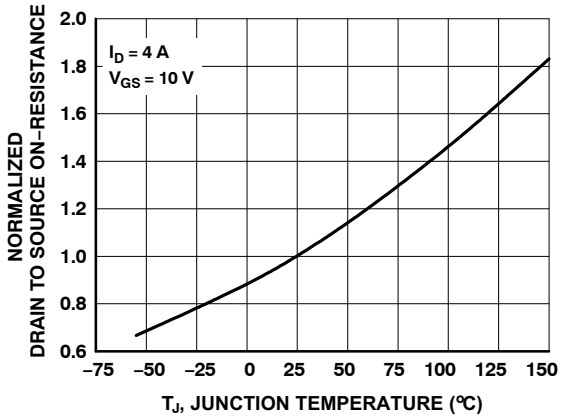


Figure 3. Normalized On Resistance vs. Junction Temperature

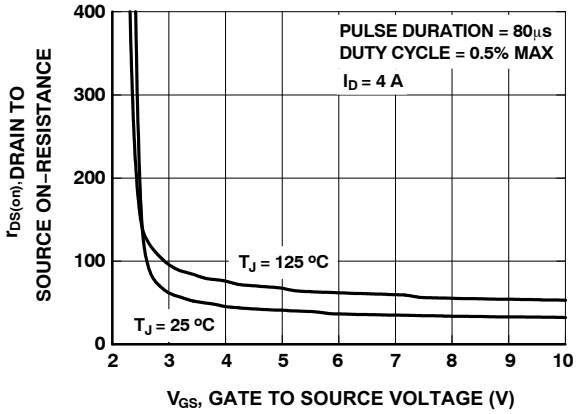


Figure 4. On-Resistance vs. Gate to Source Voltage

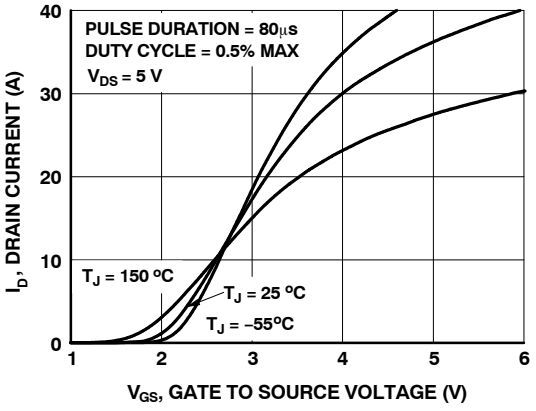


Figure 5. Transfer Characteristics

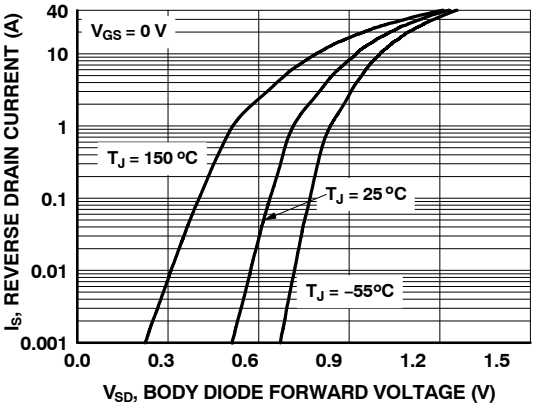


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (CONTINUED)

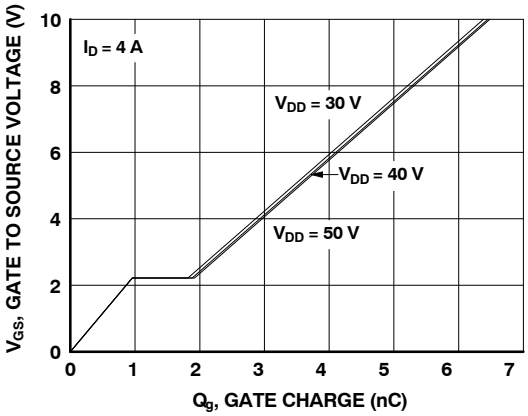


Figure 7. Gate Charge Characteristics

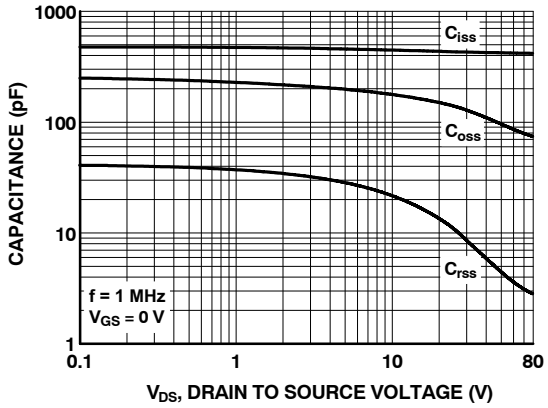


Figure 8. Capacitance vs. Drain to Source Voltage

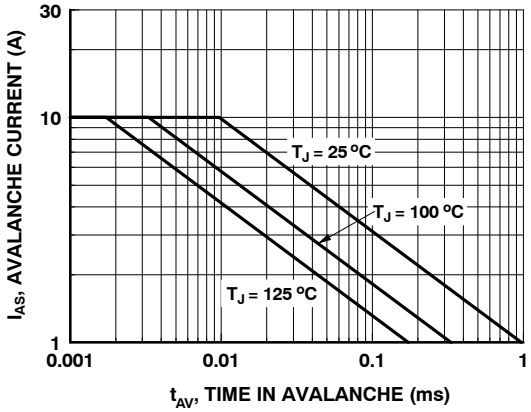


Figure 9. Unclamped Inductive Switching Capability

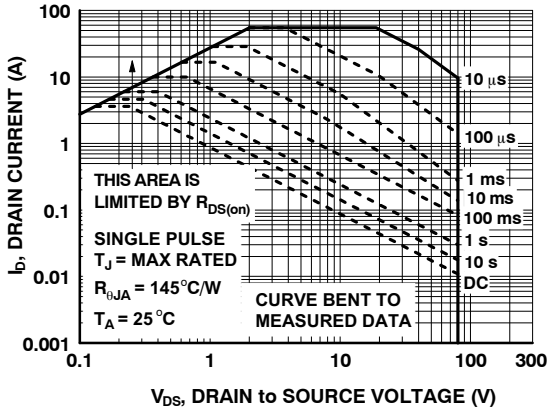


Figure 10. Forward Bias Safe Operating Area

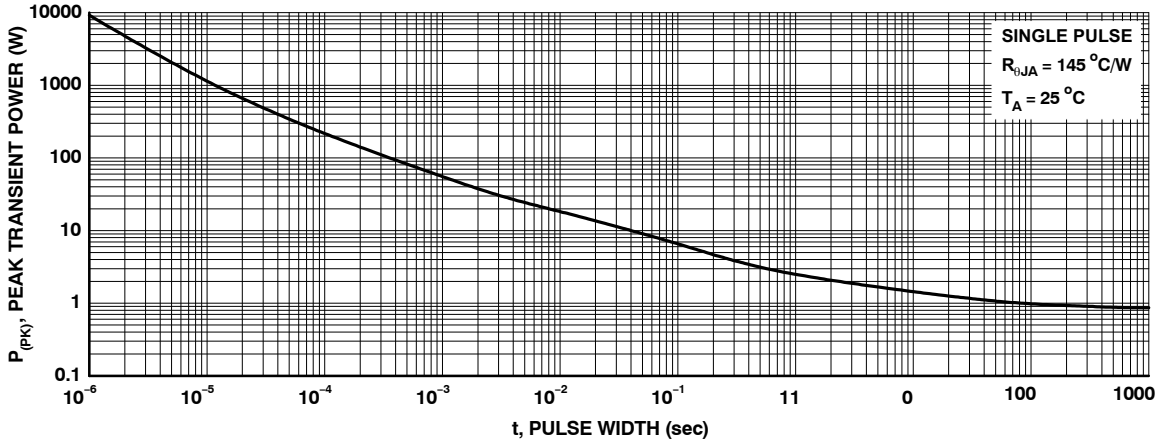


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (CONTINUED)

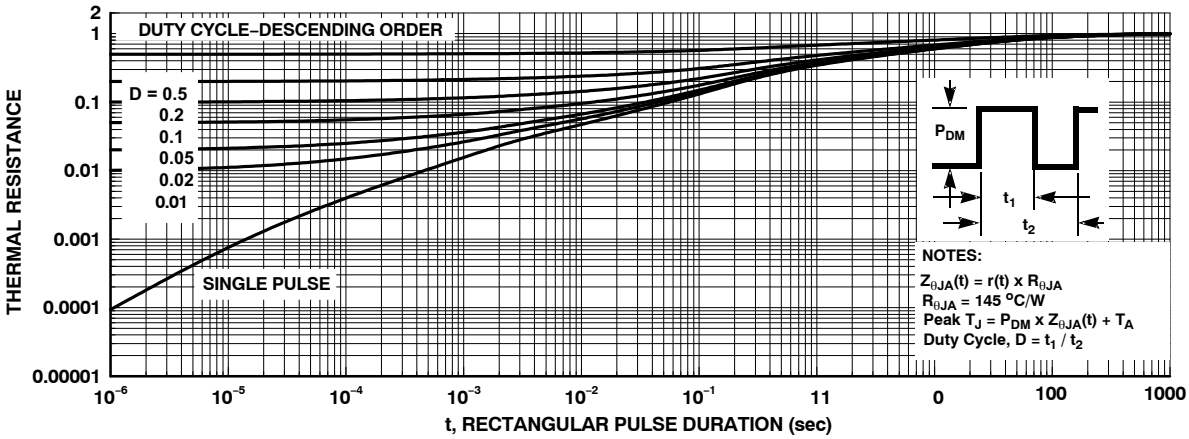
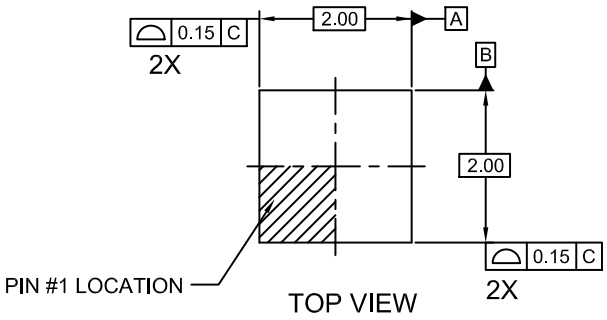


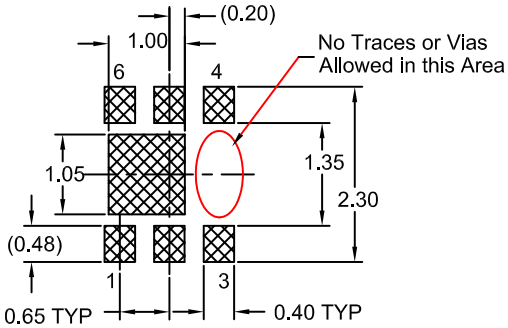
Figure 12. Junction−to−Case Transient Thermal Response Curve

WDFN6 2x2, 0.65P
CASE 511DB
ISSUE O

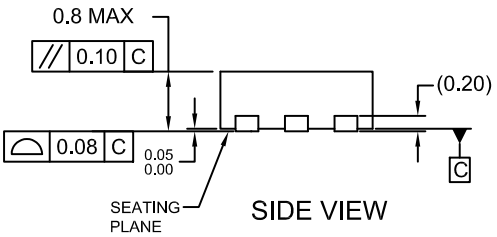
DATE 31 AUG 2016



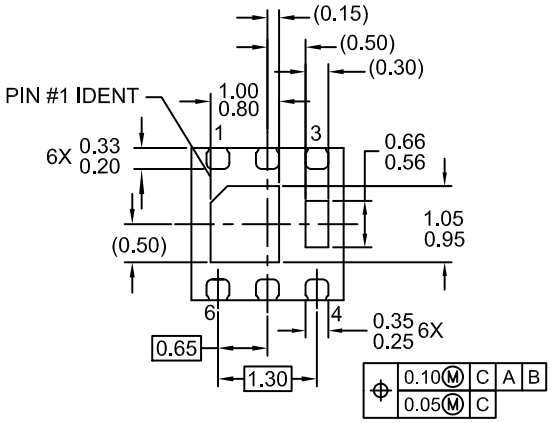
TOP VIEW



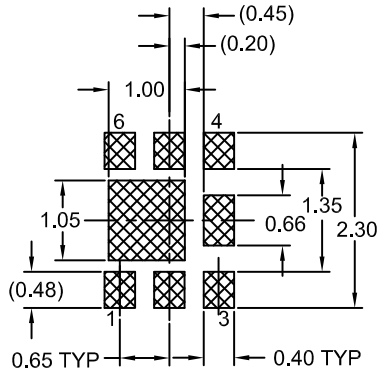
RECOMMENDED LAND PATTERN OPT 1



SIDE VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN OPT 2

NOTES:

A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION
MO-229 DATED AUG/2003
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER
ASME Y14.5M, 1994

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