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FAIRCHILD SEMICONDUCTOR®

May 2024

FAN7621S
PFM Controller for Half-Bridge Resonant Converters

Features

- Variable Frequency Control with 50% Duty Cycle for Half-bridge Resonant Converter Topology
- High Efficiency through Zero Voltage Switching (ZVS)
- Fixed Dead Time: 350ns
- Up to 300kHz Operating Frequency
- Auto-Restart Operation for All Protections with an External LV_{CC}
- Protection Functions: Over-Voltage Protection (OVP), Over-Current Protection (OCP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown (TSD)

Applications

- PDP and LCD TVs
- Desktop PCs and Servers
- Adapters
- Telecom Power Supplies
- Video Game Consoles

Description

The FAN7621S is a pulse frequency modulation controller for high-efficiency half-bridge resonant converters. Offering everything necessary to build a reliable and robust resonant converter, the FAN7621S simplifies designs and improves productivity while improving performance. The FAN7621S includes a high-side gate-drive circuit, an accurate current-controlled oscillator, frequency-limit circuit, soft-start, and built-in protection functions. The high-side gate-drive circuit has a common-mode noise cancellation capability, which guarantees stable operation with excellent noise immunity. Using the zero-voltage-switching (ZVS) technique dramatically reduces the switching losses and significantly improves efficiency. The ZVS also reduces the switching noise noticeably, which allows a small-sized Electromagnetic Interference (EMI) filter.

The FAN7621S can be applied to various resonant converter topologies; such as series resonant, parallel resonant, and LLC resonant converters.

Related Resources

AN4151 — Half-Bridge LLC Resonant Converter Design Using FSFR-Series Fairchild Power Switch (FPS™)

Ordering Information

Part Number	Operating Junction Temperature	Package	Packaging Method
FAN7621SSJ	-40°C to +130°C	16-Lead, Small Outline Package (SOP)	Tube
FAN7621SSJX			Tape & Reel

Application Circuit Diagram

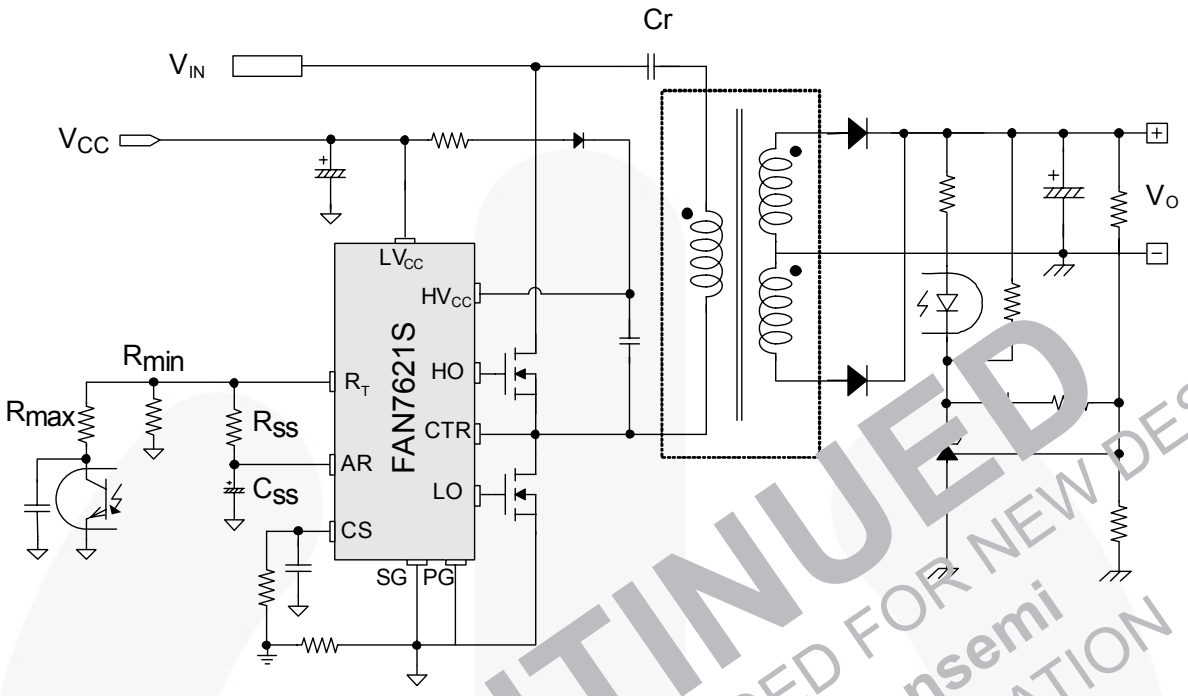


Figure 1. Typical Application Circuit (LLC Resonant Half Bridge Converter)

Block Diagram

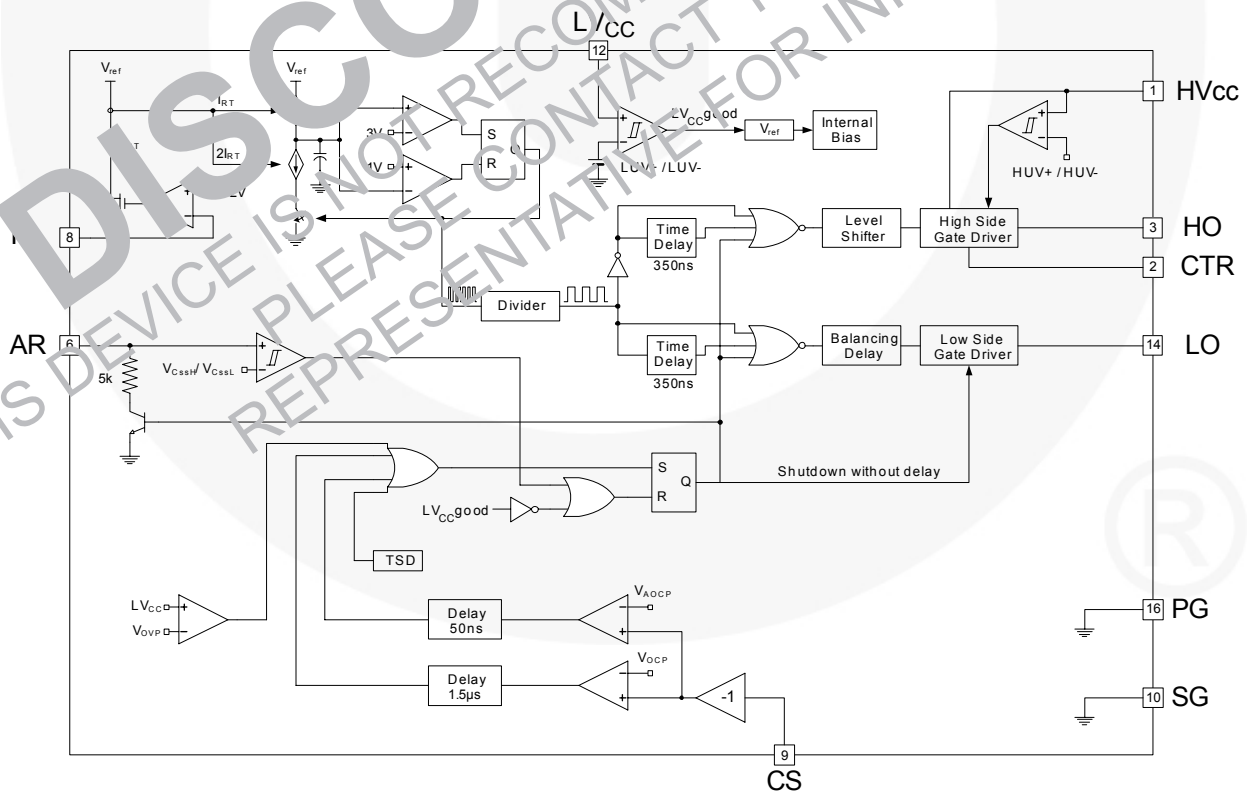


Figure 2. Internal Block Diagram

Pin Configuration

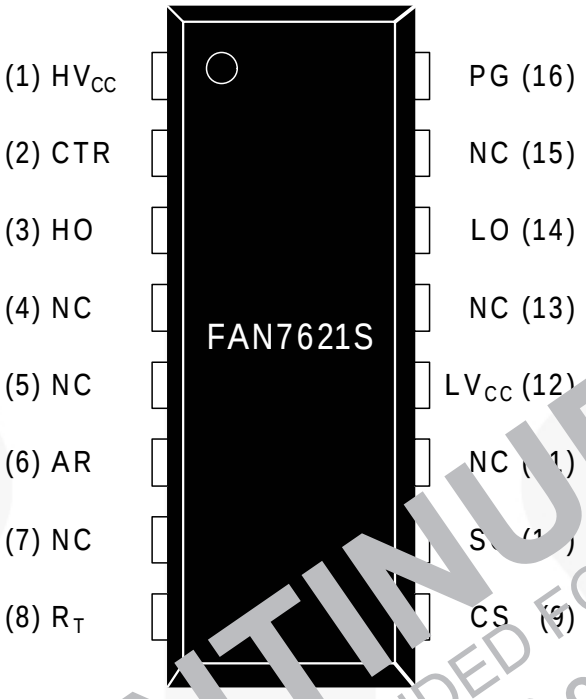


Figure. Package Diagram

Pin Definitions

Pin #	Name	Description
1	HV	This is the supply voltage of the high-side gate-drive circuit IC.
2	CTR	This is the drain of the low-side MOSFET. Typically, a transformer is connected to this pin.
3	HO	This is the high-side gate driving signal.
4	NC	No connection
5	NC	No connection
6	AR	This pin is for discharging the external soft-start capacitor when any protection is triggered. When the voltage of this pin drops to 0.2V, all protections are reset and the controller starts to operate again.
7	NC	No connection
8	R_T	This pin programs the switching frequency. Typically, an opto-coupler is connected to control the switching frequency for the output voltage regulation.
9	CS	This pin senses the current flowing through the low-side MOSFET. Typically, negative voltage is applied on this pin.
10	SG	This pin is the control ground.
11	NC	No connection
12	LV_{CC}	This pin is the supply voltage of the control IC.
13	NC	No connection
14	LO	This is the low-side gate driving signal.
15	NC	No connection
16	PG	This pin is the power ground. This pin is connected to the source of the low-side MOSFET.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A=25°C unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
V_{HO}	High-Side Gate Driving Voltage	V_{CTR}-0.3	HV_{CC}	V
V_{LO}	Low-Side Gate Driving Voltage	-0.3	LV_{CC}	
LV_{CC}	Low-Side Supply Voltage	-0.3	25.0	V
HV_{CC} to V_{CTR}	High-Side V_{CC} Pin to Center Voltage	-0.3	25.0	V
V_{CTR}	Center Voltage	-0.3		V
V_{AR}	Auto-Restart Pin Input Voltage	-0.3	LV_{CC}	V
V_{CS}	Current Sense (CS) Pin Input Voltage		0	V
V_{RT}	R_T Pin Input Voltage	-0.	5.0	V
dV_{CTR}/dt	Allowable Center Voltage Slew Rate		50	V/ns
P_D	Total Power Dissipation		1.13	W
T_J	Maximum Junction Temperature(1)		+150	°C
	Recommended Operating Junction Temperature(1)	-40	+130	
T_{STG}	Storage Temperature Range	-55	+150	°C

Note:
1. The maximum value of the recommended operating junction temperature is limited by the thermal shutdown.

Thermal Impedance

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Impedance	110	ºC/W

Electrical Characteristics

T_A=25°C and LV_{CC}=17V unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply Section						
I_{LK}	Offset Supply Leakage Current	$HV_{CC}=V_{CTR}$			50	μA
I_QHV_{CC}	Quiescent HV_{CC} Supply Current	(HV_{CC}UV+) - 0.1V		50	120	μA
I_QLV_{CC}	Quiescent LV_{CC} Supply Current	(LV_{CC}UV+) - 0.1V		100	200	μA
I_OHV_{CC}	Operating HV_{CC} Supply Current (RMS Value)	f_{OSC}=100kHz, C_{Load}=1nF		5	8	mA
		No Switching		100	200	μA
I_OLV_{CC}	Operating LV_{CC} Supply Current (RMS Value)	f_{OSC}=100kHz, C_{Load}=1nF		[illegible]	9	mA
		No Switching		2	4	mA
UVLO Section						
LV_{CC}UV+	LV_{CC} Supply Under-Voltage Positive-Going Threshold (LV_{CC} Start)		12	12.5	13.8	V
LV_{CC}UV-	LV_{CC} Supply Under-Voltage Negative-Going Threshold (LV_{CC} Stop)		8.9	10.0	11.1	V
LV_{CC}UVH	LV_{CC} Supply Under-Voltage Hysteresis			2.5		V
HV_{CC}UV+	HV_{CC} Supply Under-Voltage Positive-Going Threshold (HV_{CC} Start)		8.2	9.2	10.2	V
HV_{CC}UV-	HV_{CC} Supply Under-Voltage Negative-Going Threshold (HV_{CC} Stop)		7.8	8.7	9.6	V
HV_{CC}UVH	HV_{CC} Supply Under-Voltage Hysteresis			0.5		V
Oscillator & Feedback Section						
V_{RT}	V-I Converter Threshold Voltage		1.5	2.0	2.5	V
f_{OSC}	Output Oscillation Frequency	R_T=5.2kΩ	94	100	106	kHz
DC	Output Duty Cycle		48	50	52	%
f_{SS}	Internal Soft-Start Initial Frequency	$f_{SS}=f_{OSC}$+40kHz, R_T=5.2kΩ		140		kHz
t_{SS}	Internal Soft-Start Time		2	3	4	ms
Output Section						
I_{source}	Peak Sourcing Current	HV_{CC}=17V	250	360		mA
	Peak Sinking Current	HV_{CC}=17V	460	600		mA
t_r	Rising Time	C_{Load}=1nF, HV_{CC}=17V		65		ns
t_f	Falling Time			35		ns
V_{HOH}	High Level of High-Side Gate Driving Signal (V_{HVCC}-V_{HO})	I_O=20mA			1.0	V
V_{HOL}	Low Level of High-Side Gate Driving Signal				0.6	V
V_{LOH}	High Level of High-Side Gate Driving Signal (V_{LVCC}-V_{LO})				1.0	V
V_{LOL}	Low Level of High-Side Gate Driving Signal				0.6	V

Electrical Characteristics (Continued)

T_A=25°C and LV_{CC}=17V unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Protection Section						
V_{CssH}	Beginning Voltage to Discharge C_{SS}		0.9	1.0	1.1	V
V_{CssL}	Beginning Voltage to Charge C_{SS} and Reset Protections		0.16	0.20	0.24	V
V_{OVP}	LV_{CC} Over-Voltage Protection	LV_{CC} > 21V	21	23	25	V
V_{AOCP}	AOCP Threshold Voltage	ΔV/Δt=-0.1V/μs	-1.0	-0.9	-0.8	V
t_{BAO}	AOCP Blanking Time(2)	V_{CS} < V_{AOCP}; ΔV/Δt=-0.1V/μs		50		ns
V_{OCP}	OCP Threshold Voltage	ΔV/Δt=-1V/μs	-0.64	-0.[illegible]	-0.52	V
t_{BO}	OCP Blanking Time(2)	V_{CS} < V_{OCP}; ΔV/Δt=-1V/μs	[illegible]	1.5	2.0	μs
t_{DA}	Delay Time (Low-Side) Detecting from V_{AOCP} to Switch Off(2)	ΔV/Δt=-1[illegible]		250	400	ns
T_{SD}	Thermal Shutdown Temperature(2)		110	130	150	°C
Dead-Time Control Section						
D_T	Dead Time(3)		[illegible]50			ns

Notes:
2. These parameters, although guaranteed, are not tested in production.
3. These parameters, although guaranteed, are tested only in EDS (wafer test) process.

Typical Performance Characteristics

These characteristic graphs are normalized at T_A=25ºC.

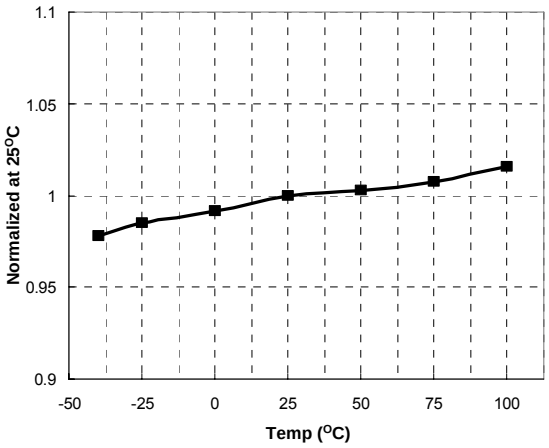


Figure 4. Low-Side MOSFET Duty Cycle vs. Temperature

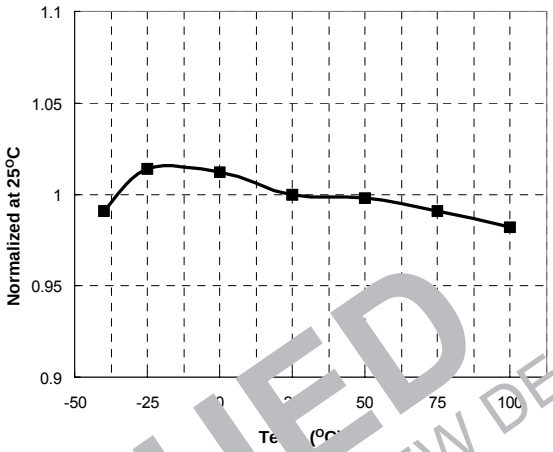


Figure 5. Switching Frequency vs. Temperature

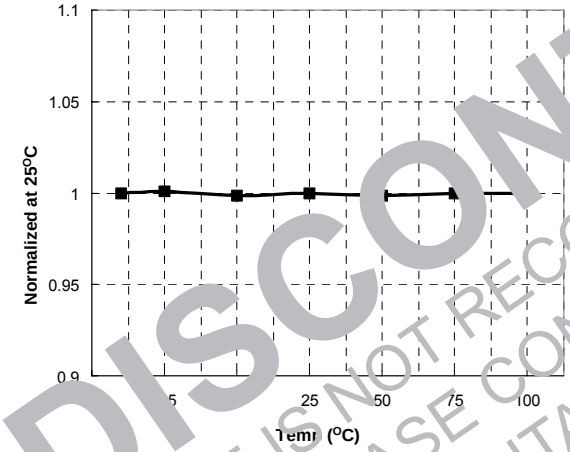


Figure 6. High-Side V_{CC} (HV_{CC}) Start vs. Temperature

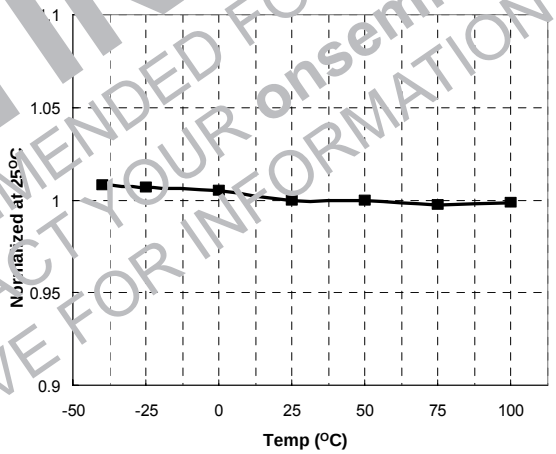


Figure 7. High-Side V_{CC} (HV_{CC}) Stop vs. Temperature

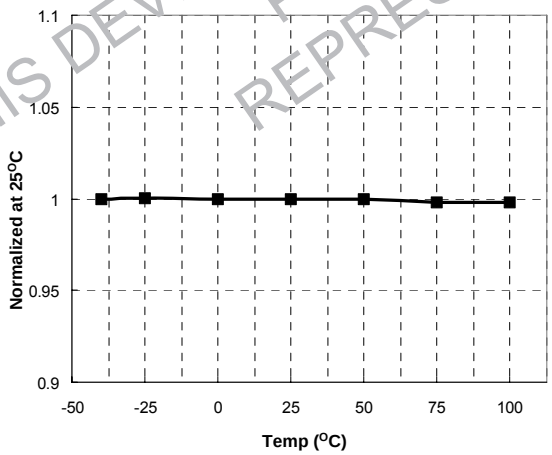


Figure 8. Low-Side V_{CC} (LV_{CC}) Start vs. Temperature

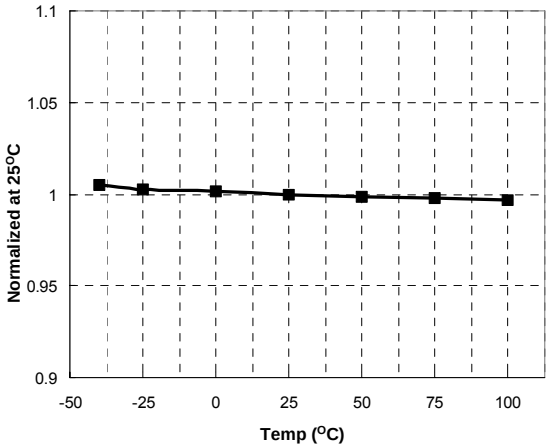


Figure 9. Low-Side V_{CC} (LV_{CC}) Stop vs. Temperature

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at T_A=25ºC.

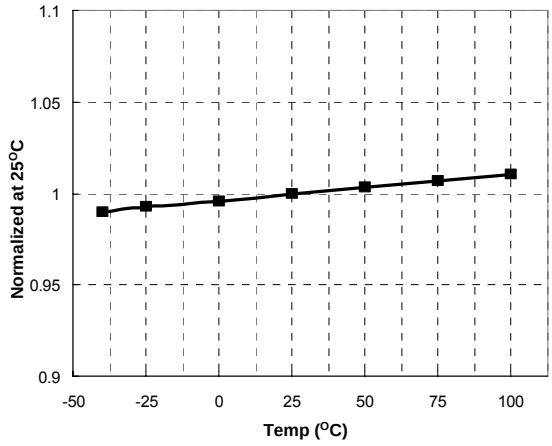


Figure 10. LV_{CC} OVP Voltage vs. Temperature

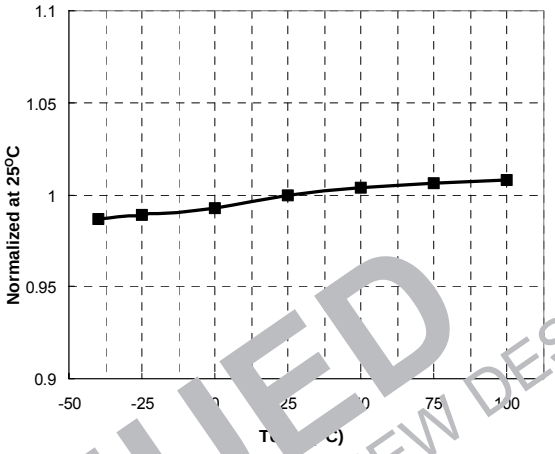


Figure 11. R Voltage vs. Temperature

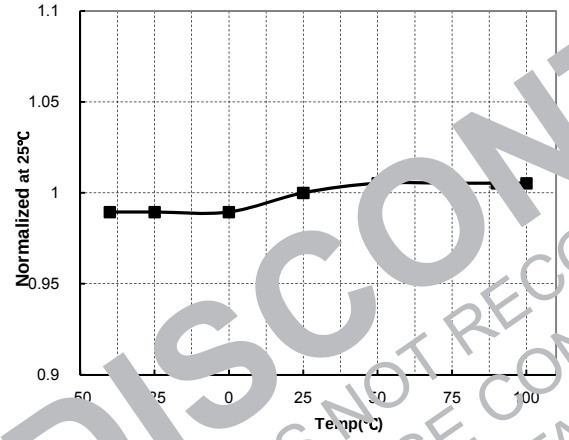


Figure 12. V_{CssL} vs. Temperature

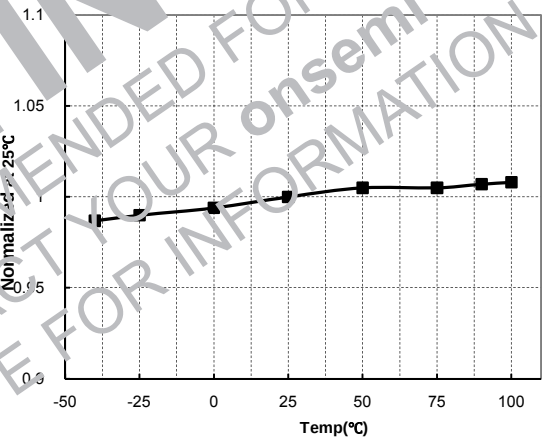


Figure 13. V_{CssH} vs. Temperature

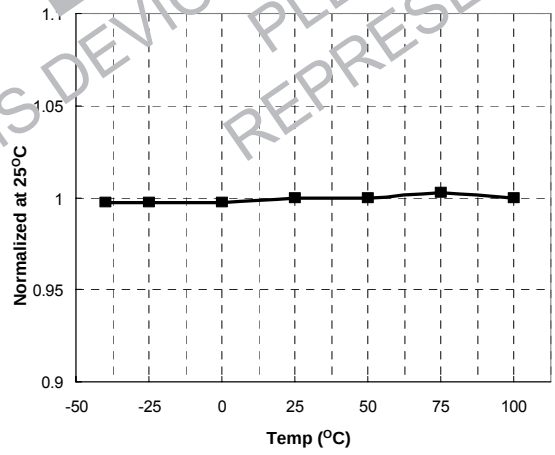


Figure 14. OCP Voltage vs. Temperature

Functional Description

1. Basic Operation: FAN7621S is designed to drive high-side and low-side MOSFETs complementarily with 50% duty cycle. A fixed dead time of 350ns is introduced between consecutive transitions, as shown in Figure 15.

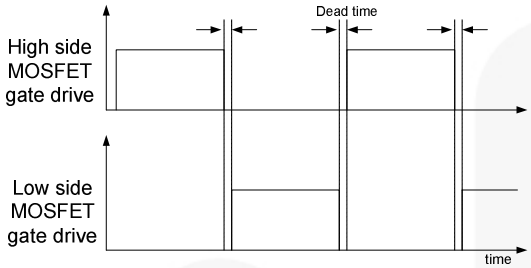


Figure 15. MOSFETs Gate Drive Signal

2. Internal Oscillator: FAN7621S employs a current-controlled oscillator, as shown in Figure 16. Internally, the voltage of R_T pin is regulated at 2V and the charging / discharging current for the oscillator capacitor, C_T, is obtained by copying the current flowing out of R_T pin (I_{CTC}) using a current mirror. Therefore, the switching frequency increases as I_{CTC} increases.

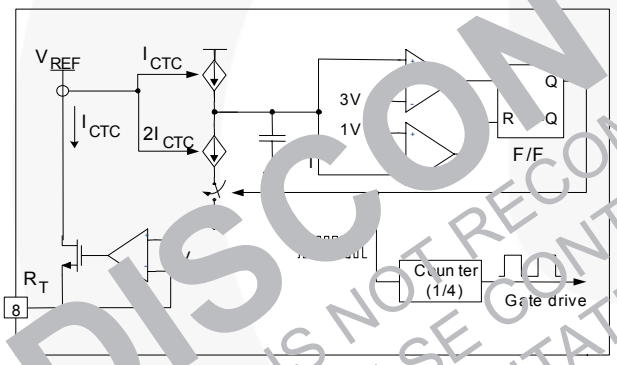


Figure 16. Current Controlled Oscillator

3. Frequency Setting: Figure 17 shows the typical voltage gain curve of a resonant converter, where the gain is inversely proportional to the switching frequency in the ZVS region. The output voltage can be regulated by modulating the switching frequency. Figure 18 shows the typical circuit configuration for R_T pin, where the opto-coupler transistor is connected to the R_T pin to modulate the switching frequency.

The minimum switching frequency is determined as:

$$f^{min} = \frac{5.2k\Omega}{R_{min}} \times 100(kHz) \quad (1)$$

Assuming the saturation voltage of the opto-coupler transistor is 0.2V, the maximum switching frequency is determined as:

$$f^{max} = (\frac{5.2k\Omega}{R_{min}} + \frac{4.68k\Omega}{R_{max}}) \times 100(kHz) \quad (2)$$

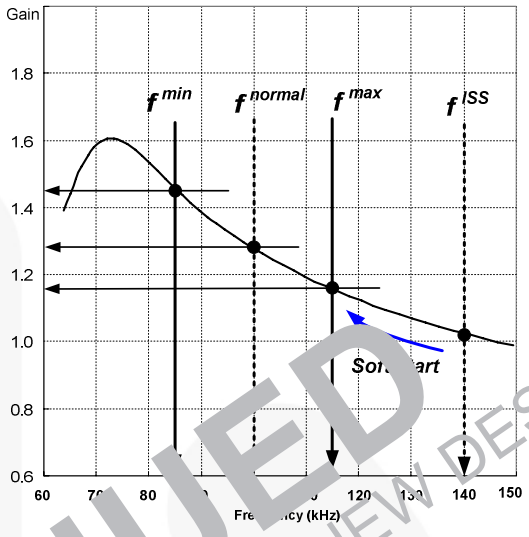


Figure 17. Resonant Converter Typical Gain Curve

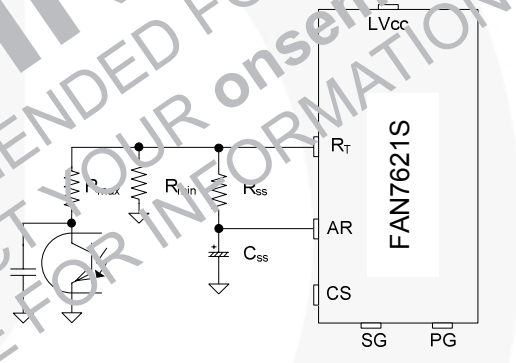


Figure 18. Frequency Control Circuit

To prevent excessive inrush current and overshoot of output voltage during startup, increase the voltage gain of the resonant converter progressively. Since the voltage gain of the resonant converter is inversely proportional to the switching frequency, the soft-start is implemented by sweeping down the switching frequency from an initial high frequency (f^{ISS}) until the output voltage is established. The soft-start circuit is made by connecting R-C series network on the R_T pin, as shown in Figure 18. FAN7621S also has an internal soft-start of 3ms to reduce the current overshoot during the initial cycles, which adds 40kHz to the initial frequency of the external soft-start circuit, as shown in Figure 19. The initial frequency of the soft-start is given as:

$$f^{ISS} = (\frac{5.2k\Omega}{R_{min}} + \frac{5.2k\Omega}{R_{SS}}) \times 100 + 40\ (kHz) \quad (3)$$

It is typical to set the initial (soft-start) frequency two ~ three times the resonant frequency (f_O) of the resonant network.

The soft-start time is three to four times the RC time constant. The RC time constant is as follows:

$$t_{SS} = R_{SS} \bullet C_{SS} \quad (4)$$

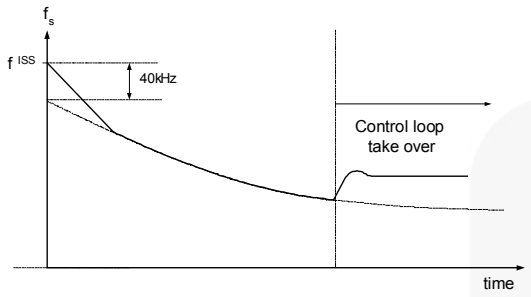


Figure 19. Frequency Sweeping of Soft-Start

4. Self Auto-restart: The FAN7621S can restart automatically even if a built-in protection is triggered with external supply voltage. As shown in Figure 20 and Figure 21; once any protections are triggered, M1 switch turns on and V-I converter is disabled. C_{SS} starts to be discharged until the V_{Css} across C_{SS} drops to V_{CssL}. Then all protections are reset, M1 turns off, and V-I converter resumes. The FAN7621S starts switching again with a soft start. If the protections occur while V_{Css} is under V_{CssL} and V_{CssH} level, the switching is terminated immediately, V_{Css} continues to increase until reaching V_{CssH}, then C_{SS} is discharged by M1.

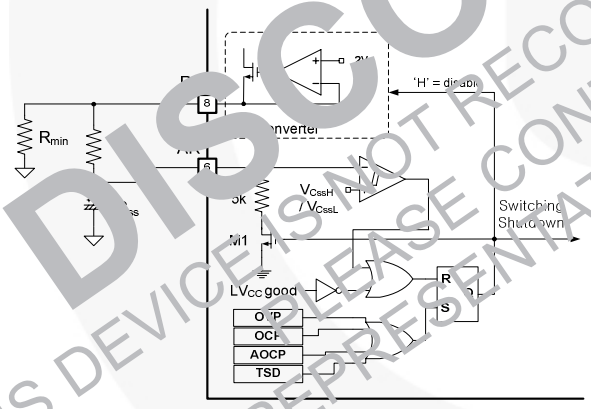
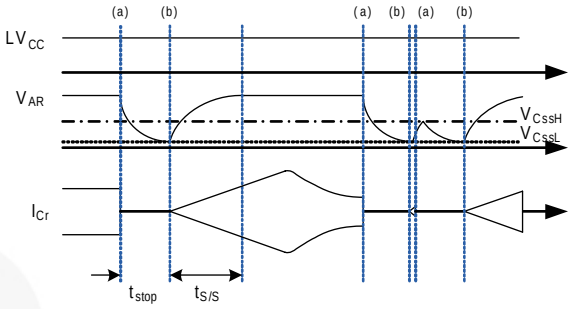


Figure 20. Internal Block of AR Pin

After protections trigger, FAN7621S is disabled during the stop-time, t_{stop}, where V_{Css} decreases and reaches to V_{CssL}. The stop-time of FAN7621S can be estimated as:

$$t_{stop} = C_{ss} \cdot \{(R_{ss} + R_{min}) \parallel 5k\Omega\} \quad (5)$$

For the soft-start time, $t_{s/s}$ it can be set as Equation (4).



(a) Protections are triggered, (b) FSFR-US restarts

Figure 21. Self Auto-Restart Operation

5. Protection Circuits: The FAN7621S has several self-protective functions, such as Over-Current Protection (OCP), Abnormal Over-Current Protection (AOCP), Over-Voltage Protection (OVP), and Thermal Shutdown (TSD). These protections are auto-restart mode protections, as shown in Figure 21.

Once a fault condition is detected, switching is terminated and the MOSFETs remain off. When LV_{CC} falls to the stop voltage of 10V or the AR signal is HIGH, the protection is reset. FAN7621S resumes normal operation when LV_{CC} reaches the start voltage of 12.5V.

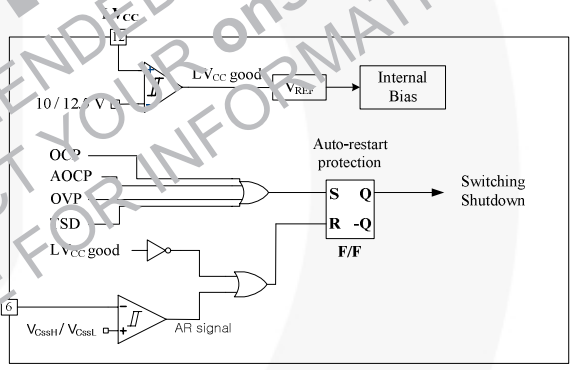


Figure 22. Protection Blocks

5.1 Over-Current Protection (OCP): When the sensing pin voltage drops below -0.58V, OCP is triggered and the MOSFETs remain off. This protection has a shutdown time delay of 1.5μs to prevent premature shutdown during startup.

5.2 Abnormal Over-Current Protection (AOCP): If the secondary rectifier diodes are shorted, large current with extremely high di/dt can flow through the MOSFET before OCP is triggered. AOCP is triggered without shutdown delay when the sensing pin voltage drops below -0.9V.

5.3 Over-Voltage Protection (OVP): When the LV_{CC} reaches 23V, OVP is triggered. This protection is used when auxiliary winding of the transformer to supply V_{CC} to the controller is utilized.

5.4 Thermal Shutdown (TSD): If the temperature of the junction exceeds approximately 130°C, the thermal shutdown triggers.

6. Current Sensing Using Resistor: FAN7621S senses drain current as a negative voltage, as shown in Figure 23 and Figure 24. Half-wave sensing allows low power dissipation in the sensing resistor, while full-wave sensing has less switching noise in the sensing signal.

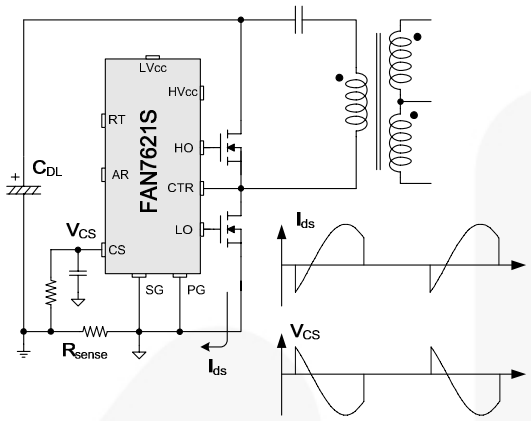


Figure 23. Half-Wave Sensing

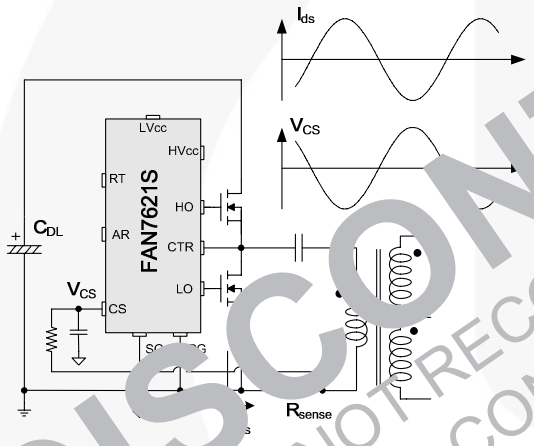


Figure 24. Full-Wave Sensing

7. PCB Layout Guidelines: Duty imbalance problems may occur due to the radiated noise from the main transformer, the inequality of the secondary-side leakage inductances of main transformer, and so on. It is one of the dominant reasons that the control components in the vicinity of R_T pin are enclosed by the primary current flow pattern on PCB layout. The direction of the magnetic field on the components caused by the primary current flow is changed when the high- and low-side MOSFET turns on by turns. The magnetic fields with opposite direction from each other induce a current through, into, or out of the R_T pin, which makes the turn-on duration of each MOSFET different. It is strongly recommended to separate the control components in the vicinity of R_T pin from the primary current flow pattern on PCB layout. **Error! Reference source not found.** shows an example for the duty-balanced case. The yellow and blue lines show the primary current flows when the lower-side and higher side MOSFETs turn on, respectively. The primary current does not enclose any component of controller.

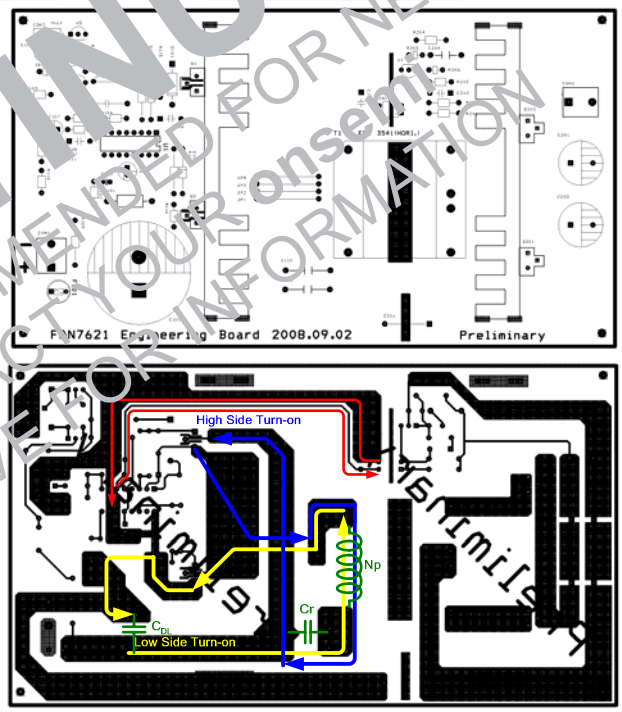
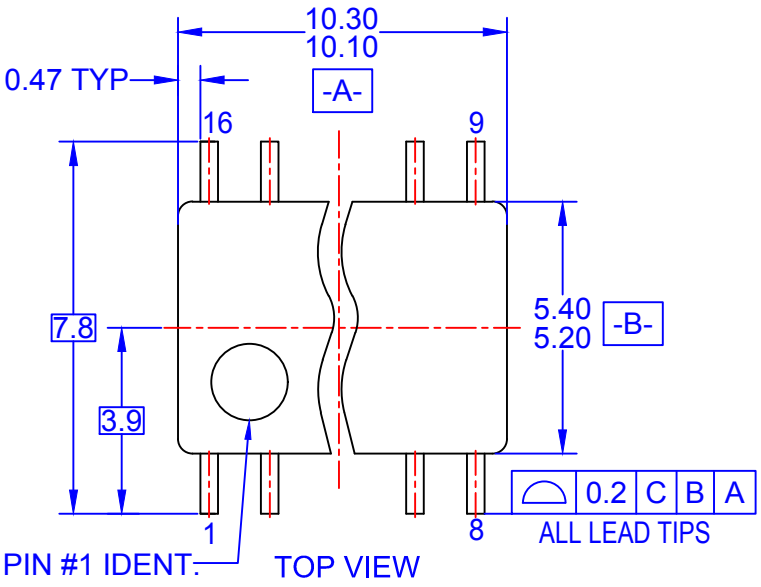
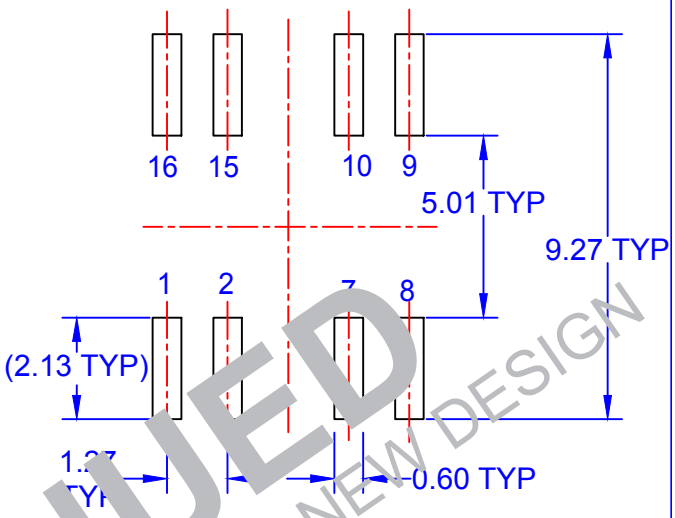
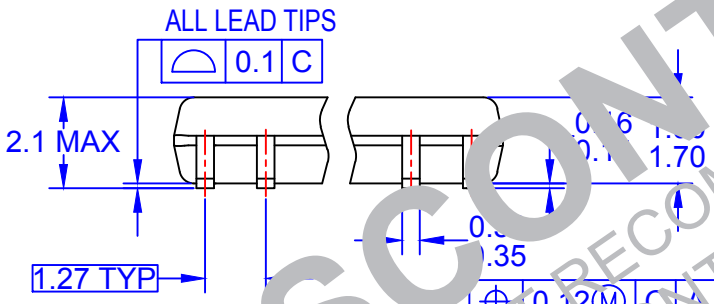


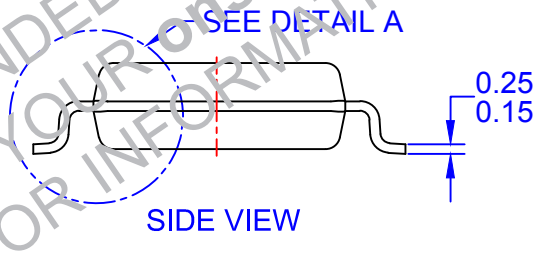
Figure 25. Example for Duty Balancing

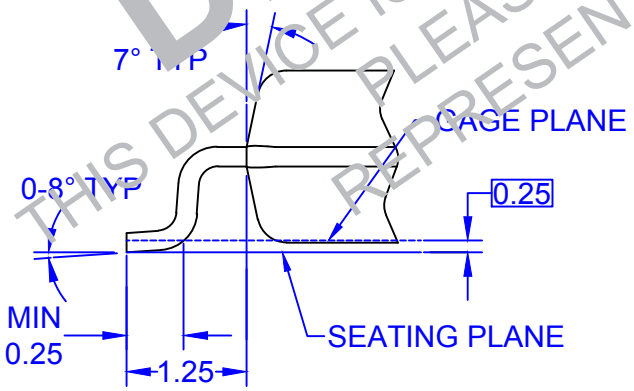




LAND PATTERN RECOMMENDATION







DETAIL A

NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DRAWING FILENAME: MKT-M16Drev5

FAIRCHILD ™

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