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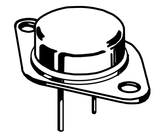
ON Semiconductor™

BU208A

5.0 AMPERES
NPN SILICON
POWER TRANSISTOR
700 VOLTS



CASE 1–07
TO–204AA
(TO–3)

Horizontal Deflection Transistor

. . . designed for use in televisions.

- Collector–Emitter Voltages V_{CES} 1500 Volts
- Fast Switching — 400 ns Typical Fall Time
- Low Thermal Resistance 1°C/W Increased Reliability
- Glass Passivated (Patented Photoglass). Triple Diffused Mesa Technology for Long Term Stability

MAXIMUM RATINGS

Rating	Symbol	BU208A	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	700	Vdc
Collector–Emitter Voltage	V_{CES}	1500	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous — Peak	I_C I_{CM}	5.0 7.5	Vdc
Base Current — Continuous — Peak (Negative)	I_B I_{BM}	4.0 3.5	Adc
Total Power Dissipation @ T_C = 95°C Derate above 95°C	P_D	12.5 0.625	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +115	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.6	°C/W
Maximum Lead Temperature for Soldering Purpose, 1/8″ from Case for 5 Seconds	T_L	275	°C

NOTES:
1. Pulsed 5.0 ms, Duty Cycle ≤ 10%.
2. See page 3 for Additional Ratings on A Type.
3. Figures in ( ) are Standard Ratings ON Semiconductor Guarantees are Superior.

March, 2001 – Rev. 9

Publication Order Number:
BU208A/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, L = 25 mH)	$V_{CEO(sus)}$	700	—	—	Vdc
Collector Cutoff Current[1] ALL TYPES (V_{CE} = rated V_{CES}, V_{BE} = 0)	I_{CES}	—	—	1.0	mAdc
Emitter Base Voltage[1]	V_{EBO}				Vdc
(I_C = 0, I_E = 10 mAdc)		5	—	—	
(I_C = 0, I_E = 100 mAdc)		—	7	—	
ON CHARACTERISTICS[1]					
DC Current Gain (I_C = 4.5 Adc, V_{CE} = 5 Vdc)	h_{FE}	2.25	—	—	
Collector–Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2 Adc)	$V_{CE(sat)}$	—	—	1	Vdc
Base–Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2 Adc)	$V_{BE(sat)}$	—	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 5 Vdc, f_{test} = 1 MHz)	f_T	—	4	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	—	125	—	pF
SWITCHING CHARACTERISTICS					
Storage Time (see test circuit fig. 1) (I_C = 4.5 Adc, I_{B1} = 1.8 Adc, L_B = 10 μH)	t_s	—	8	—	μs
Fall time (see test circuit fig. 1) (I_C = 4.5 Adc, I_{B1} = 1.8 Adc, L_B = 10 μH)	t_f	—	0.4	—	μs

[1]Pulse test: PW = 300 μs; Duty cycle ≤ 2%.

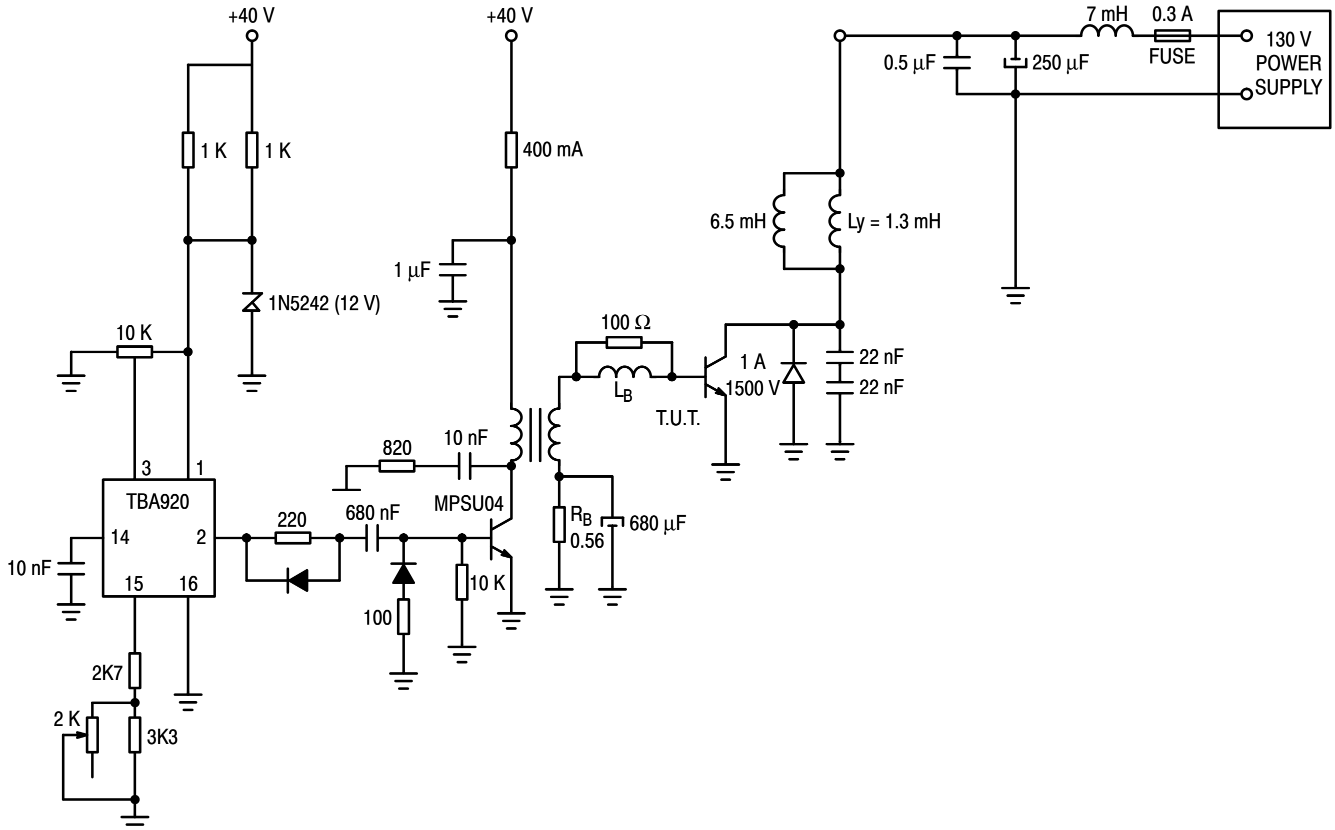


Figure 1. Switching Time Test Circuit

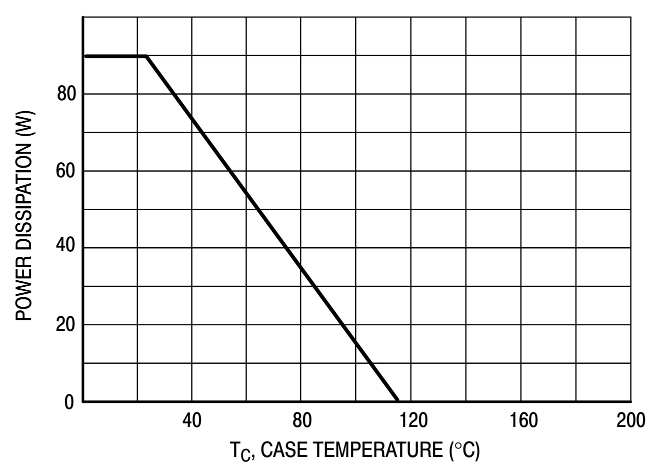


Figure 2. Power Derating

BASE DRIVE
The Key to Performance

By now, the concept of controlling the shape of the turn–off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn–off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM}. Worst–case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn–off base current will reverse very quickly as shown in Figure 3. This results in rapid, but only partial collector turn–off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 4, thus allowing access carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B Is usually done empirically since the equivalent circuit is complex, and since there are several important variables (I_{CM}, I_{B1}, and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B, at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B.

This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. For very low L_B a very narrow optimum is obtained. This occurs when I_{B1} h_{FE} $\cong$ I_{CM}, and therefore would be acceptable only for the “typical” device with constant I_{CM}. As L_B is increased, the curves become broader and flatter above the I_{B1}. h_{FE} = I_{CM} point as the turn off “tails” are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor initiation of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE}, essentially moves the curves to the left, or right according to the relation I_{B1} h_{FE} = constant. It then becomes obvious that, for a specified I_{CM}, an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1}. The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Neither L_B nor I_{B1} are absolutely critical. Due to the high gain of ON Semiconductor devices it is suggested that in general a low value of I_{B1} be used to obtain optimum efficiency — eg. for BU208A with I_{CM} = 4.5 A use I_{B1} $\approx$ 1.5 A, at I_{CM} = 4 A use I_{B1} $\approx$ 1.2 A. These values are lower than for most competition devices but practical tests have showed comparable efficiency for ON Semiconductor devices even at the higher level of I_{B1}.

An L_B of 10 μH to 12 μH should give satisfactory operation of BU208A with I_{CM} of 4 to 4.5 A and I_{B1} between 1.2 and 2 A.

TEST CIRCUIT WAVEFORMS

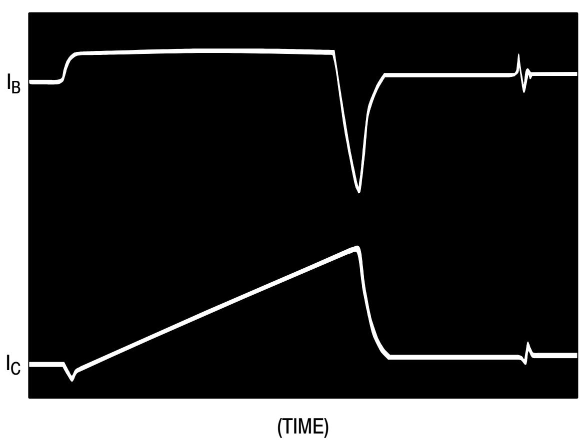


Figure 3.

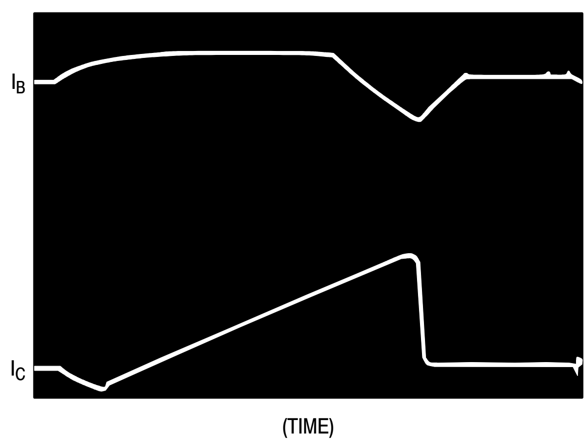


Figure 4.

TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance. Once the required transistor operating current is determined, fixed circuit values may be selected.

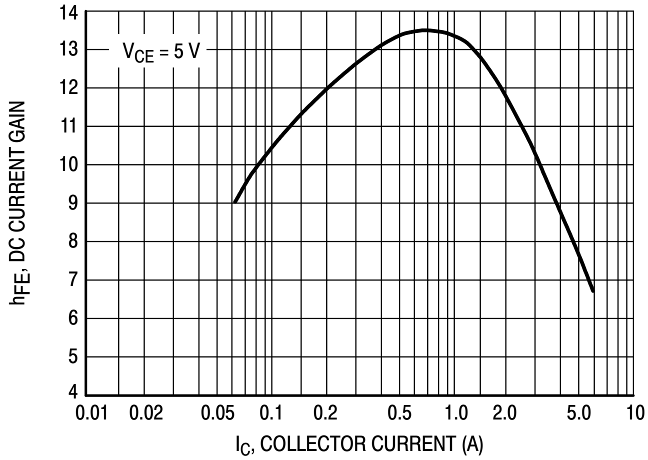


Figure 5. DC Current Gain

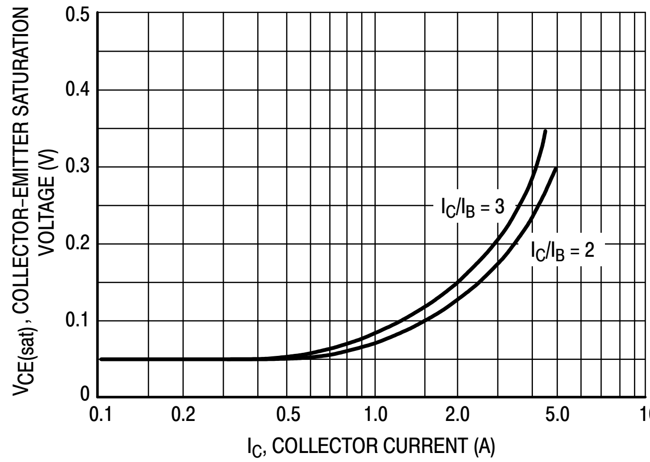


Figure 6. Collector−Emitter Saturation Voltage

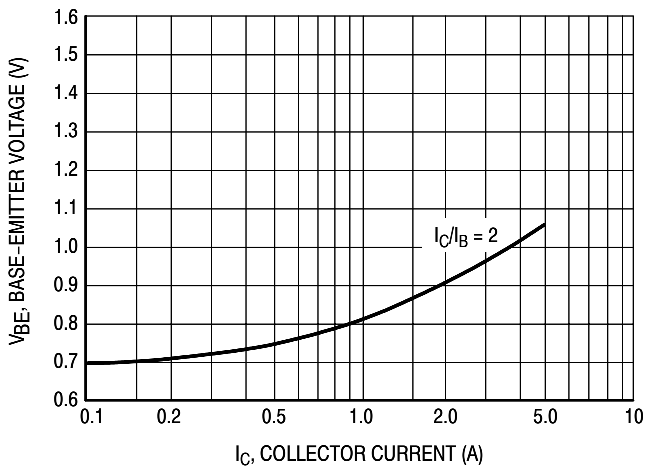


Figure 7. Base−Emitter Saturation Voltage

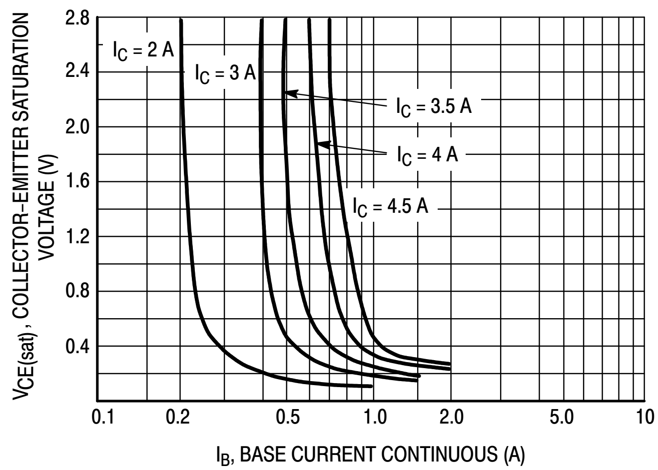


Figure 8. Collector Saturation Region

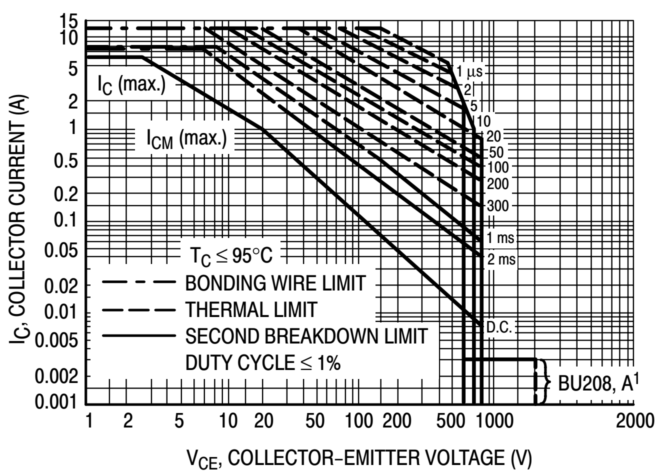
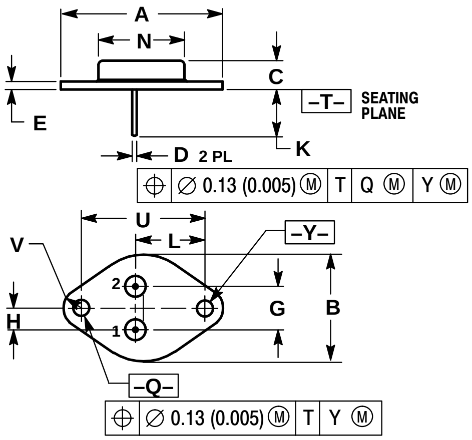


Figure 9. Maximum Forward Bias Safe Operating Area

[1]Pulse width ≤ 20 μs. Duty cycle ≤ 0.25. R_{BE} ≤ 100 Ohms.

PACKAGE DIMENSIONS

CASE 1–07
TO–204AA (TO–3)
ISSUE Z



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

Notes

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Phone: 1–303–675–2121 (Tue–Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:
001–800–4422–3781
Email: ONlit–asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031
Phone: 81–3–5740–2700
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

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