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MOSFET - PowerTrench®
Power Clip, Asymmetric, Dual N-Channel
30 V

NTMFD2D4N03P8

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General Description

This device includes two specialized N−Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET (Q2) have been designed to provide optimal power efficiency.

Features

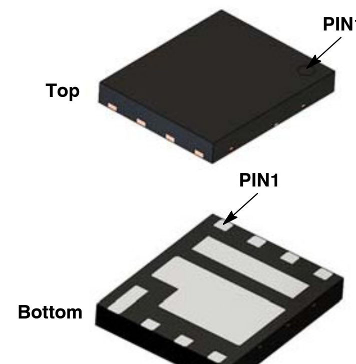
Q1: N−Channel
- Max $r_{DS(on)}$ = 5.0 mΩ at V_{GS} = 10 V, I_D = 17 A
- Max $r_{DS(on)}$ = 6.5 mΩ at V_{GS} = 4.5 V, I_D = 14 A

Q2: N−Channel
- Max $r_{DS(on)}$ = 2.4 mΩ at V_{GS} = 10 V, I_D = 25 A
- Max $r_{DS(on)}$ = 3.0 mΩ at V_{GS} = 4.5 V, I_D = 22 A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- MOSFET Integration Enables Optimum Layout for Lower Circuit Inductance and Reduced Switch Node Ringing
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

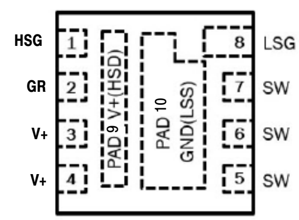
Applications

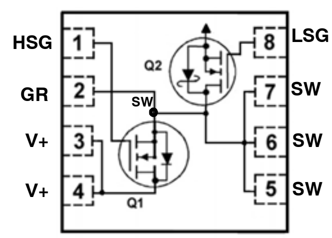
- Computing
- Communications
- General Purpose Point of Load

Pin	Name	Description
1	HSG	High Side Gate
2	GR	Gate Return
3, 4, 9	V+(HSD)	High Side Drain
5, 6, 7	SW	Switching Node, Low Side Drain
8	LSG	Low Side Gate
10	GND(LSS)	Low Side Source



PQFN8
POWER CLIP
CASE 483AR





ORDERING INFORMATION

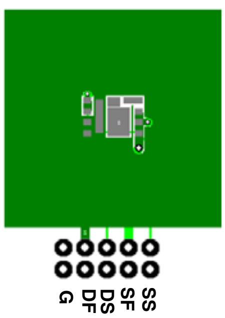
See detailed ordering and shipping information on page 3 of this data sheet.

Table 1. MOSFET MAXIMUM RATINGS T_A = 25°C unless otherwise noted.

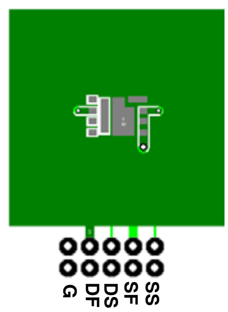
Symbol	Parameter		Q1	Q2	Units
V_{DS}	Drain to Source Voltage		30	30	V
B_{VDDST}	B_{VDDST} (transient) < 100 ns		36	36	V
V_{GS}	Gate to Source Voltage		±20	±12	V
I_D	Drain Current − Continuous	T_C = 25°C (Note 1)	56	84	A
	− Continuous	T_C = 100°C (Note 1)	35	53	
	− Continuous	T_A = 25°C	17 (Note 4)	25 (Note 5)	
	− Pulsed	T_A = 25°C (Note 2)	227	503	
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	54	96	mJ
P_D	Power Dissipation for Single Operation	T_C = 25°C	23	25	W
	Power Dissipation for Single Operation	T_A = 25°C	2.1 (Note 4)	2.3 (Note 5)	
	Power Dissipation for Single Operation	T_A = 25°C	1.0 (Note 6)	1.1 (Note 7)	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

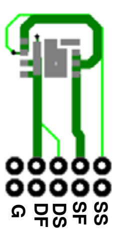
1. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro−mechanical application board design.
2. Pulsed Id refer to Figure 11 and Figure 24 SOA curve for more details.
3. Q1 :EAS of 54 mJ is based on starting T_J = 25°C; L = 3 mH, I_{AS} = 6 A, V_{DD} = 30 V, V_{GS} = 10 V. 100% tested at L = 0.1 mH, I_{AS} = 20 A.
   Q2: EAS of 96 mJ is based on starting T_J = 25°C; L = 3 mH, I_{AS} = 8 A, V_{DD} = 30 V, V_{GS} = 10 V. 100% tested at L = 0.1 mH, I_{AS} = 27 A.



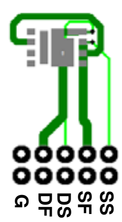
4. 60°C/W when mounted on a 1 in^2 pad of 2 oz copper



5. 55°C/W when mounted on a 1 in^2 pad of 2 oz copper



6. 130°C/W when mounted on a 1 in^2 pad of 2 oz copper



7. 120°C/W when mounted on a 1 in^2 pad of 2 oz copper

Table 2. PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
D2D4	NTMFD2D4N03P8	Power Clip 56	13″	12 mm	3000 units

Table 3. THERMAL CHARACTERISTICS

$R_{\theta JC}$	Thermal Resistance, Junction to Case	5.6	4.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	60 (Note 8)	55 (Note 8)	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	130 (Note 8)	120 (Note 8)	

8. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material, $R_{\theta CA}$ is determined by the user's board design.

Table 4. ELECTRICAL CHARACTERISTICS T_J = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V I_D = 1 mA, V_{GS} = 0 V	Q1 Q2	30 30			V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C I_D = 10 mA, referenced to 25°C	Q1 Q2		15 16		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V V_{DS} = 24 V, V_{GS} = 0 V	Q1 Q2			1 500	μA μA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V V_{GS} = 12 V, V_{DS} = 0 V	Q1 Q2			100 100	nA nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA V_{GS} = V_{DS}, I_D = 1 mA	Q1 Q2	1.0 1.0	1.7 1.6	3.0 3.0	V
$\Delta V_{GS(th)}$ / ΔT_J	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C I_D = 10 mA, referenced to 25°C	Q1 Q2		−5 −3		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10 V, I_D = 17 A V_{GS} = 4.5 V, I_D = 14 A V_{GS} = 10 V, I_D = 17 A, T_J = 125°C	Q1		4.1 5.4 5.7	5.0 6.5 7.0	mΩ
		V_{GS} = 10 V, I_D = 25 A V_{GS} = 4.5 V, I_D = 22 A V_{GS} = 10 V, I_D = 25 A, T_J = 125°C	Q2		1.9 2.4 2.7	2.4 3.0 3.4	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 17 A V_{DS} = 5 V, I_D = 25 A	Q1 Q2		93 139		S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	Q1: V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ Q2: V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2		1224 2730	1715 3825	pF
C_{oss}	Output Capacitance		Q1 Q2		397 801	560 1125	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		42 72	60 100	pF
R_g	Gate Resistance		Q1 Q2	0.1 0.1	0.5 1.1	1.5 2.2	Ω
SWITCHING CHARACTERISTICS							
$t_{d(on)}$	Turn−On Delay Time	Q1: V_{DD} = 15 V, I_D = 17 A, R_{GEN} = 6 Ω Q2: V_{DD} = 15 V, I_D = 25 A, R_{GEN} = 6 Ω	Q1 Q2		8 10	16 19	ns
t_r	Rise Time		Q1 Q2		2 4	10 10	ns
$t_{d(off)}$	Turn−Off Delay Time		Q1 Q2		18 30	33 48	ns
t_f	Fall Time		Q1 Q2		2 3	10 10	ns

Table 4. ELECTRICAL CHARACTERISTICS T_J = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions		Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS								
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V	Q1 V_{DD} = 15 V, I_D = 17 A Q2 V_{DD} = 15 V, I_D = 25 A	Q1 Q2		17 39	24 55	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V		Q1 Q2		8 18	11 26	nC
Q_{gs}	Gate to Source Gate Charge			Q1 Q2		3.1 6.1		nC
Q_{gd}	Gate to Drain “Miller” Charge			Q1 Q2		2.0 4.3		nC
DRAIN−SOURCE DIODE CHARACTERISTICS								
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 17 A (Note 9) V_{GS} = 0 V, I_S = 25 A (Note 9)		Q1 Q2		0.8 0.8	1.2 1.2	V
t_{rr}	Reverse Recovery Time	Q1 I_F = 17 A, di/dt = 100 A/μs Q2 I_F = 25 A, di/dt = 230 A/μs		Q1 Q2		23 27	37 44	ns
Q_{rr}	Reverse Recovery Charge			Q1 Q2		8 31	16 50	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.

Typical Characteristics (Q1 N−Channel) T_J = 25°C unless otherwise noted.

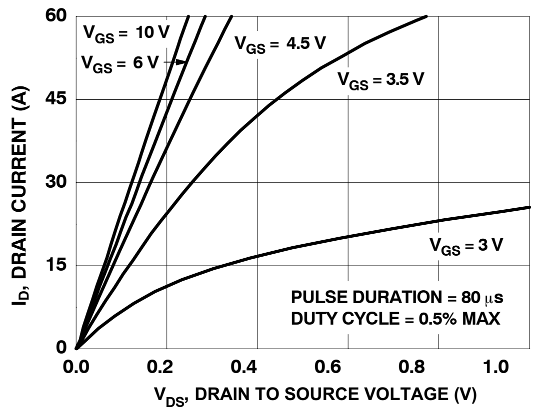


Figure 1. On Region Characteristics

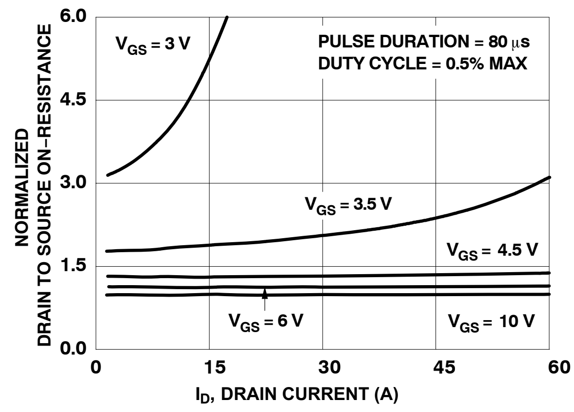


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

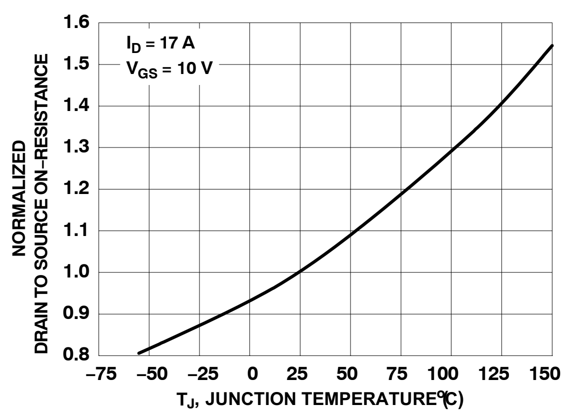


Figure 3. Normalized On−Resistance vs. Junction Temperature

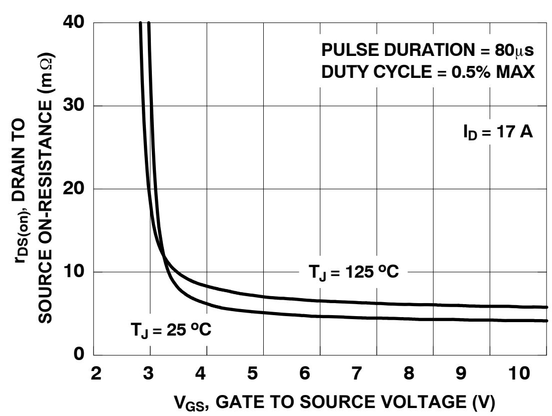


Figure 4. On−Resistance vs. Gate to Source Voltage

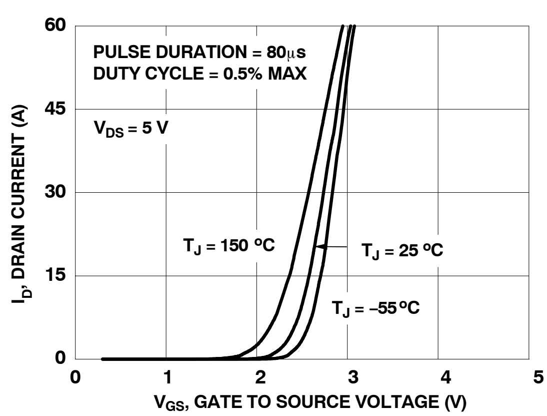


Figure 5. Transfer Characteristics

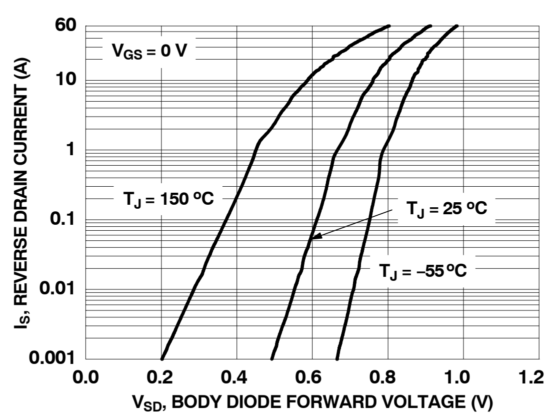


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics (Q1 N−Channel) T_J = 25°C unless otherwise noted.

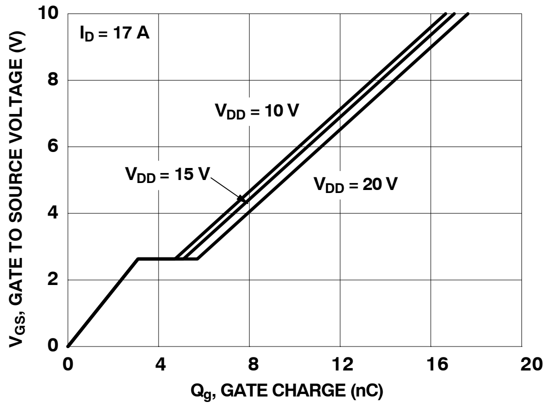


Figure 7. Gate Charge Characteristics

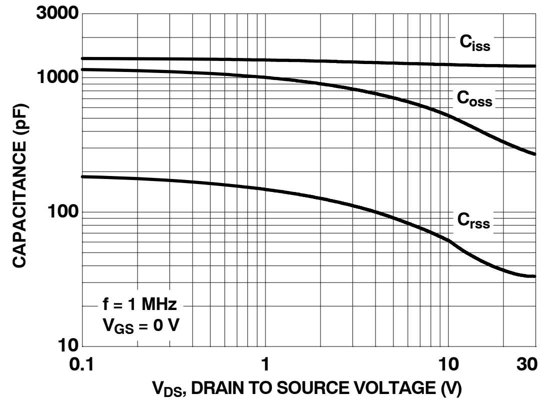


Figure 8. Capacitance vs. Drain to Source Voltage

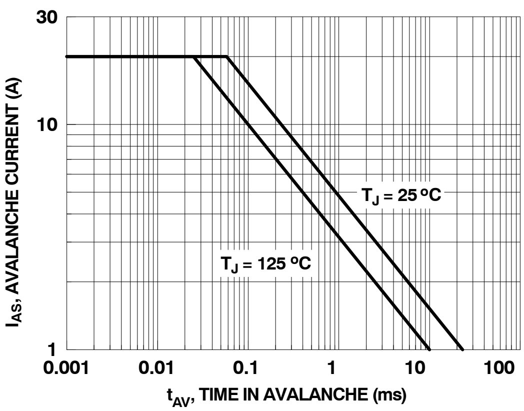


Figure 9. Unclamped Inductive Switching Capability

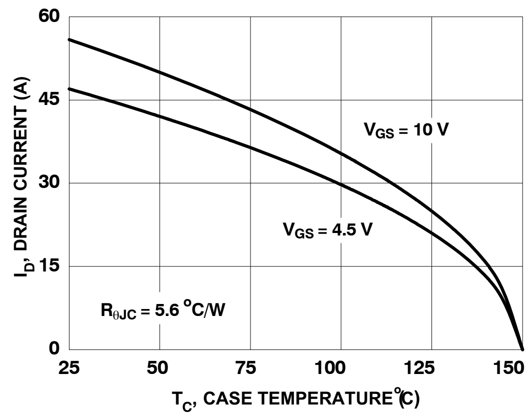


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

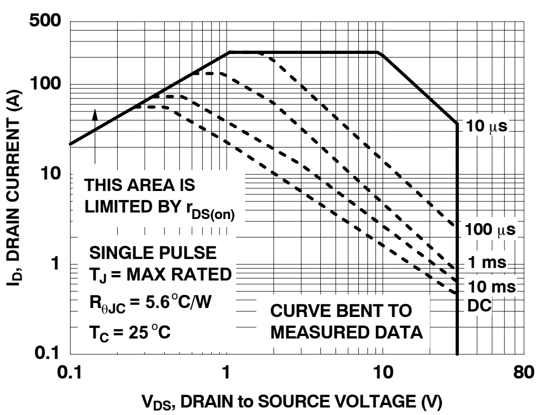


Figure 11. Forward Bias Safe Operating Area

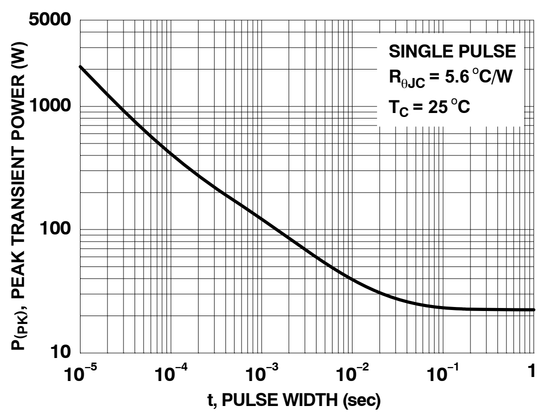


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N−Channel) T_J = 25°C unless otherwise noted.

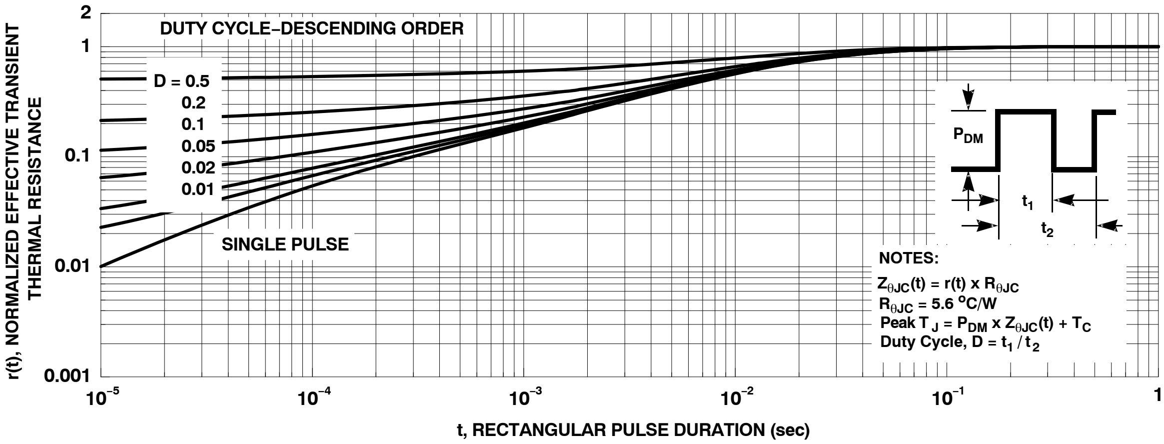


Figure 13. Junction−to−Case Transient Thermal Response Curve

Typical Characteristics (Q2 N−Channel) T_J = 25°C unless otherwise noted.

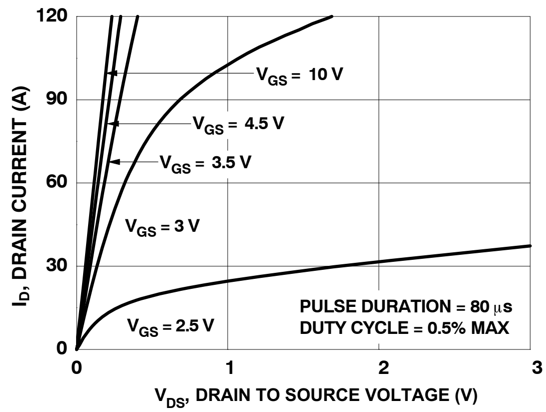


Figure 14. On Region Characteristics

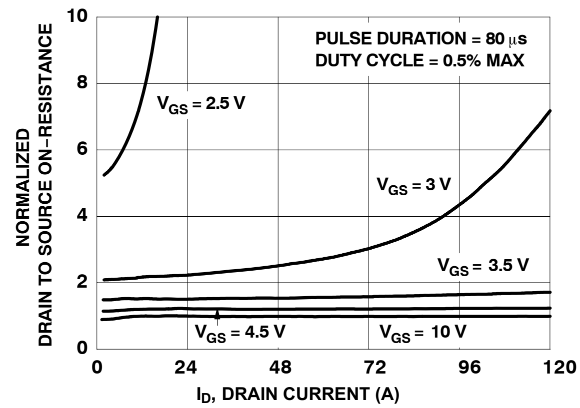


Figure 15. Normalized On−Resistance vs. Drain Current and Gate Voltage

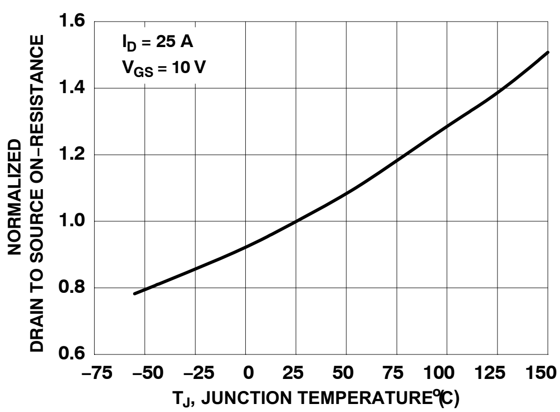


Figure 16. Normalized On−Resistance vs. Junction Temperature

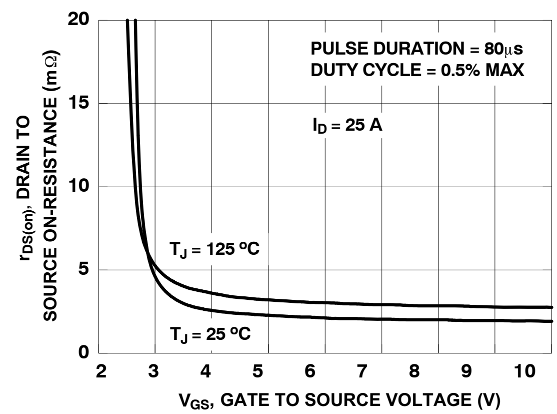


Figure 17. On−Resistance vs. Gate to Source Voltage

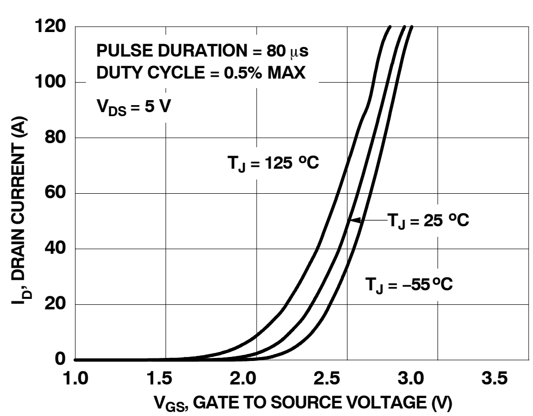


Figure 18. Transfer Characteristics

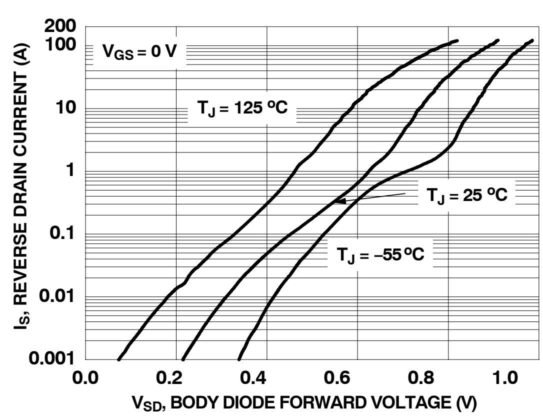


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics (Q2 N−Channel) T_J = 25°C unless otherwise noted.

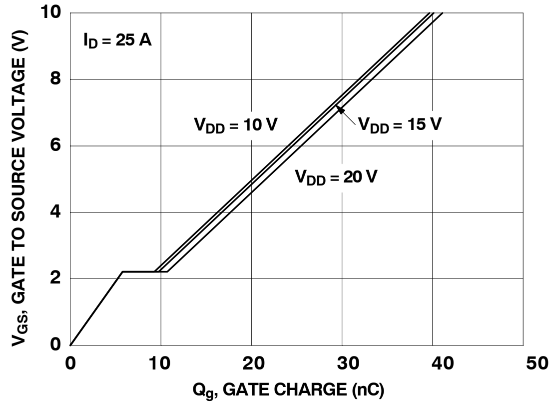


Figure 20. Gate Charge Characteristics

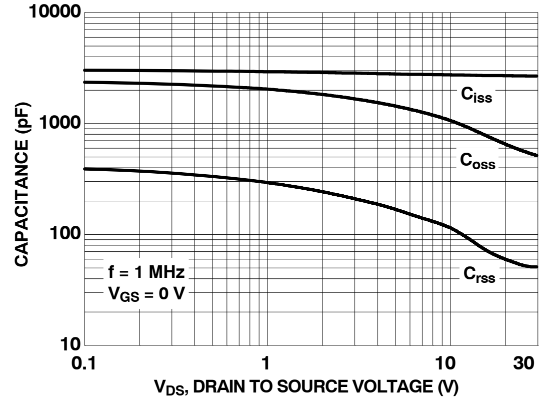


Figure 21. Capacitance vs. Drain to Source Voltage

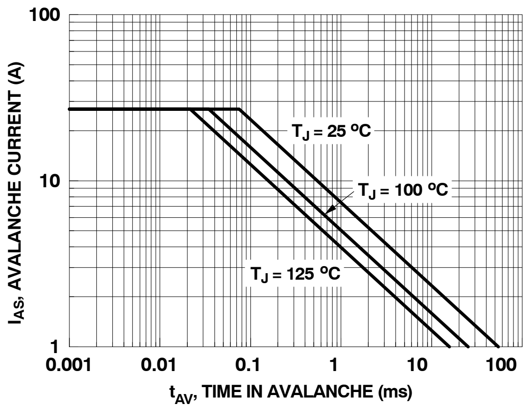


Figure 22. Unclamped Inductive Switching Capability

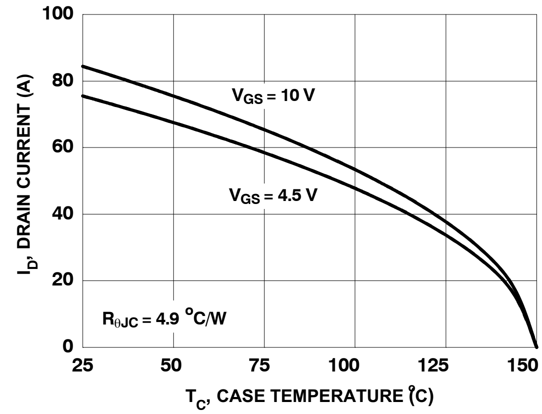


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

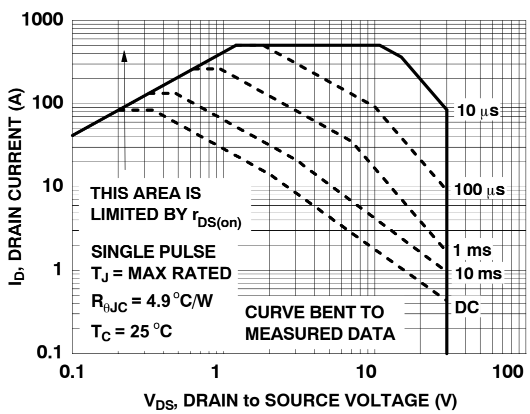


Figure 24. Forward Bias Safe Operating Area

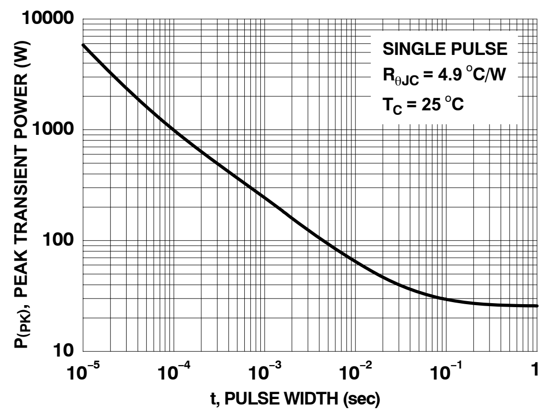


Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N−Channel) T_J = 25°C unless otherwise noted.

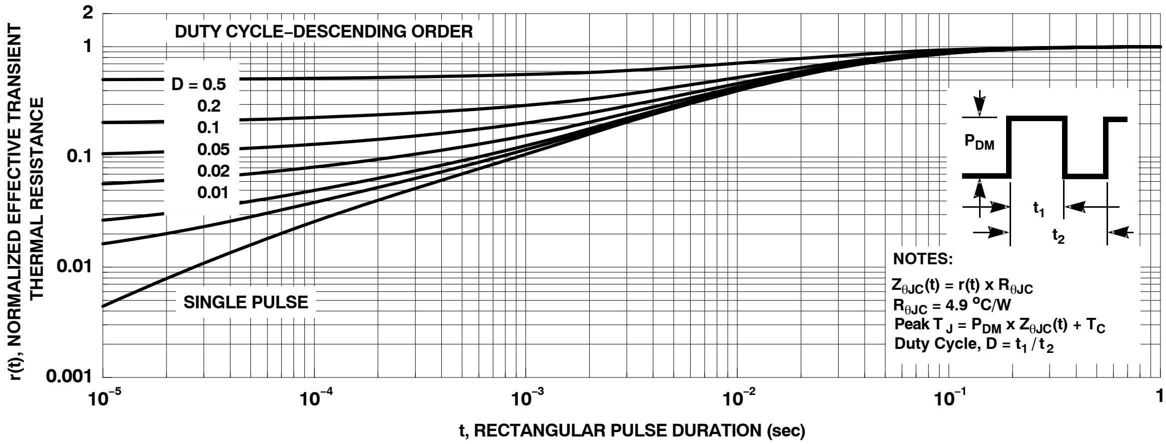


Figure 26. Junction−to−Case Transient Thermal Response Curve

Typical Characteristics

SyncFET Schottky Body Diode Characteristics

ON Semiconductor's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDPC5018SG.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

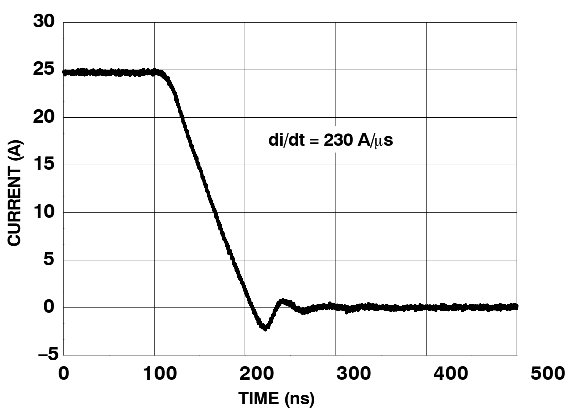


Figure 27. SyncFET Body Diode Reverse Recovery Characteristic

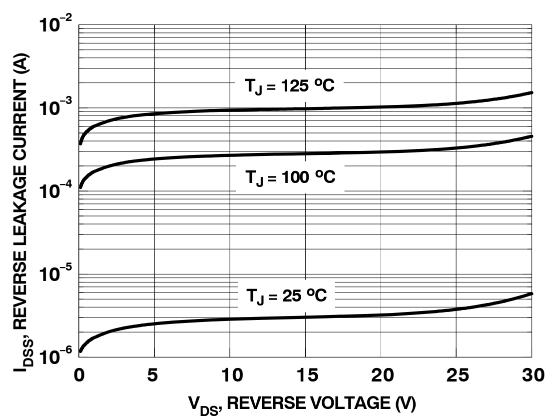
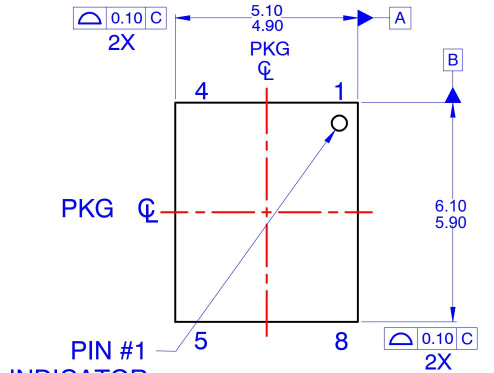


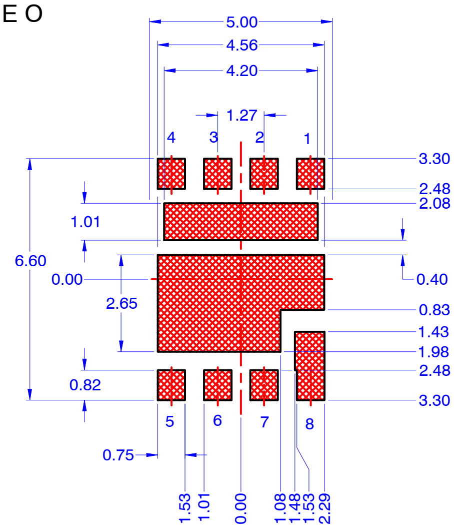
Figure 28. SyncFET Body Diode Reverse Leakage vs. Drain−Source Voltage

PACKAGE DIMENSIONS

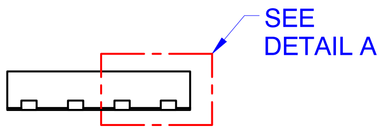
PQFN8 5X6, 1.27P
CASE 483AR
ISSUE O



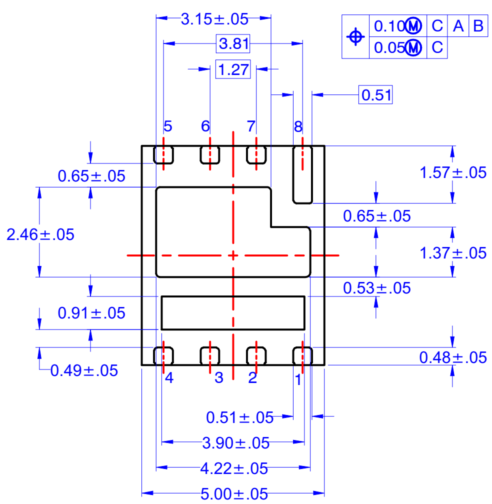
TOP VIEW



RECOMMENDED LAND PATTERN



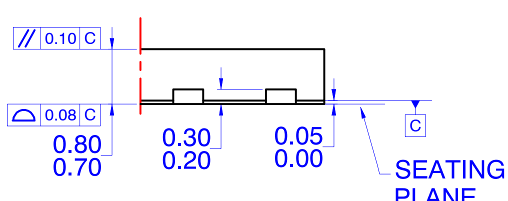
SIDE VIEW



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO−229, DATED 11/2001.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.



DETAIL A
(SCALE: 2X)

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PUBLICATION ORDERING INFORMATION

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