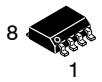
High Side Driver, Self Protected, Very Low Iq, with Analog Current Sense

NCV84090



SOIC−8
CASE 751
STYLE 11

The NCV84090 is a fully protected single channel high side driver that can be used to switch a wide variety of loads, such as bulbs, solenoids, and other actuators. The device incorporates advanced protection features such as active inrush current management, over−temperature shutdown with automatic restart and an overvoltage active clamp. A dedicated Current Sense pin provides precision analog current monitoring of the output as well as fault indication of short to V_D, short circuit to ground and ON and OFF state open load detection. An active high Current Sense Enable pin allows all diagnostic and current sense features to be enabled.

Features

- Short Circuit Protection with Inrush Current Management
- CMOS (3 V / 5 V) Compatible Control Input
- Very Low Standby Current
- Very Low Current Sense Leakage
- Proportional Load Current Sense
- Current Sense Enable
- Off State Open Load Detection
- Output Short to V_D Detection
- Overload and Short to Ground Indication
- Thermal Shutdown with Automatic Restart
- Undervoltage Shutdown
- Integrated Clamp for Inductive Switching
- Loss of Ground and Loss of V_D Protection
- ESD Protection
- Reverse Battery Protection with External Components
- AEC−Q100 Grade 1 Qualified and PPAP Capable
- This is a Pb−Free Device

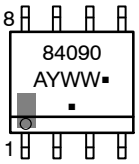
Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

FEATURE SUMMARY

Max Supply Voltage	V_D	41	V
Operating Voltage Range	V_D	4 to 28	V
R_{DSon} (typical) T_J = 25°C	R_{ON}	90	mΩ
Output Current Limit (typical)	I_{lim}	24	A
OFF−state Supply Current (max)	$I_{D(off)}$	0.5	μA

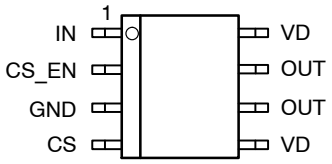
MARKING DIAGRAM



84090	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCV84090DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Block Diagram & Pin Configuration

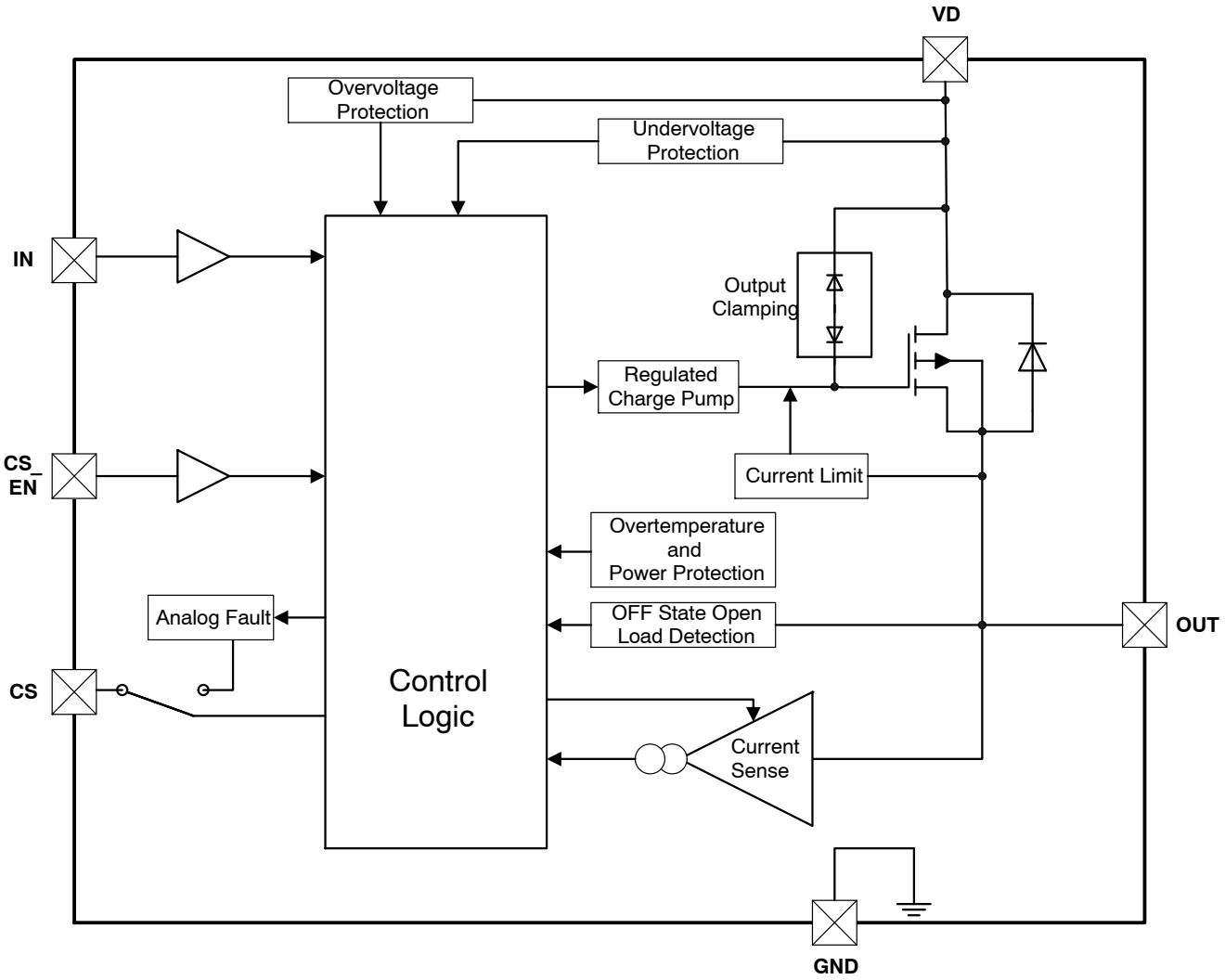


Figure 1. Block Diagram

Table 1. SO8 PACKAGE PIN DESCRIPTION

Pin #	Symbol	Description
1	IN	Logic Level Input
2	CS_EN	Current Sense Enable
3	GND	Ground
4	CS	Analog Current Sense Output
5	V_D	Supply Voltage
6	OUT	Output
7	OUT	Output
8	V_D	Supply Voltage

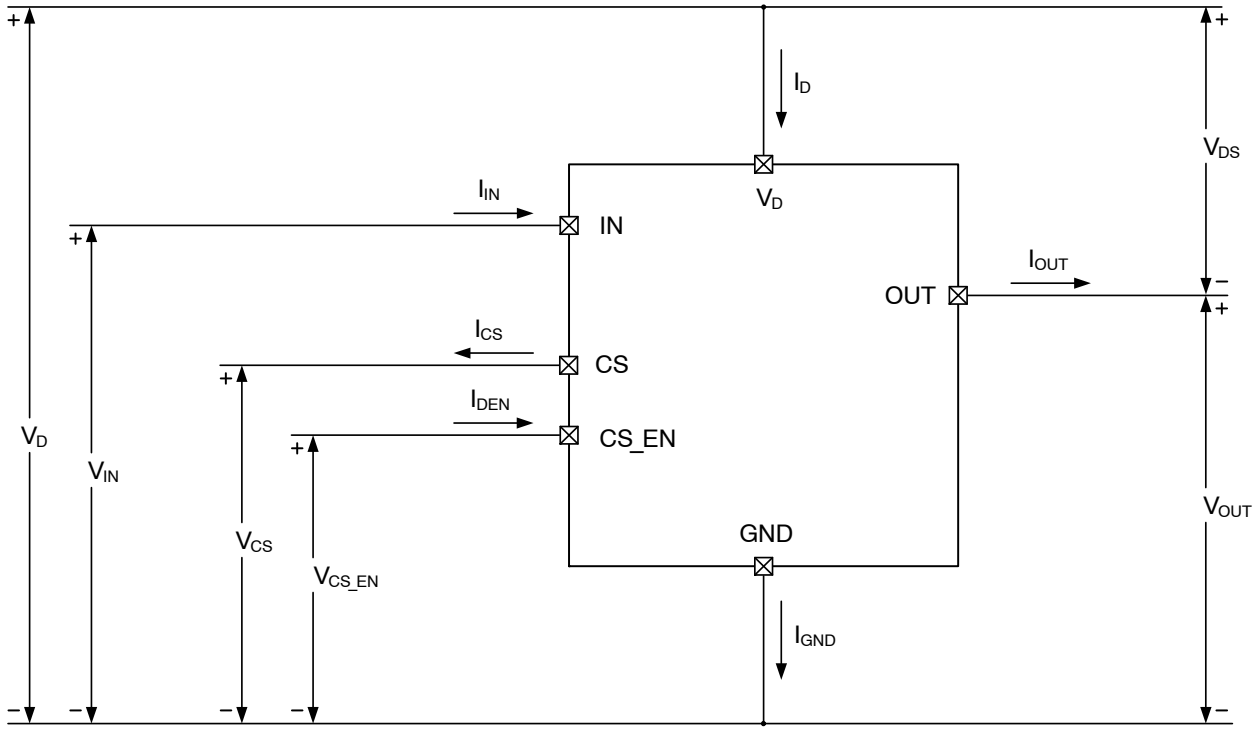


Figure 2. Voltage and Current Conventions

Table 2. Connection suggestions for unused and or unconnected pins

Connection	Input	Output	Current Sense	Current Sense Enable
Floating	X	X	Not Allowed	X
To Ground	Through 10 kΩ resistor	Not Allowed	Through 1 kΩ Resistor	Through 10 kΩ resistor

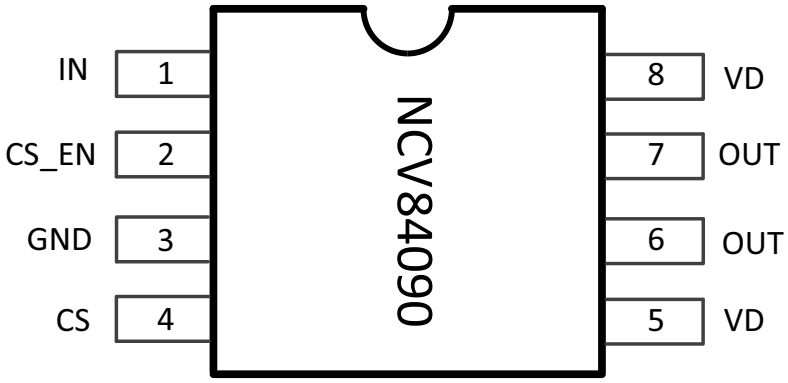


Figure 3. Pin Configuration (top view)

ELECTRICAL SPECIFICATIONS

Table 3. MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		Min	Max	
DC Supply Voltage	V_D	−0.3	41	V
Max Transient Supply Voltage (Note 1) Load Dump Suppresses	V_{PEAK}	−	45	V
Input Voltage	V_{IN}	−10	10	V
Input Current	I_{IN}	−5	5	mA
Reverse Ground Pin Current	I_{GND}	−	−200	mA
Output Current (Note 2)	I_{OUT}	−6	Internally Limited	A
Reverse CS Current (Note 1)	I_{CS}	−	−200	mA
CS Voltage	V_{CS}	V_D−41	V_D	V
CS_EN Voltage	V_{CS_EN}	−10	10	V
CS_EN Current	I_{CS_EN}	−5	5	mA
Power Dissipation Tc = 25°C (Note 6)	P_{tot}	1.95		W
Electrostatic Discharge (Note 3) (HBM Model 100 pF / 1500 Ω) Input Current Sense Current Sense Enable Output V_D Charge Device Model CDM−AEC−Q100−011	V_{ESD}	 4 4 4 4 4 750	− 	DC kV kV kV kV kV V
+Single Pulse Inductive Load Switching Energy (L = 5 mH, Vbat = 13.5 V; I_L = 4.8 A, T_{Jstart} = 150°C (Note 4)	E_{AS}	−	81	mJ
Operating Junction Temperature	T_J	−40	+150	°C
Storage Temperature	$T_{storage}$	−55	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Load Dump Test B (with centralized load dump suppression) according to ISO16750−2 standard. Guaranteed by design. Not tested in production. Passed Class C (or A, B) according to ISO16750−1.
2. Reverse Output current has to be limited by the load to stay within absolute maximum ratings and thermal performance.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JS−001−2017)
   Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes smaller than 2 x 2 mm due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS−002−2018
4. Not subjected to production testing.

Table 4. THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max. Value	Units
Thermal Resistance Junction−to−Lead (Note 5) Junction−to−Ambient (Note 5) Junction−to−Ambient (Note 6)	 R_{thJL} R_{thJA} R_{thJA}	 27.3 50 64	°C / W

5. 645 mm^2 pad size, mounted on four−layer 2s2p PCB − FR4, 2 oz. Cu thickness for top layer and 1 oz. Cu thickness for inner layers (planes not electrically connected)
6. 2 cm^2 pad size, mounted on single−layer 2s0p PCB − FR4, 2 oz. Cu thickness (planes not electrically connected)

ELECTRICAL CHARACTERISTICS ($7 \le V_D \le 28$ V; $-40°C < T_J < 150°C$ unless otherwise specified)
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. POWER

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Operating Supply Voltage	V_D		4	–	28	V
Undervoltage Shutdown	V_{UV}		–	3.5	4	V
Undervoltage Shutdown Hysteresis	V_{UV_hyst}		–	0.4	–	V
On Resistance	R_{ON}	I_{OUT} = 2.5 A, T_J = 25°C	–	90	–	mΩ
		I_{OUT} = 2.5 A, T_J = 150°C	–	–	180	
		I_{OUT} = 2.5 A, V_D = 4.5 V, T_J = 25°C	–	–	144	
Supply Current (Note 7)	I_D	OFF−state: V_D = 13 V, V_{IN} = V_{OUT} = 0 V, T_J = 25°C	–	0.2	0.5	μA
		OFF−state: V_D = 13 V, V_{IN} = V_{OUT} = 0 V, T_J = 85°C (Note 8)	–	0.2	0.5	μA
		OFF−state: V_D = 13 V, V_{IN} = V_{OUT} = 0 V, T_J = 125°C	–	–	3	μA
		ON−state: V_D = 13 V, V_{IN} = 5 V, I_{OUT} = 0 A	–	1.9	3.5	mA
On State Ground Current	$I_{GND(ON)}$	V_D = 13 V, V_{CS_EN} = 5 V V_{IN} = 5 V, I_{OUT} = 1 A	–	–	6	mA
Output Leakage Current	I_L	V_{IN} = V_{OUT} = 0 V, V_D = 13 V, T_J = 25°C	–	–	0.5	μA
		V_{IN} = V_{OUT} = 0 V, V_D = 13 V, T_J = 125°C	–	–	3	

7. Includes PowerMOS leakage current.
8. Not Subject to production testing.

Table 6. LOGIC INPUTS (V_D = 13.5 V; $-40°C \le T_J \le 150°C$)

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Input Voltage − Low	V_{in_low}		–	–	0.9	V
Input Current − Low	I_{in_low}	V_{in} = 0.9 V	1	–	–	μA
Input Voltage − High	V_{in_high}		2.1	–	–	V
Input Current − High	I_{in_high}	V_{in} = 2.1 V	–	–	10	μA
Input Hysteresis Voltage	V_{in_hyst}		–	0.2	–	V
Input Clamp Voltage	V_{in_cl}	I_{in} = 1 mA	12	13	14	V
		I_{in} = −1 mA	−14	−13	−12	
CS_EN Voltage − Low	V_{CSE_low}		–	–	0.9	V
CS_EN Current − Low	I_{CSE_low}	V_{CS_EN} = 0.9 V	1	–	–	μA
CS_EN Voltage − High	V_{CSE_high}		2.1	–	–	V
CS_EN Current − High	I_{CSE_high}	V_{CS_EN} = 2.1 V	–	–	10	μA
CS_EN Hysteresis Voltage	V_{CSE_Hys}		–	0.2	–	V
CS_EN Clamp Voltage	V_{CSE_cl}	I_{CS_EN} = 1 mA	12	13	14	V
		I_{CS_EN} = −1 mA	−14	−13	−12	

Table 7. SWITCHING CHARACTERISTICS (Note 11) (V_D = 13. V, −40°C < T_J < 150°C)

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Turn−On Delay Time	t_{d_on}	V_{in} high to 20% Vout, V_D = 13 V, R_L = 6.5 Ω, T_J = 25°C	5	70	120	μs
Turn−Off Delay Time	t_{d_off}	V_{in} low to 80% Vout, V_D = 13 V, R_L = 6.5 Ω, T_J = 25°C	5	40	100	μs
Slew Rate On	dV_{out}/dt_{on}	20% to 80% Vout, V_D = 13 V, R_L = 6.5 Ω, T_J = 25°C	0.1	0.27	0.7	V / μs
Slew Rate Off	dV_{out}/dt_{off}	80% to 20% Vout, V_D = 13 V, R_L = 6.5 Ω, T_J = 25°C	0.1	0.35	0.7	V / μs
Turn−On Switching Loss (Note 9)	E_{on}	V_D = 13 V, R_L = 6.5 Ω	–	0.15	0.22	mJ
Turn−Off Switching Loss (Note 9)	E_{off}	V_D = 13 V, R_L = 6.5 Ω	–	0.15	0.22	mJ
Differential Pulse Skew, (t_{OFF} − t_{ON}) see Figure 4	t_{skew}	V_D = 13 V, R_L = 6.5 Ω	−50	–	50	μs

9. Not subjected to production testing.

Table 8. OUTPUT DIODE CHARACTERISTICS

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Forward Voltage	V_F	I_{out} = −1 A, V_F = V_{OUT} −VD, T_J = 150°C	–	–	0.7	V

Table 9. PROTECTION FUNCTIONS (Note 10) (7 ≤ V_D ≤ 18 V, −40°C < T_J < 150°C)

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Temperature Shutdown (Note 11)	T_{SD}		150	175	200	°C
Temperature Shutdown Hysteresis (Note 11)	T_{SD_hyst}		–	7	–	°C
Reset Temperature (Note 11)	T_R		T_{RS}+1	T_{RS}+7	–	°C
Thermal Reset of Status (Note 11)	T_{RS}		135	–	–	°C
Delta T Temperature Limit (Note 11)	T_{DELTA}	T_J = −40°C, V_D = 13 V	–	60	–	°C
DC Output Current Limit	I_{limH}	V_D = 13 V	16	24	32	A
		4 V < V_D < 18 V	–	–	32	A
Short Circuit Current Limit during Thermal Cycling (Note 11)	$I_{limTCycling}$	V_D = 13 V T_R < Tj < T_{TSD}	–	8	–	A
Switch Off Output Clamp Voltage	V_{out_clamp}	I_{out} = 0.5 A, V_{in} = 0 V, L = 20 mH	V_D − 41	V_D − 46	V_D − 52	V
Overvoltage Protection	V_{OV}	V_{in} = 0 V, I_D = 20 mA	41	46	52	V
Output Voltage Drop Limitation	V_{DS_ON}	I_{out} = 0.2 A, T_J = −40°C to 150°C	–	20	–	mV

10. To ensure long term reliability during overload or short circuit conditions, protection and related diagnostic signals must be used together with a fitting hardware & software strategy. If the device operates under abnormal conditions, this hardware & software solution must limit the duration and number of activation cycles.
11. Not subjected to production testing.

Table 10. OPEN−LOAD DETECTION ($7 \le V_D \le 18$ V, $-40°C < T_J < 150°C$)

Rating	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Open−load Off State Detection Threshold	V_{OL}	V_{in} = 0 V, V_{CS_EN} = 5 V	2	–	4	V
Open−load Detection Delay at Turn Off	$t_{d\_OL\_off}$		100	350	850	μs
Off State Output Current	I_{OLOFF1}	V_{in} = 0 V, V_{OUT} = V_{OL}	−3	–	3	μA
Output rising edge to CS rising edge during open load	t_{d_OL}	V_{OUT} = 4 V, V_{in} = 0 V V_{CS} = 90% of V_{CS_High}	–	5	30	μs

Table 11. CURRENT SENSE CHARACTERISTICS ($7 \le V_D \le 18$ V, $-40°C < T_J < 150°C$)

Rating	Symbol	Conditions	Value			Unit
			min	typ	max	
Current Sense Ratio	K_0	I_{out} = 0.01 A, V_{CS} = 0.5 V, V_{CS_EN} = 5 V	435	–	1250	
Current Sense Ratio	K_1	I_{out} = 0.025 A, V_{CS} = 0.5 V, V_{CS_EN} = 5 V	400	800	1200	
Current Sense Ratio Drift (Note 13)	$\Delta K_1 / K_1$	I_{out} = 0.025 A, V_{CS_EN} = 5 V	−20	–	15	%
Current Sense Ratio	K_2	I_{out} = 0.35 A, V_{CS} = 4V, V_{CS_EN} = 5 V	450	750	1000	
Current Sense Ratio Drift (Note 13)	$\Delta K_2 / K_2$	I_{out} = 0.35 A, V_{CS_EN} = 5 V	−15	–	15	%
Current Sense Ratio	K_3	I_{out} = 0.5 A, V_{CS} = 4 V, V_{CS_EN} = 5 V	530	750	950	
Current Sense Ratio Drift (Note 13)	$\Delta K_3 / K_3$	I_{out} = 0.5 A, V_{CS_EN} = 5 V	−15	–	10	%
Current Sense Ratio	K_4	I_{out} = 1 A, V_{CS} = 4 V, V_{CS_EN} = 5 V	625	750	835	
Current Sense Ratio Drift (Note 13)	$\Delta K_4 / K_4$	I_{out} = 1 A, V_{CS_EN} = 5 V	−10	–	10	%
Current Sense Ratio	K_5	I_{out} = 3 A, V_{CS} = 4 V, V_{CS_EN} = 5 V	690	750	775	
Current Sense Ratio Drift (Note 13)	$\Delta K_5 / K_5$	I_{out} = 3 A, V_{CS_EN} = 5 V	−5	–	5	%
Current Sense Leakage Current	CS_{llkg}	I_{out} = 0 A, V_{CS} = 0 V V_{CS_EN} = 5 V, V_{IN} = 0 V	–	–	1	μA
		I_{out} = 0 A, V_{CS} = 0 V V_{CS_EN} = 5 V, V_{IN} = 5 V	–	–	2	
		I_{out} = 2 A, V_{CS} = 0 V V_{CS_EN} = 0 V, V_{IN} = 5 V,	–	–	0.5	
CS Max Voltage	CS_{Max}	V_D = 7 V, V_{IN} = 5 V, R_{CS} = 15 kΩ, I_{OUT} = 2 A, V_{CS_EN} = 5 V	5	–	7	V
Current Sense Voltage in Fault Condition (Note 12)	V_{CS_fault}	V_D = 13 V, V_{IN} = 0 V, R_{CS} = 1 kΩ, V_{OUT} = 4 V, V_{CS_EN} = 5 V	–	10	–	V
Current Sense Current in Fault Condition (Note 12)	I_{CS_fault}	V_D = 13 V, V_{CS} = 5 V, V_{IN} = 0 V, V_{OUT} = 4 V, V_{CS_EN} = 5 V	7	20	30	mA
Output Saturation Current (Note 13)	I_{OUT_sat}	V_D = 7 V, V_{CS}= 4 V, V_{IN} = 5 V, T_J = 150°C, V_{CS_EN} = 5 V	3	–	–	A
CS_EN High to CS High Delay Time	t_{CS_High1}	V_{IN} = 5 V, V_{CS_EN} = 0 to 5 V, R_{CS} = 1 kΩ, R_L = 6.5 Ω	–	–	100	μs
CS_EN Low to CS Low Delay Time	t_{CS_Low1}	V_{IN} = 5 V, V_{CS_EN} = 5 to 0 V, R_{CS} = 1 kΩ, R_L = 6.5 Ω	–	5	25	μs
V_{in} High to CS High Delay Time	t_{CS_High2}	V_{IN} = 0 to 5 V, V_{CS_EN} = 5 V, R_{CS} = 1 kΩ, R_L = 6.5 Ω	–	100	250	μs
V_{in} Low to CS Low Delay Time	t_{CS_Low2}	V_{IN} = 5 to 0 V, V_{CS_EN} = 5 V, R_{CS} = 1 kΩ, R_L = 6.5 Ω	–	50	250	μs
Delay Time I_D Rising Edge to Rising Edge of CS	Δt_{CS_High2}	V_{IN} = 5 V, V_{CS_EN} = 5 V R_{CS} = 1 kΩ, I_{CS} = 90% of I_{CS} Max	–	–	100	μs

12. The following fault conditions are: Overtemperature, Power Limitation, and OFF State Open−Load Detection.
13. Not subjected to production testing. For more information, refer to the AND9733−D Applications Note.

Table 12. TRUTH TABLE

Conditions	Input	Output	CS (V_{CS_EN} = 5V) (Note 14)
Normal Operation	L H	L H	0 $I_{CS} = I_{OUT}/K_{NOMINAL}$
Overtemperature	L H	L L	0 V_{CS_High}
Undervoltage	L H	L L	0 0
Overload	H H	H (no active current mgmt) Cycling (active current mgmt)	$I_{CS} = I_{OUT}/K_{NOMINAL}$ V_{CS_High}
Short circuit to Ground	L H	L L	0 V_{CS_High}
OFF State Open Load	L	H	V_{CS_High}

14. If V_{CS_EN} is low, the Current Sense output is at a high impedance, its potential depends on leakage currents and external circuitry.

WAVEFORMS AND GRAPHS

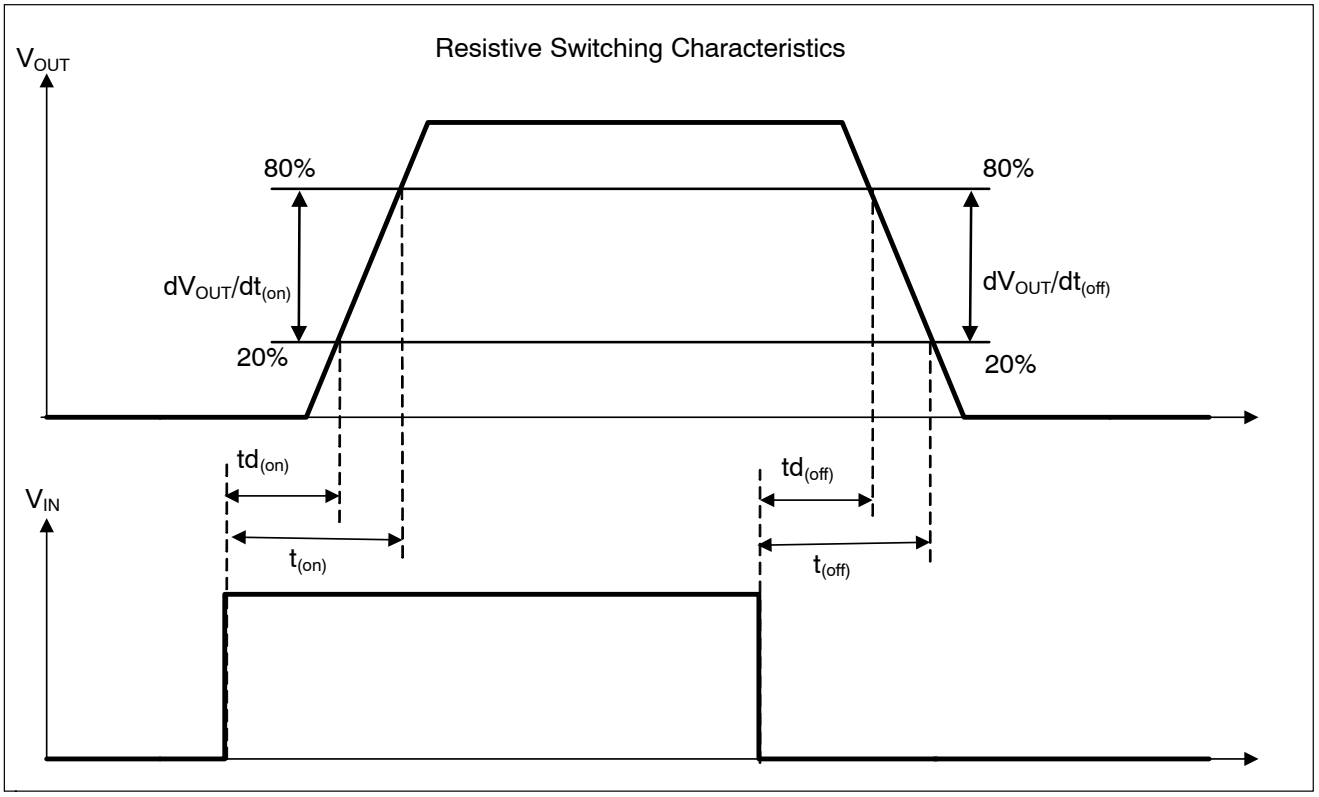


Figure 4. Switching Characteristics

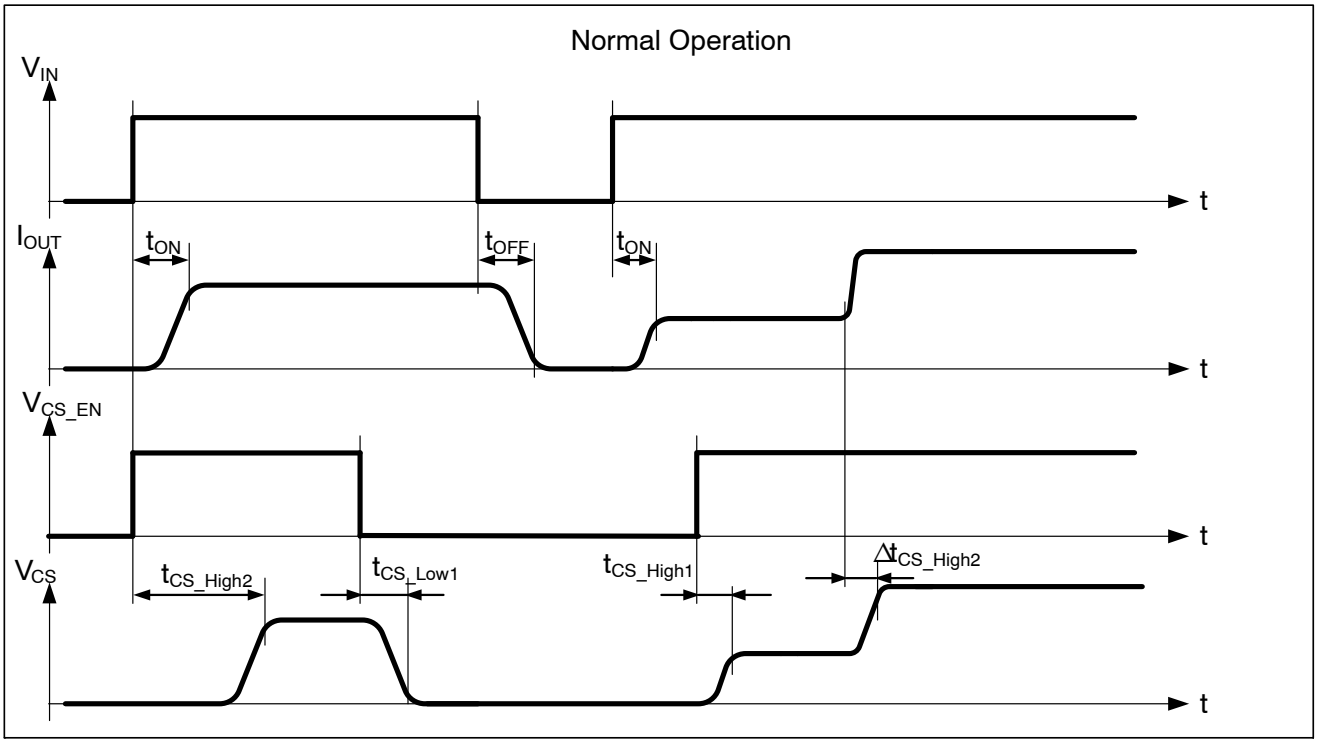


Figure 5. Normal Operation with Current Sense Timing Characteristics

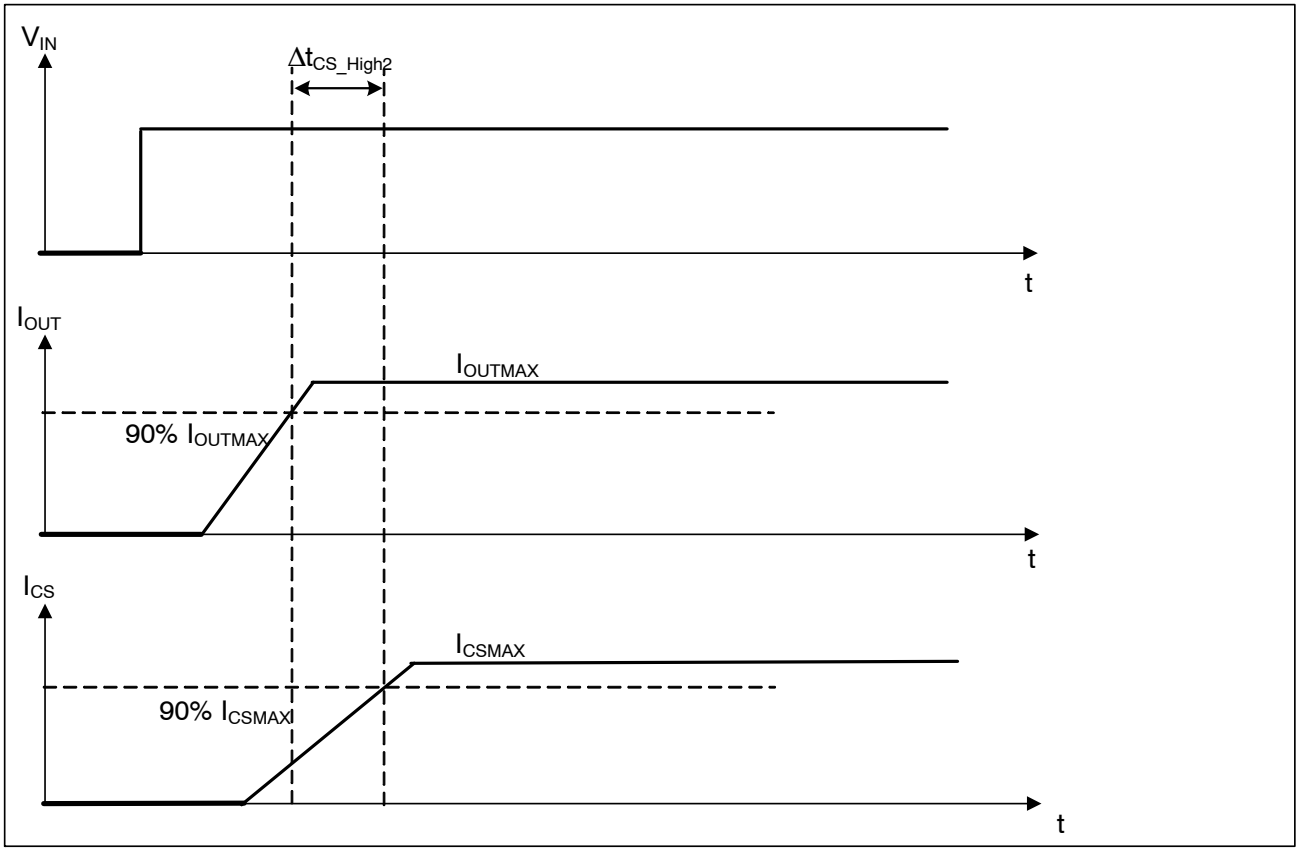


Figure 6. Delay Response from rising edge of IOUT and rising edge of CS (for CS_EN = 5V)

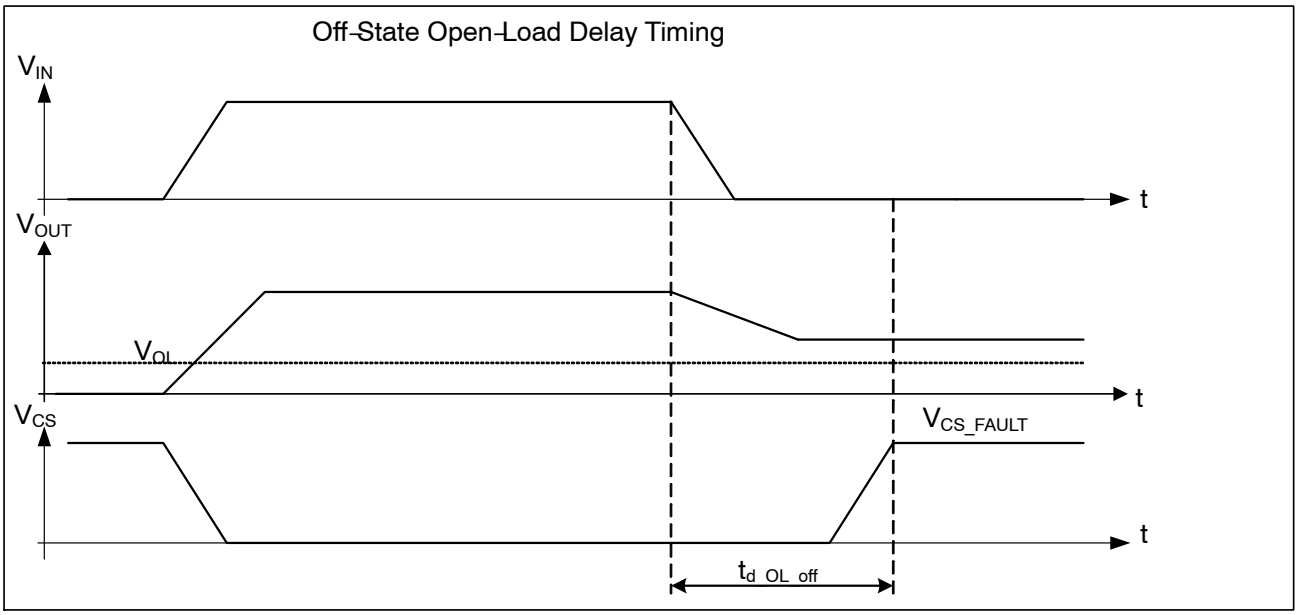


Figure 7. OFF−State Open−Load Flag Delay Timing

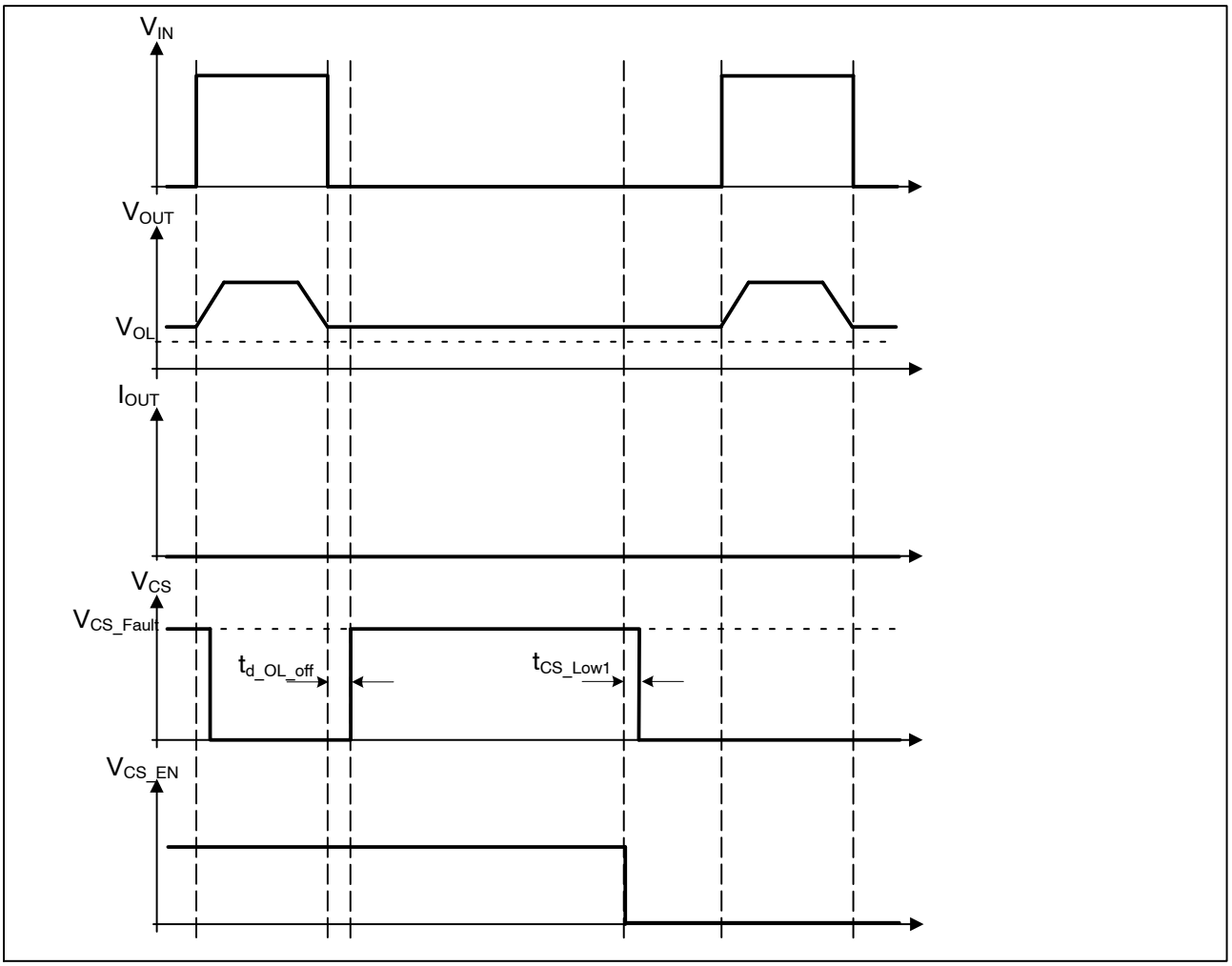


Figure 8. Off−State Open−Load with added external components

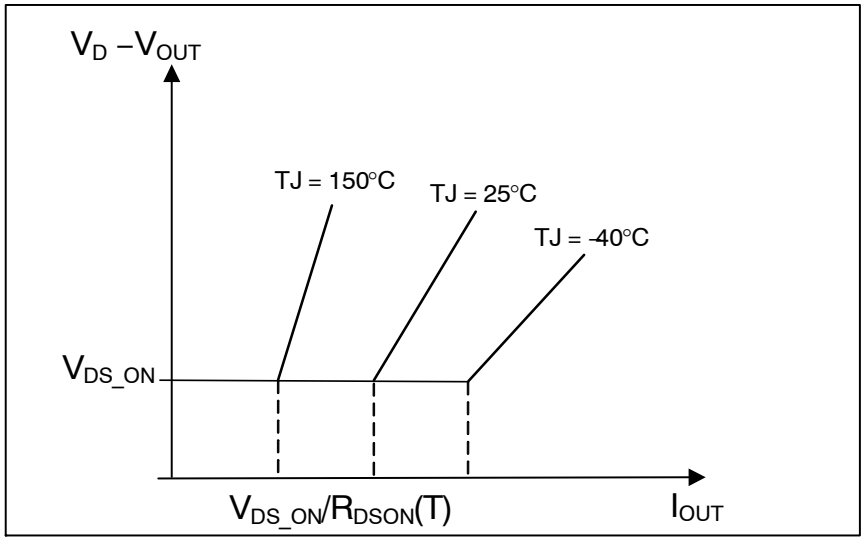


Figure 9. Voltage Drop Limitation for VDS_ON

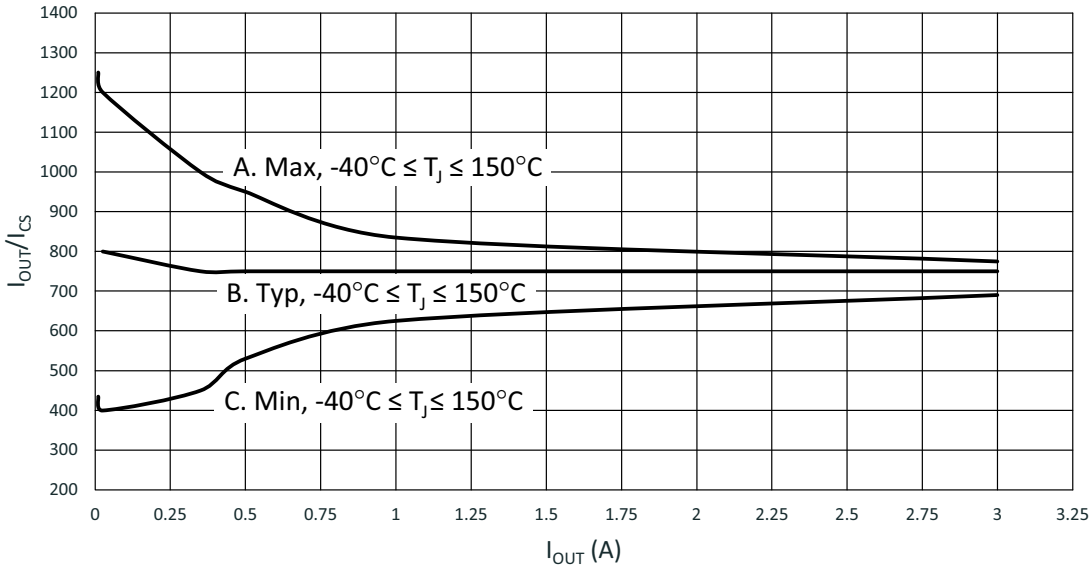


Figure 10. I_{OUT}/I_{CS} vs. I_{OUT}

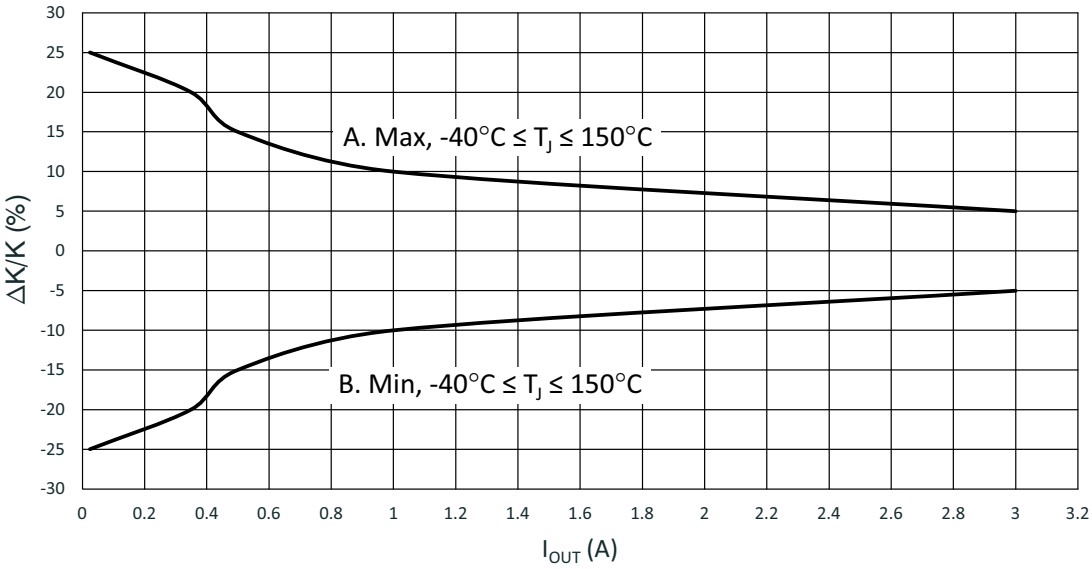


Figure 11. Current Sense Ratio Drift vs. Load Current

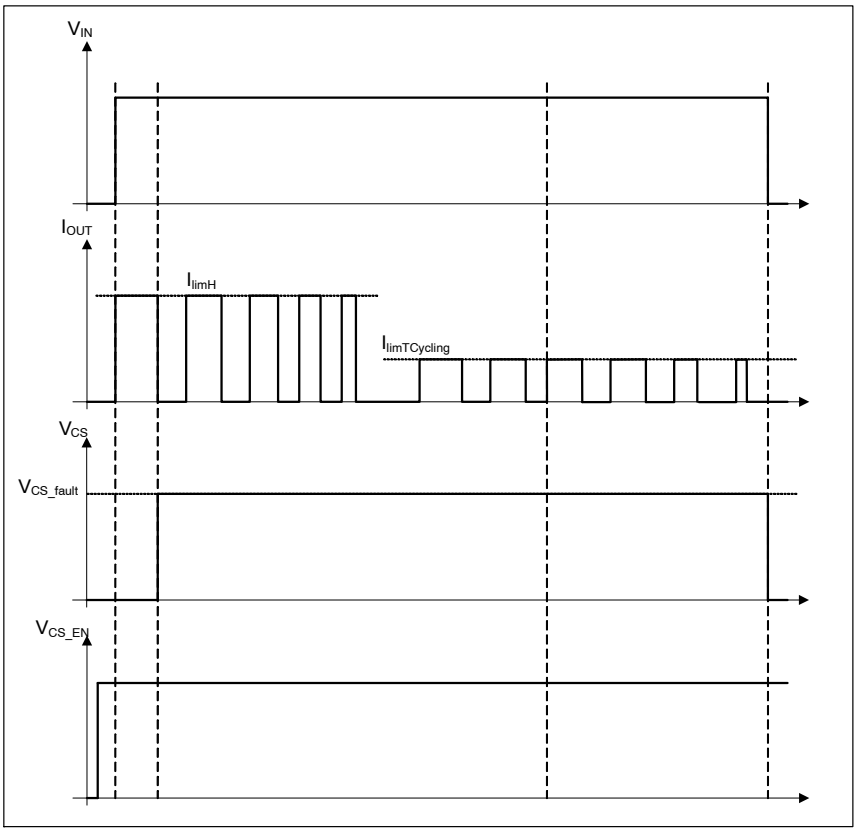


Figure 12. Short to GND or Overload

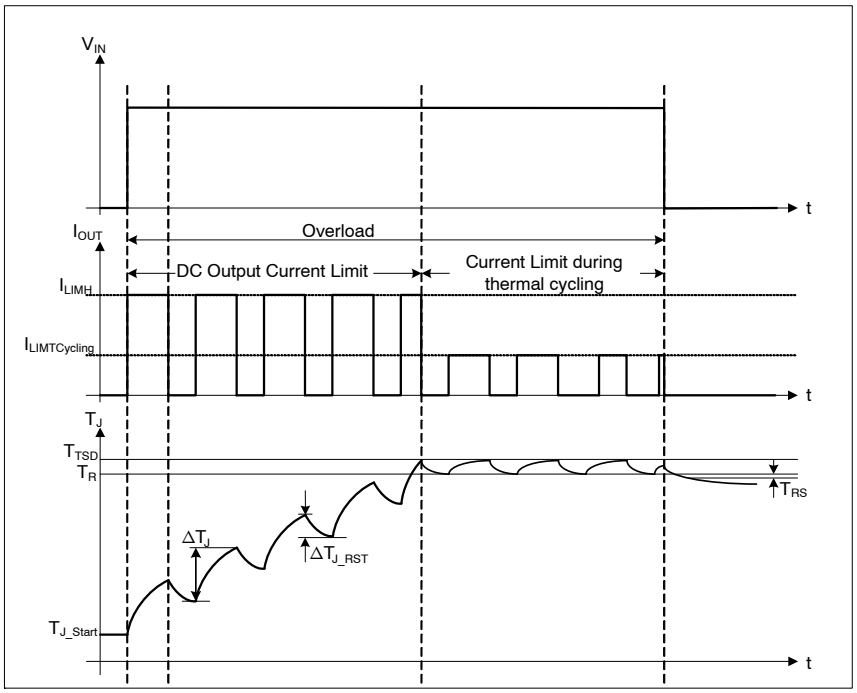


Figure 13. How T_J progresses during Short to GND or Overload

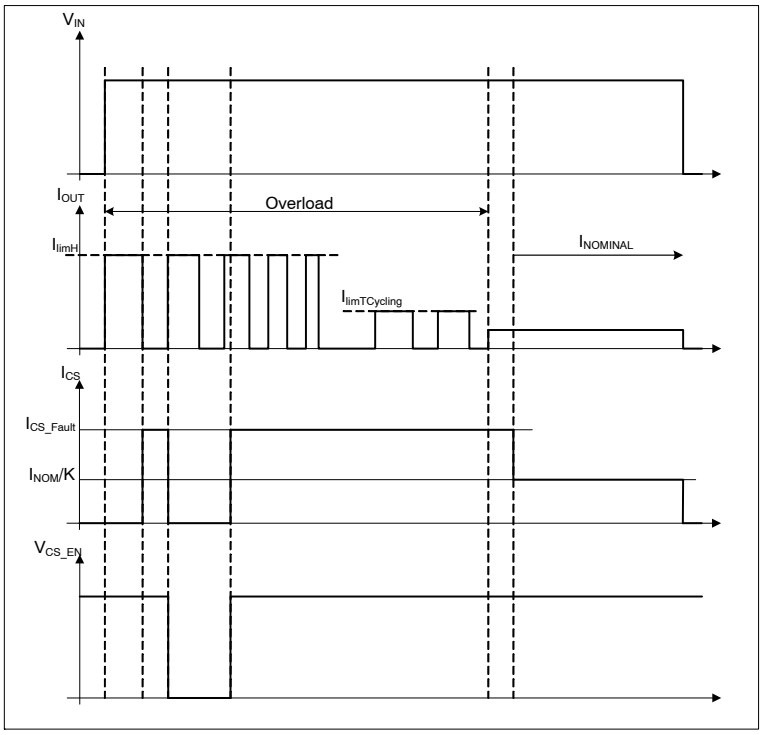


Figure 14. Discontinuous Overload or Short to GND

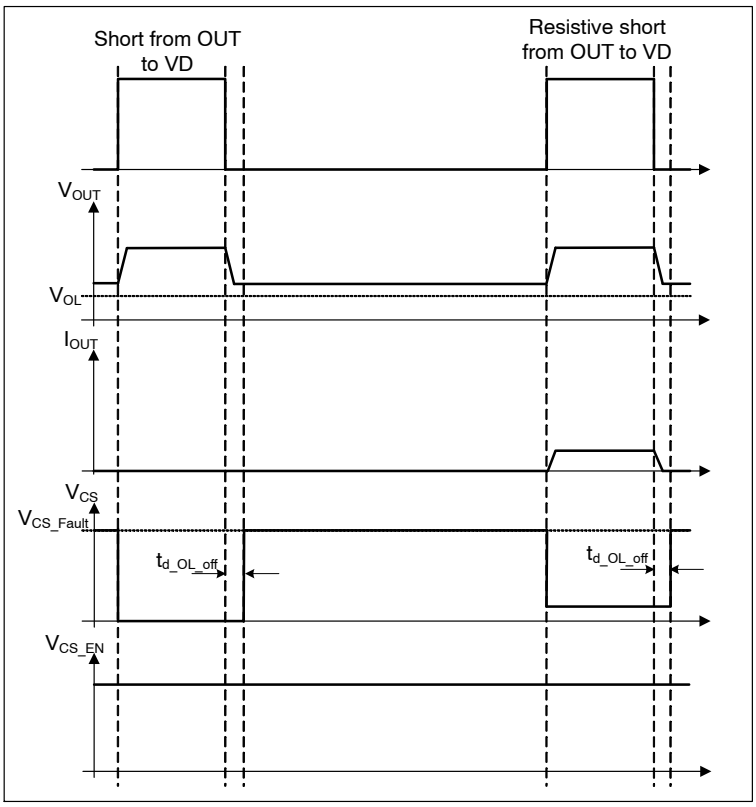


Figure 15. Short Circuit from OUT to VD

TYPICAL CHARACTERISTICS

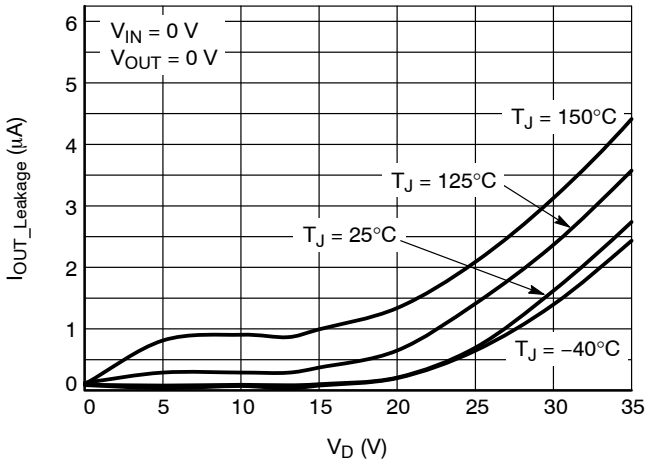


Figure 16. Output Leakage Current vs. V_D

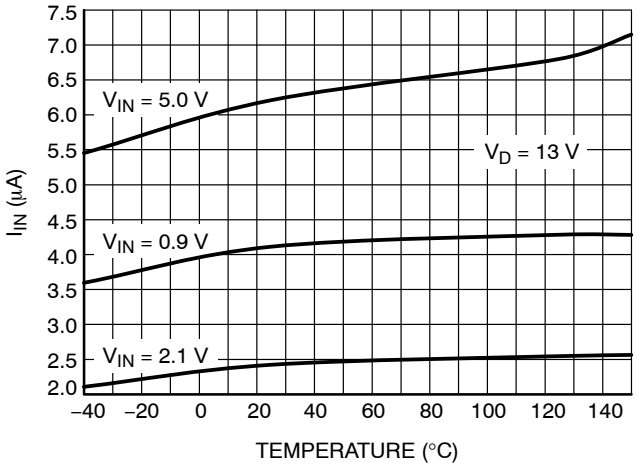


Figure 17. Input Current vs. Temperature

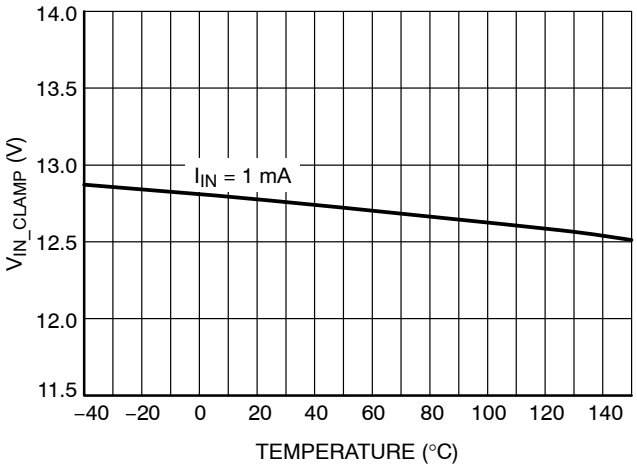


Figure 18. Input Clamp Voltage (Positive) vs. Temperature

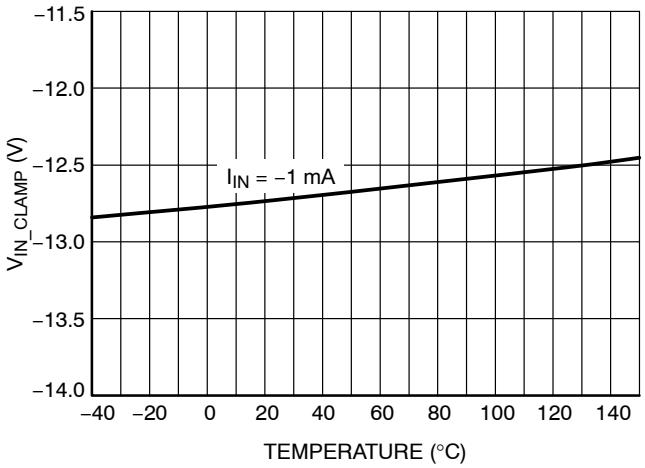


Figure 19. Input Clamp Voltage (Negative) vs. Temperature

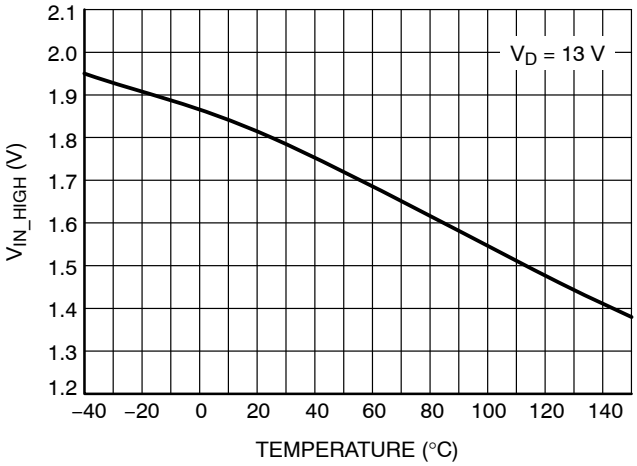


Figure 20. V_{IN} Threshold High vs. Temperature

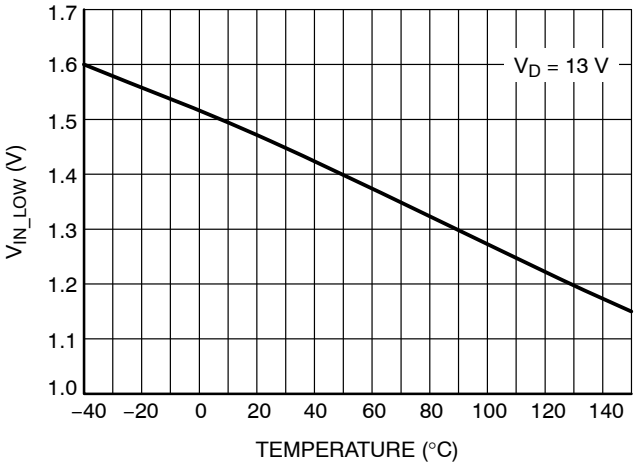


Figure 21. V_{IN} Threshold Low vs. Temperature

TYPICAL CHARACTERISTICS

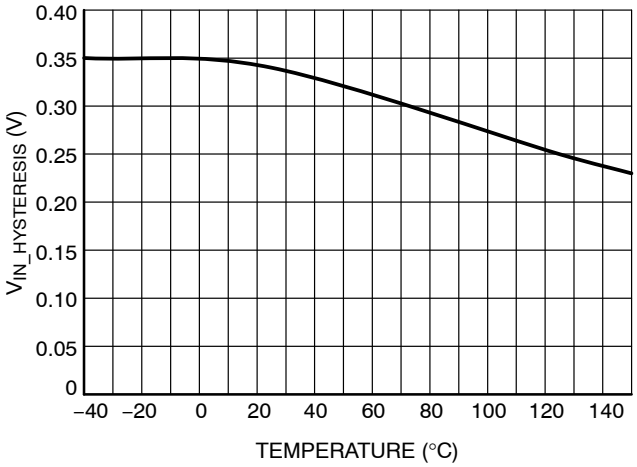


Figure 22. Hysteresis Input Voltage vs. Temperature

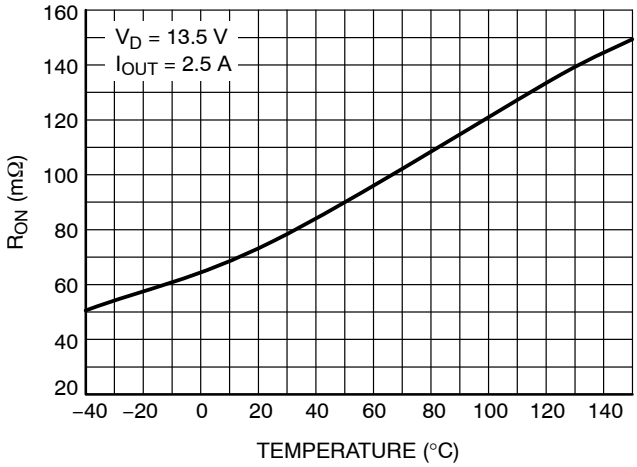


Figure 23. R_{ON} vs. Temperature

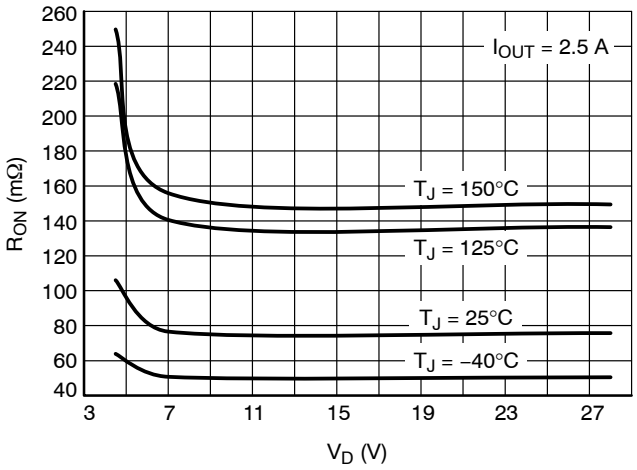


Figure 24. R_{ON} vs. V_D Voltage

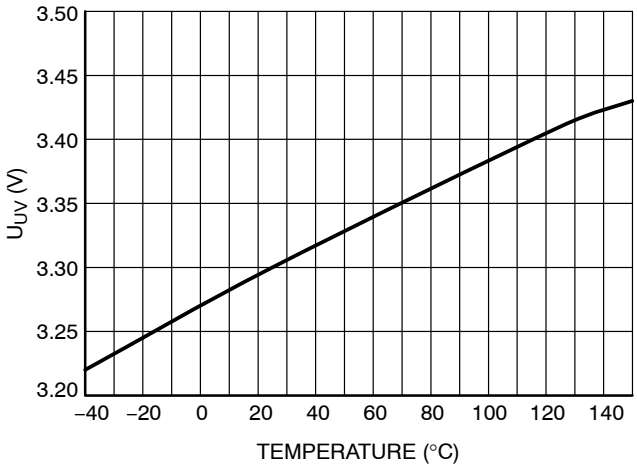


Figure 25. Undervoltage Shutdown vs. Temperature

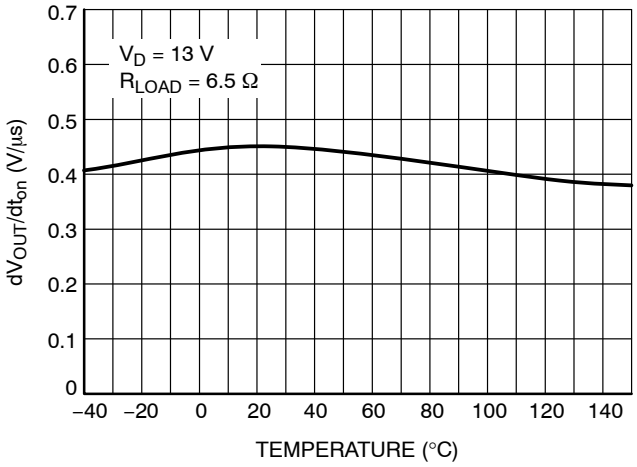


Figure 26. Slew Rate ON vs. Temperature

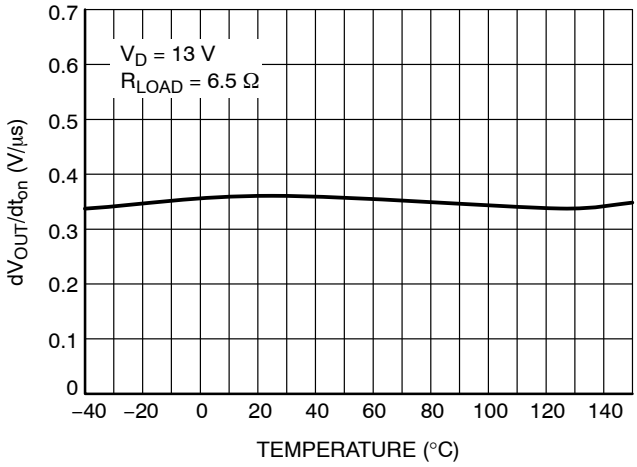


Figure 27. Slew Rate OFF vs. Temperature

TYPICAL CHARACTERISTICS

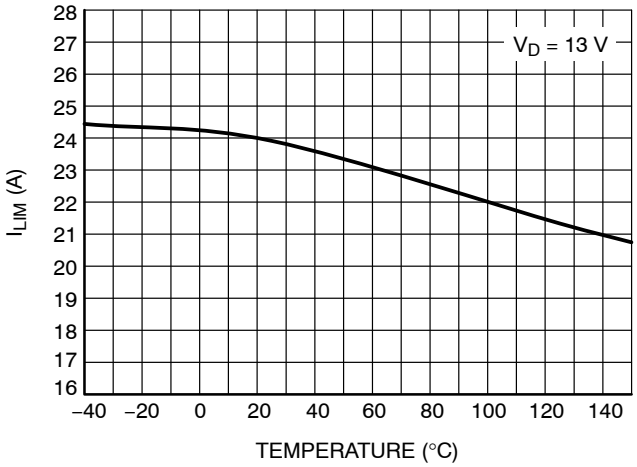


Figure 28. Current Limit vs. Temperature

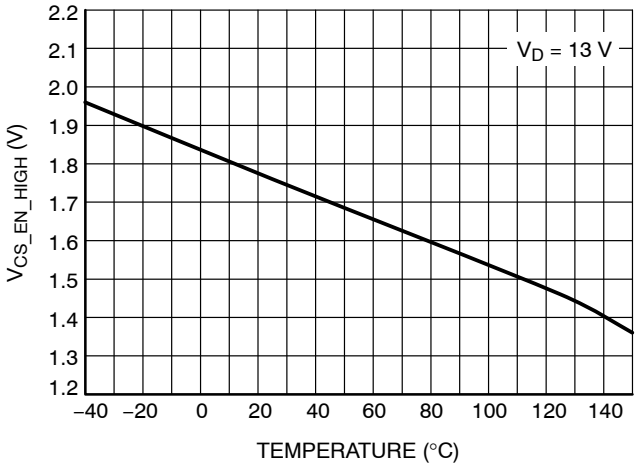


Figure 29. CS_EN Threshold High vs. Temperature

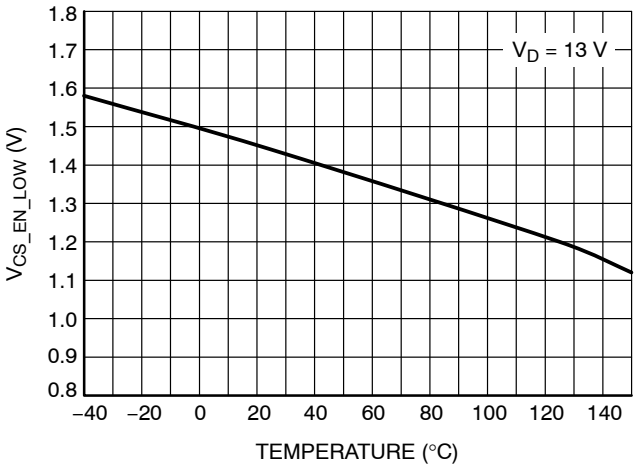


Figure 30. CS_EN Threshold Low vs. Temperature

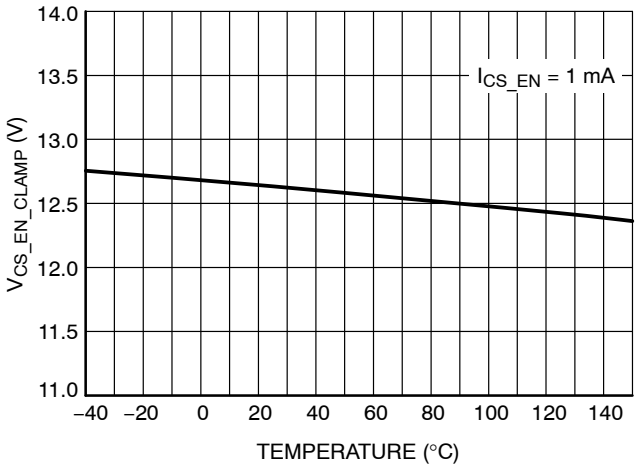


Figure 31. CS_EN Clamp Voltage (Positive) vs. Temperature

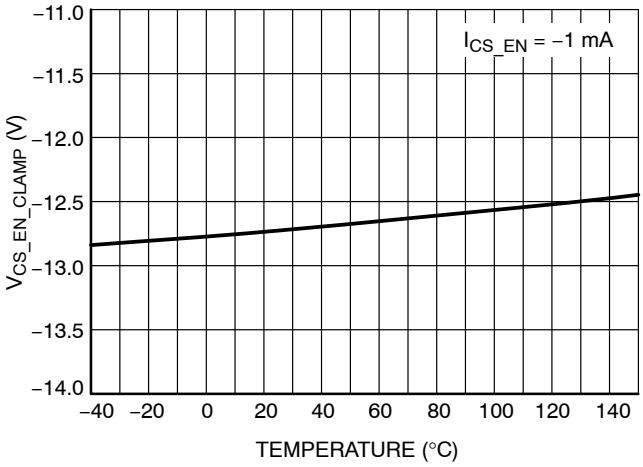


Figure 32. CS_EN Clamp Voltage (Negative) vs. Temperature

Table 13. ISO 7637−2: 2011(E) PULSE TEST RESULTS

ISO 7637−2:2011 Test Pulse	Test Severity Levels		Delays and Impedance	# of Pulses or Test Time	Pulse / Burst Rep. Time
	III	IV			
1	−112	−150	2 ms, 10 Ω	500 pulses	0.5 s
2a	55	112	0.05 ms, 2 Ω	500 pulses	0.5 s
3a	−165	−220	0.1 μs, 50 Ω	1 h	100 ms
3b	112	150	0.1 μs, 50 Ω	1 h	100 ms

ISO 7637−2:2011 Test Pulse	Test Results				
	III	IV			
1		**A**			
2a		**C**			
3a		**A**			
3b		**A**			

Class	Functional Status
A	All functions of a device perform as designed during and after exposure to disturbance.
B	All functions of a device perform as designed during exposure. However, one or more of them can go beyond specified tolerance. All functions return automatically to within normal limits after exposure is removed. Memory functions shall remain class A.
C	One or more functions of a device do not perform as designed during exposure but return automatically to normal operation after exposure is removed.
D	One or more functions of a device do not perform as designed during exposure and do not return to normal operation until exposure is removed and the device is reset by simple “operator/use” action.
E	One or more functions of a device do not perform as designed during and after exposure and cannot be returned to proper operation without replacing the device.

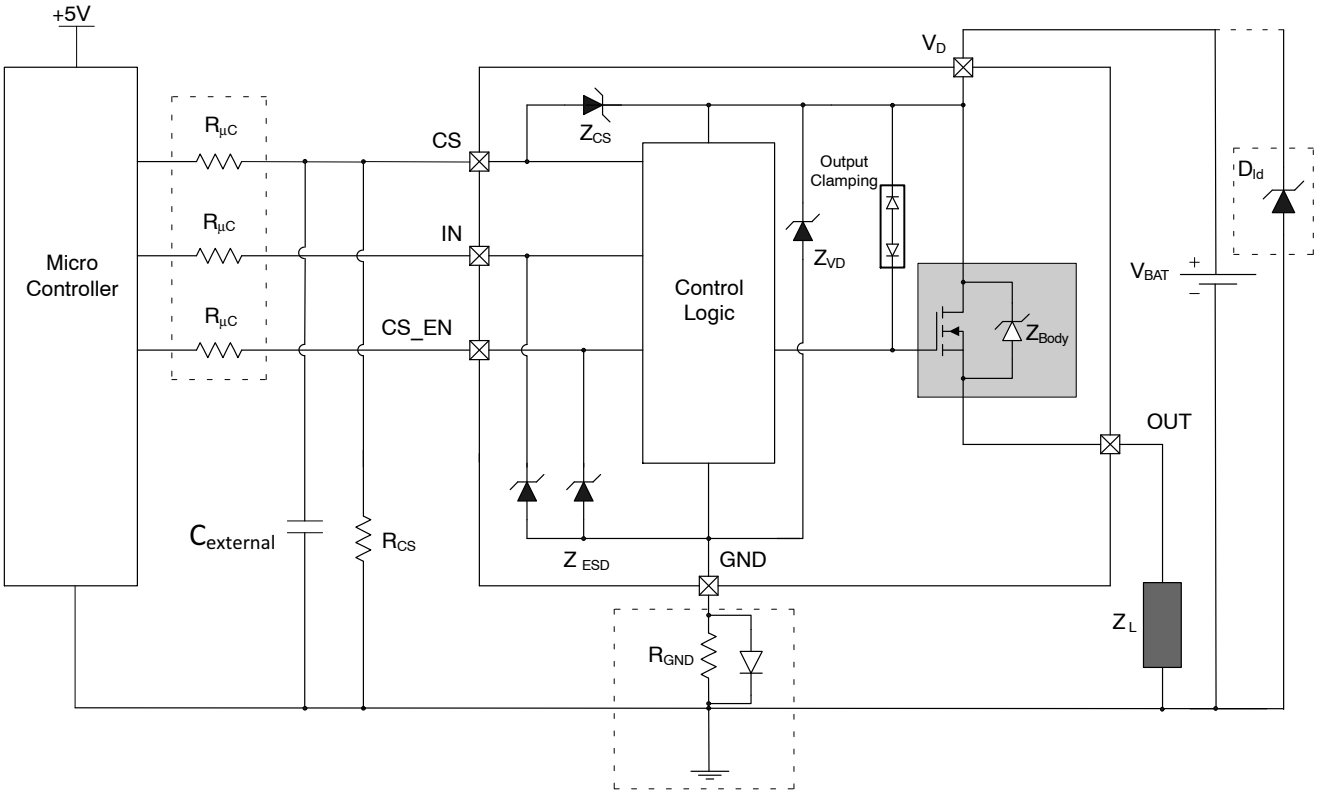


Figure 33. Application Schematic

Protection Features

In application, the device can be subject to stressful conditions which are outside of normal operating range. To prevent damage and destruction of the device from these fault conditions, several protection functions are integrated in device design. It is important to diagnose and remove any fault condition that may exist since the protection functions cannot prevent damage for continuous and repetitive faulty operation.

Loss of Ground Protection

When device or ECU ground connection is lost and load is still connected to ground, the device will turn the output OFF. In loss of ground state, the output stage is held OFF independent of the state of the input. Input resistors are recommended between the device and microcontroller.

Undervoltage Protection

The device has two under−voltage threshold levels, V_{D_MIN} and V_{UV}. Switching function (ON/OFF) requires supply voltage to be at least V_{D_MIN}. The device features a lower supply threshold V_{UV}, above which the output can remain in ON state. While all protection functions are guaranteed when the switch is ON, diagnostic functions are operational only within nominal supply voltage range V_D.

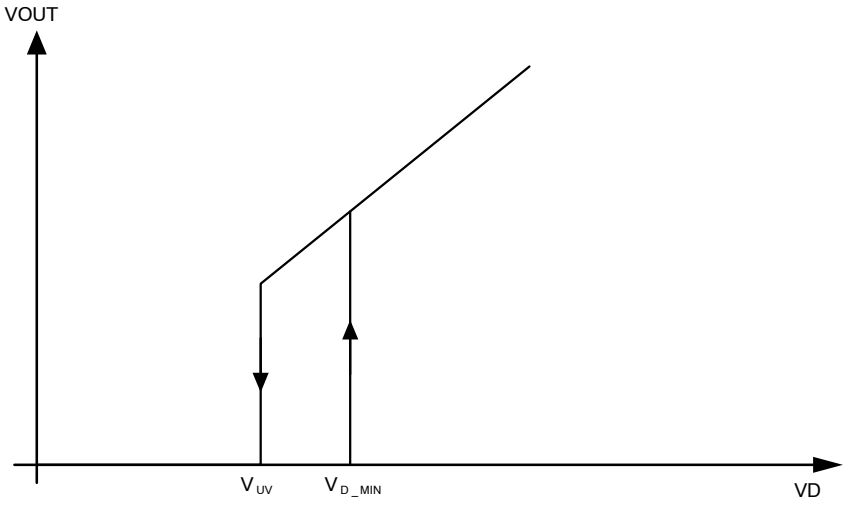


Figure 34. Undervoltage Behavior

Overvoltage Protection:

The NCV84090 has two Zener diodes Z_{VD} and Z_{CS}, which provide integrated overvoltage protection. Z_{VD} protects the logic block by clamping the voltage between supply pin V_D and ground pin GND to V_{ZVD}. Z_{CS} limits voltage at current sense pin CS to $V_D - V_{ZCS}$. The output power MOSFET's output clamping diodes provide protection by clamping the voltage across the MOSFET (between V_D pin and OUT pin) to V_{CLAMP}. During overvoltage protection, current flowing through Z_{VD}, Z_{CS} and the output clamp must be limited. Load impedance Z_L limits the current in the body diode Z_{Body}. In order to limit the current in Z_{VD} a resistor, R_{GND} (150 Ω), is required in the GND path. External resistors R_{CS} and R_{SENSE} limit the current flowing through Z_{CS} and out of the CS pin into the micro−controller I/O pin. With RGND, the GND pin voltage is elevated to $V_D - V_{ZVD}$ when the supply voltage V_D rises above V_{ZVD}. ESD diodes Z_{ESD} pull up the voltage at logic pins IN, CS_EN close to the GND pin voltage $V_D - V_{ZVD}$. External resistors R_{IN}, and R_{CS_EN} are required to limit the current flowing out of the logic pins into the micro−controller I/O pins. During overvoltage exposure, the device transitions into a self−protection state, with automatic recovery after the supply voltage comes back to the normal operating range. The specified parameters as well as short circuit robustness and energy capability cannot be guaranteed during overvoltage exposure.

Reverse Battery Protection

Solution 1: Resistor in the GND line only (no parallel Diode)

The following calculations are true for any type of load.

In the case for no diode in parallel with R_{GND}, the calculations below explain how to size the resistor.

Consider the following parameters:

$-I_{GND}$ Maximum = 200 mA for up to $-V_D$ = 32 V.

Where $-I_{GND}$ is the DC reverse current through the GND pin and $-V_D$ is the DC reverse battery voltage.

$$-I_{GND} = \frac{-V_D}{R_{GND}} \qquad \text{(eq. 1)}$$

Since this resistor can be used amongst multiple High−Side devices, please take note the sum of the maximum active GND currents ($I_{GND(On)max}$) for each device when sizing the resistor. Please note that if the microprocessor GND is not shared by the device GND, then R_{GND} produces a shift of ($I_{GND(On)max} \times R_{GND}$) in the input thresholds and CS output values. If the calculated power dissipation leads to too large of a resistor size or several devices have to share the same resistor, please look at the second solution for Reverse Battery Protection. Refer to Figure 35 for selecting the proper R_{GND}.

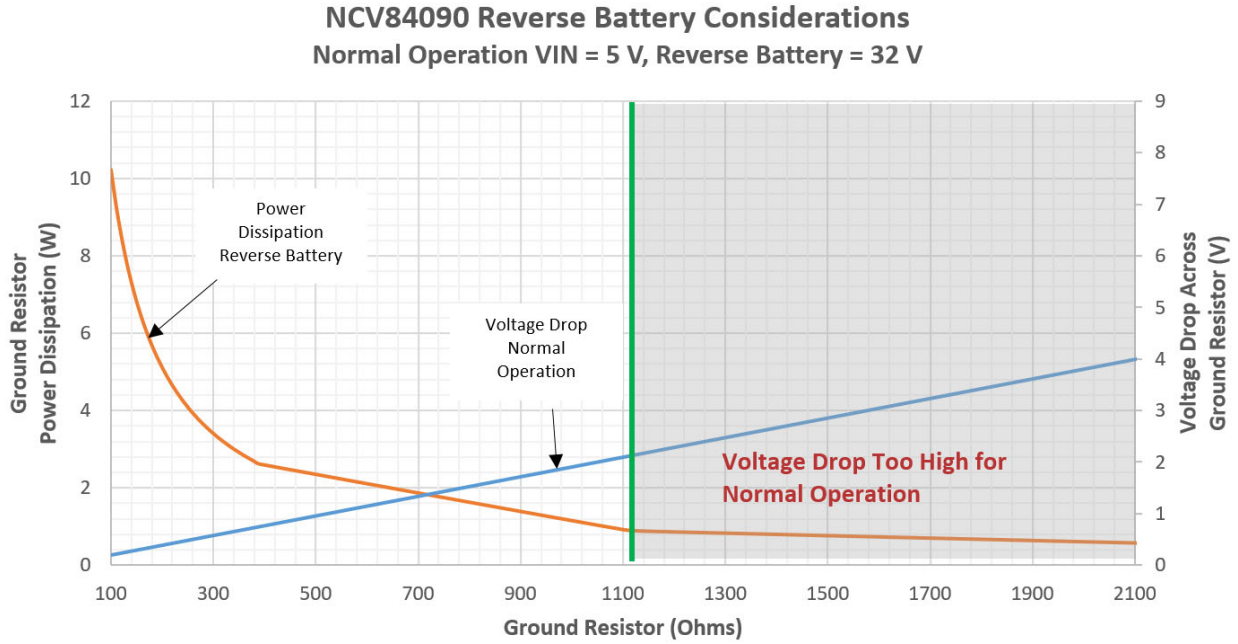


Figure 35. Reverse Battery R_{GND} Considerations

Overload Protection

Current limitation as well as overtemperature shutdown mechanisms are integrated into NCV84090 to provide protection from overload conditions such as bulb inrush or short to ground.

Current Limitation

In case of overload, NCV84090 limits the current in the output power MOSFET to a safe value. Due to high power dissipation during current limitation, the device's junction temperature increases rapidly. In order to protect the device, the output driver is shut down by one of the two overtemperature protection mechanisms. The output current limit is dependent on the device temperature, and will fold back once the die reaches thermal shutdown. If the input remains active during the shutdown, the output power MOSFET will automatically be re−activated after a minimum OFF time or when the junction temperature returns to a safe level.

Output Clamping with Inductive Load Switch Off:

The output voltage V_{OUT} drops below GND potential when switching off inductive loads. This is because the inductance develops a negative voltage across the load in response to a decaying current. The integrated clamp of the device clamps the negative output voltage to a certain level relative to the supply voltage V_{BAT}. During output clamping with inductive load switch off, the energy stored in the inductance rapidly dissipated in the device resulting in high power dissipation. This is a stressful condition for the device and the maximum energy allowed for a given load inductance should not be exceeded in any application.

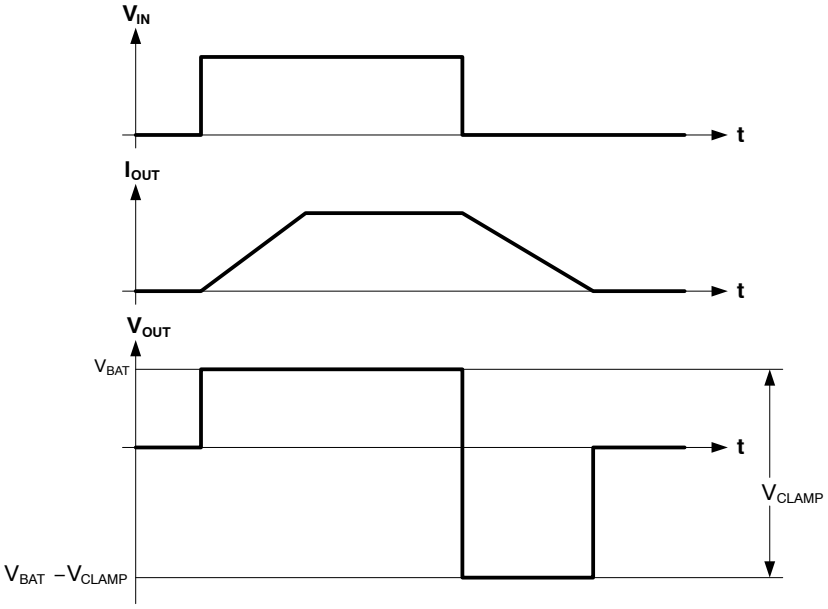


Figure 36. Inductive Load Switching

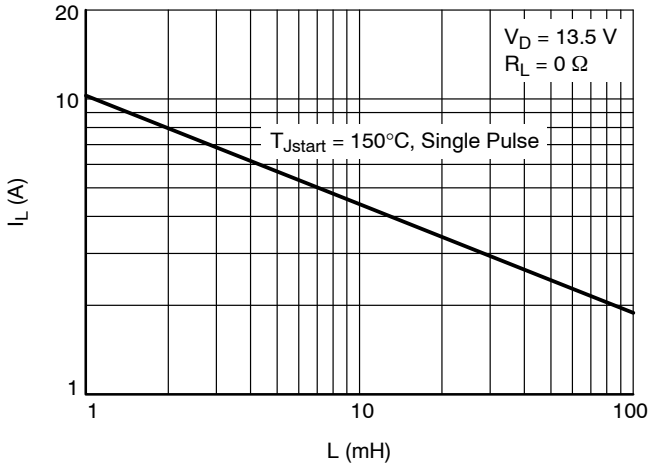


Figure 37. Maximum Switch−Off Current vs. Load Inductance, V_D = 13.5 V; R_L = 0 Ω

Inverse Current:

When the output voltage V_{OUT} rises above the supply voltage V_D, the output power MOSFET's integral body diode will be forward biased causing a current flow from the OUT pin to the V_D pin. The device does not provide any protection function such as current limitation or overtemperature shutdown.

Underload Detection in ON State

An underload condition in ON state is indicated by reducing the sense output current to a very minimal current. In order to detect an underload condition, NCV84090 performs a real−time monitoring of the load current. In case the output current falls below a specified threshold level (I_{OL}), the current sense output current is reduced to a very low value (I_{OL}). This mechanism helps to overcome a high absolute tolerance of the current sense signal at very low load current and to implement an accurate underload detection threshold.

Open Load Detection in OFF State

Open load diagnosis in OFF state can be performed by activating an external resistive pull−up path (R_{PU}) to V_{BAT}. To calculate the pull−up resistance, external leakage currents (designed pull−down resistance, humidity−induced leakage etc) as well as the open load threshold voltage V_{OL_OFF} have to be taken into account.

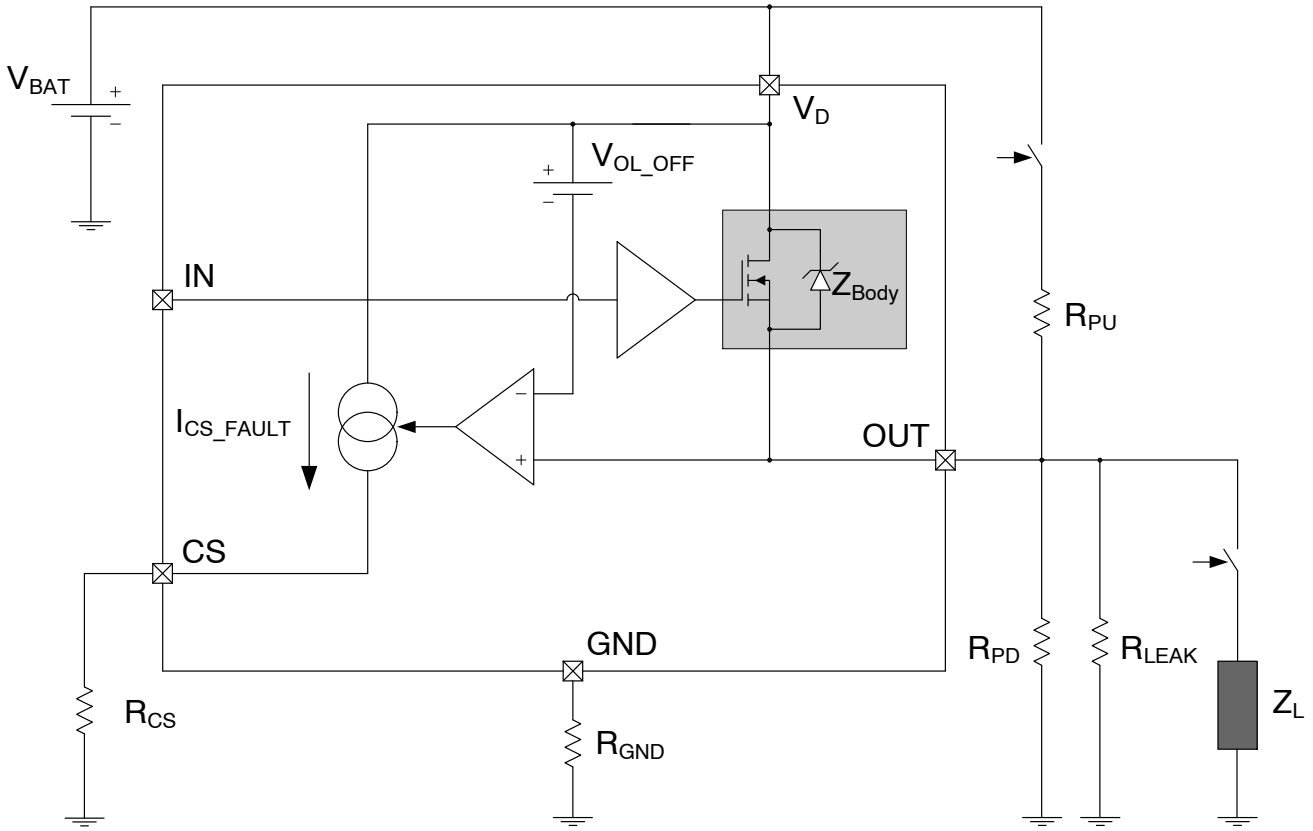


Figure 38. Open Load Detection in Off State

Current Sense in PWM Mode

When operating in PWM mode, the current sense functionality can be used, but the timing of the input signal and the response time of the current sense need to be considered. When operating in PWM mode, the following performance is to be expected. The CS_EN pin should be left high to eliminate any unnecessary delay time to the circuit. When VIN switches from low to high, there will be a typical delay (tCS_High2) before the current sense responds. Once this timing delay has passed, the rise time of the current sense output (ΔtCS_High2) also needs to be considered. When VIN switches from high to low a delay time (tCS_Low1) needs to be considered. As long as these timing delays are allowed, the current sense pin can be operated in PWM mode.

PACKAGE AND PCB THERMAL DATA

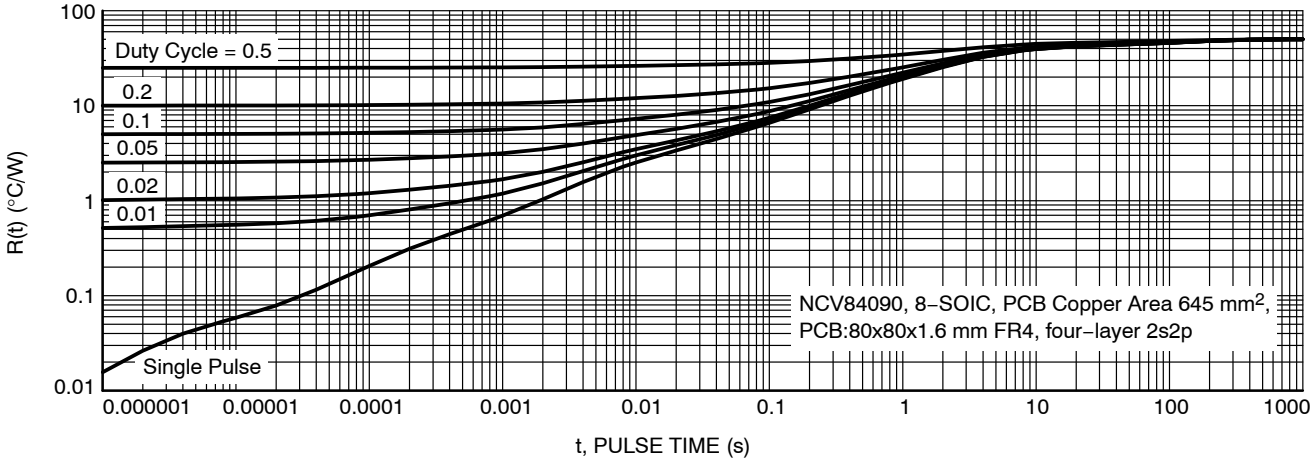


Figure 39. Junction−to−Ambient Transient Thermal Impedance (645 mm^2 Cu Area)

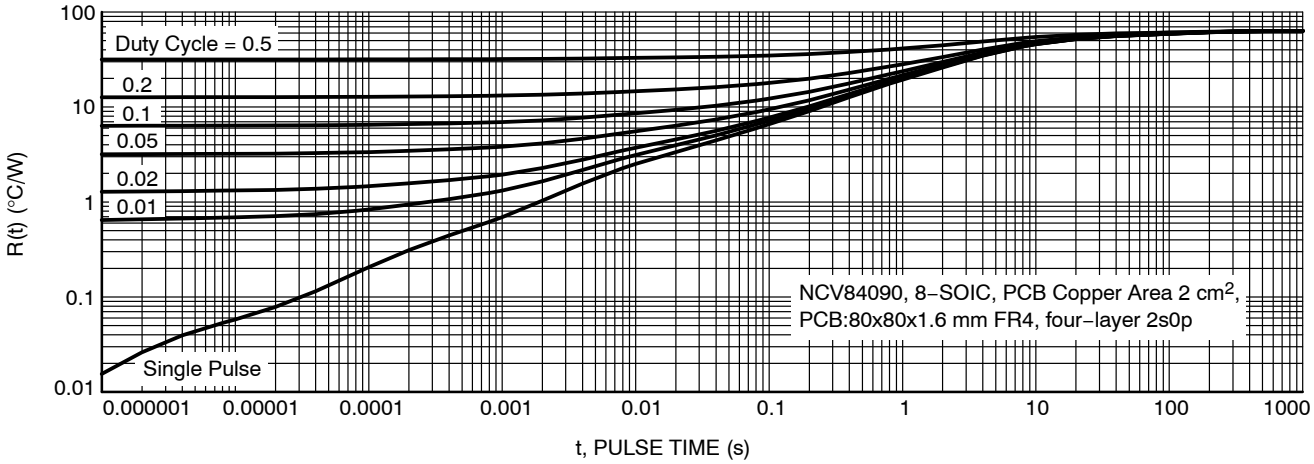
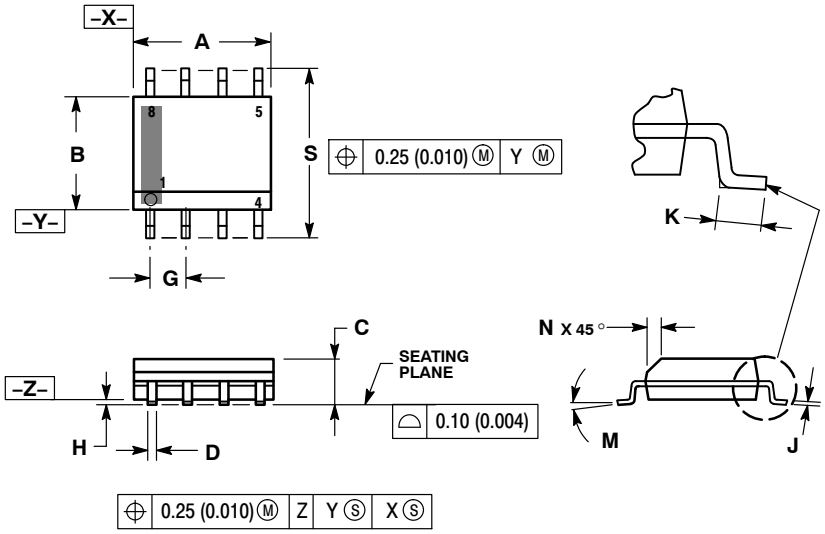


Figure 40. Junction−to−Ambient Transient Thermal Impedance (2 cm^2 Cu Area)

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

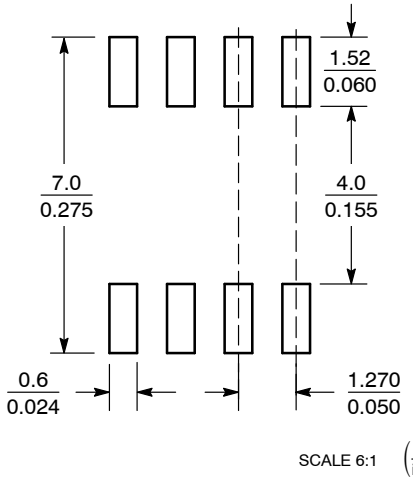
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

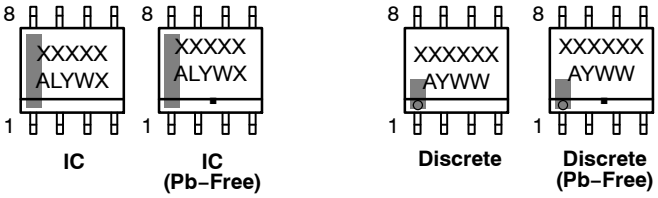
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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