

# Sensitive Gate Silicon Controlled Rectifiers

## Reverse Blocking Thyristors

### 2N5060 Series

Annular PNP devices designed for high volume consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO-92/TO-226AA package which is readily adaptable for use in automatic insertion equipment.

#### Features

- Sensitive Gate Trigger Current – 200  $\mu$ A Maximum
- Low Reverse and Forward Blocking Current – 50  $\mu$ A Maximum,  $T_C = 110^\circ\text{C}$
- Low Holding Current – 5 mA Maximum
- Passivated Surface for Reliability and Uniformity
- These are Pb-Free Devices

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) ( $T_J = -40$ to $110^\circ\text{C}$ , Sine Wave, 50 to 60 Hz, $R_{GK} = 1\text{ k}\Omega$ ) 2N5060	$V_{DRM}$ , $V_{RRM}$	30 60 100 200	V
On-State Current RMS ( $180^\circ$ Conduction Angles; $T_C = 80^\circ\text{C}$ )	$I_{T(RMS)}$	0.8	A
*Average On-State Current ( $180^\circ$ Conduction Angles) ( $T_C = 67^\circ\text{C}$ ) ( $T_C = 102^\circ\text{C}$ )	$I_{T(AV)}$	0.51 0.255	A
*Peak Non-repetitive Surge Current, $T_A = 25^\circ\text{C}$ (1/2 cycle, Sine Wave, 60 Hz)	$I_{TSM}$	10	A
Circuit Fusing Considerations ( $t = 8.3\text{ ms}$ )	$I^2t$	0.4	$\text{A}^2\text{s}$
*Average On-State Current ( $180^\circ$ Conduction Angles) ( $T_C = 67^\circ\text{C}$ ) ( $T_C = 102^\circ\text{C}$ )	$I_{T(AV)}$	0.51 0.255	A
*Forward Peak Gate Power (Pulse Width $\leq 1.0\text{ }\mu\text{sec}$ ; $T_A = 25^\circ\text{C}$ )	$P_{GM}$	0.1	W
*Forward Average Gate Power ( $T_A = 25^\circ\text{C}$ , $t = 8.3\text{ ms}$ )	$P_{G(AV)}$	0.01	W
*Forward Peak Gate Current (Pulse Width $\leq 1.0\text{ }\mu\text{sec}$ ; $T_A = 25^\circ\text{C}$ )	$I_{GM}$	1.0	A
*Reverse Peak Gate Voltage (Pulse Width $\leq 1.0\text{ }\mu\text{sec}$ ; $T_A = 25^\circ\text{C}$ )	$V_{RGM}$	5.0	V
*Operating Junction Temperature Range	$T_J$	$-40$ to $+110$	$^\circ\text{C}$
*Storage Temperature Range	$T_{stg}$	$-40$ to $+150$	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1.  $V_{DRM}$  and  $V_{RRM}$  for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

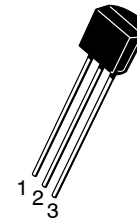
\*Indicates JEDEC Registered Data.

## SILICON CONTROLLED RECTIFIERS

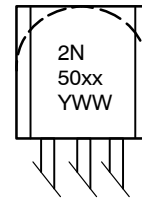
### 0.8 A RMS, 30 – 200 V



#### MARKING DIAGRAM



TO-92  
CASE 29  
STYLE 10



50xx Specific Device Code  
Y = Year  
WW = Work Week

#### PIN ASSIGNMENT

Pin	Assignment
1	Cathode
2	Gate
3	Anode

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

## 2N5060 Series

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	75	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	200	$^{\circ}\text{C/W}$

2. This measurement is made with the case mounted "flat side down" on a heatsink and held in position by means of a metal clamp over the curved surface.

\*Indicates JEDEC Registered Data.

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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#### OFF CHARACTERISTICS

*Peak Repetitive Forward or Reverse Blocking Current (Note 3) ( $V_{AK} = \text{Rated } V_{DRM} \text{ or } V_{RRM}$ )	$I_{DRM}, I_{RRM}$	–	–	10	$\mu\text{A}$
$T_C = 25^{\circ}\text{C}$		–	–	50	$\mu\text{A}$
$T_C = 110^{\circ}\text{C}$		–	–		

#### ON CHARACTERISTICS

*Peak Forward On-State Voltage (Note 4) ( $I_{TM} = 1.2 \text{ A peak @ } T_A = 25^{\circ}\text{C}$ )	$V_{TM}$	–	–	1.7	V
Gate Trigger Current (Continuous DC) (Note 5) *( $V_{AK} = 7.0 \text{ Vdc}, R_L = 100 \Omega$ )	$I_{GT}$	–	–	200	$\mu\text{A}$
$T_C = 25^{\circ}\text{C}$		–	–	350	
$T_C = -40^{\circ}\text{C}$		–	–		
Gate Trigger Voltage (Continuous DC) (Note 5) *( $V_{AK} = 7.0 \text{ Vdc}, R_L = 100 \Omega$ )	$V_{GT}$	–	–	0.8	V
$T_C = 25^{\circ}\text{C}$		–	–	1.2	
$T_C = -40^{\circ}\text{C}$		–	–		
*Gate Non-Trigger Voltage ( $V_{AK} = \text{Rated } V_{DRM}, R_L = 100 \Omega, T_C = 110^{\circ}\text{C}$ )	$V_{GD}$	0.1	–	–	V
Holding Current (Note 3) *( $V_{AK} = 7.0 \text{ Vdc}, \text{initiating current} = 20 \text{ mA}$ )	$I_H$	–	–	5.0	mA
$T_C = 25^{\circ}\text{C}$		–	–	10	
$T_C = -40^{\circ}\text{C}$		–	–		
Turn-On Time Delay Time Rise Time ( $I_{GT} = 1.0 \text{ mA}, V_D = \text{Rated } V_{DRM},$ Forward Current = $1.0 \text{ A}, di/dt = 6.0 \text{ A}/\mu\text{s}$ )	$t_d$ $t_r$	– –	3.0 0.2	– –	$\mu\text{s}$
Turn-Off Time (Forward Current = $1.0 \text{ A}$ pulse, Pulse Width = $50 \mu\text{s}$ , 0.1% Duty Cycle, $di/dt = 6.0 \text{ A}/\mu\text{s}$ , $dv/dt = 20 \text{ V}/\mu\text{s}, I_{GT} = 1 \text{ mA}$ )	$t_q$				$\mu\text{s}$
2N5060, 2N5061		–	10	–	
2N5062, 2N5064		–	30	–	

#### DYNAMIC CHARACTERISTICS

Critical Rate of Rise of Off-State Voltage (Rated $V_{DRM}$ , Exponential, $R_{GK} = 1 \text{ k}\Omega$ )	$dv/dt$	–	30	–	$\text{V}/\mu\text{s}$
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\*Indicates JEDEC Registered Data.

3.  $R_{GK} = 1000 \Omega$  is included in measurement.

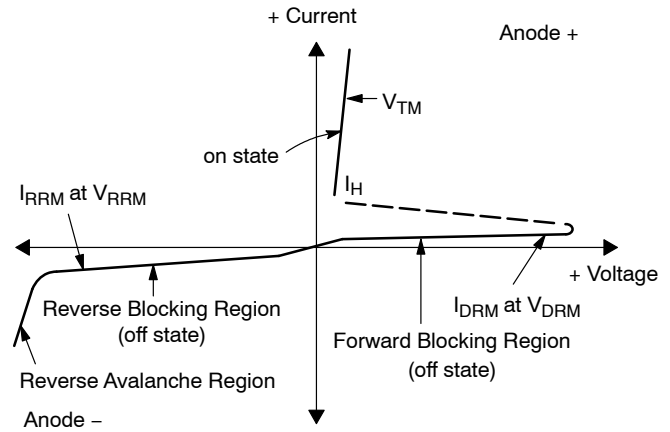
4. Forward current applied for 1 ms maximum duration, duty cycle  $\leq 1\%$ .

5.  $R_{GK}$  current is not included in measurement.

## 2N5060 Series

### Voltage Current Characteristic of SCR

Symbol	Parameter
$V_{DRM}$	Peak Repetitive Off State Forward Voltage
$I_{DRM}$	Peak Forward Blocking Current
$V_{RRM}$	Peak Repetitive Off State Reverse Voltage
$I_{RRM}$	Peak Reverse Blocking Current
$V_{TM}$	Peak on State Voltage
$I_H$	Holding Current



### CURRENT DERATING

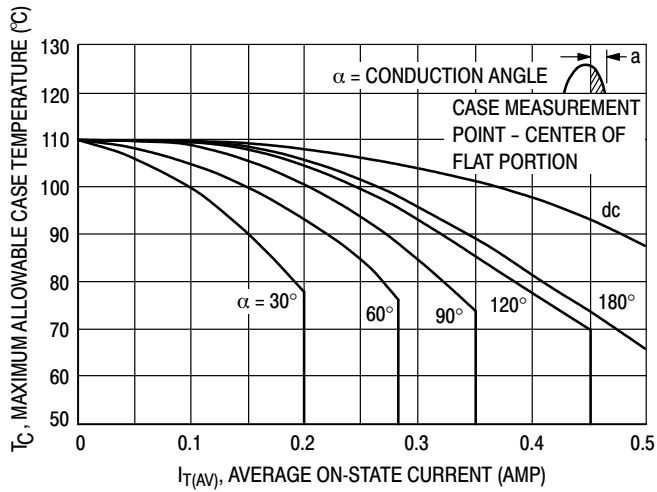


Figure 1. Maximum Case Temperature

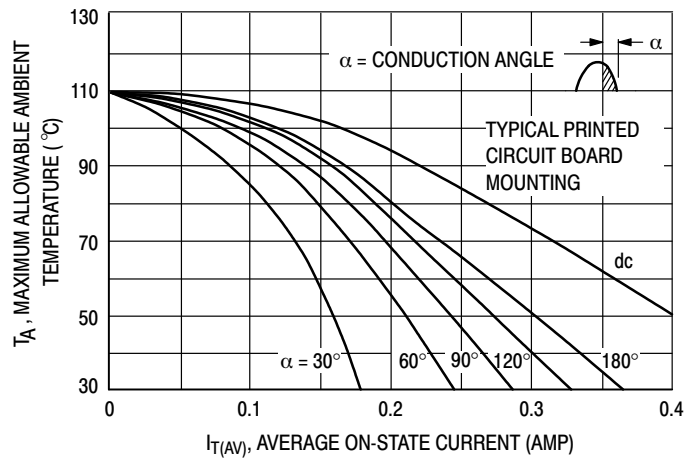


Figure 2. Maximum Ambient Temperature

# 2N5060 Series

## CURRENT DERATING

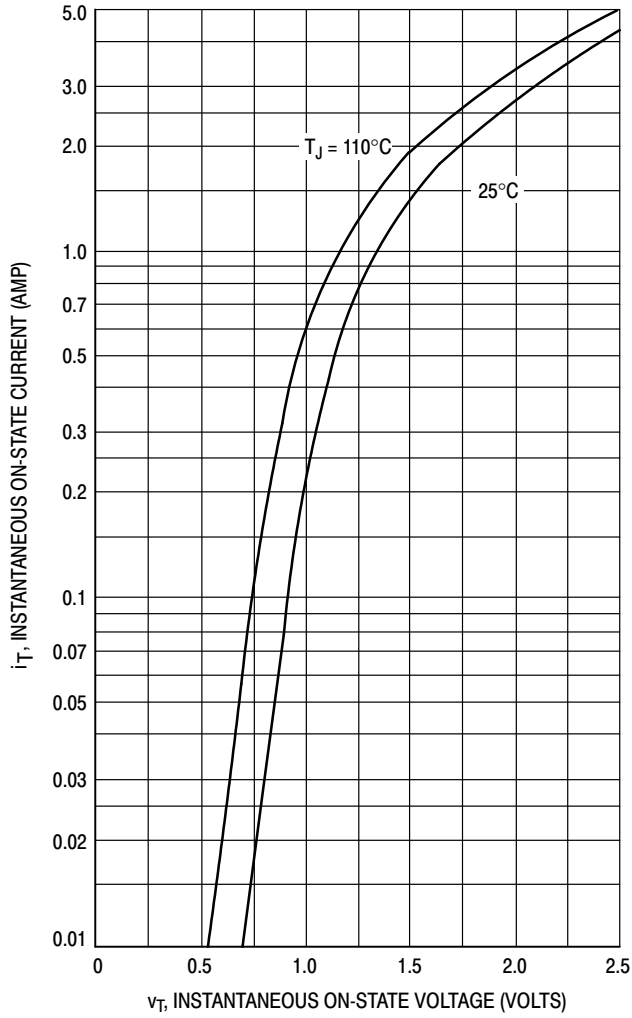


Figure 3. Typical Forward Voltage

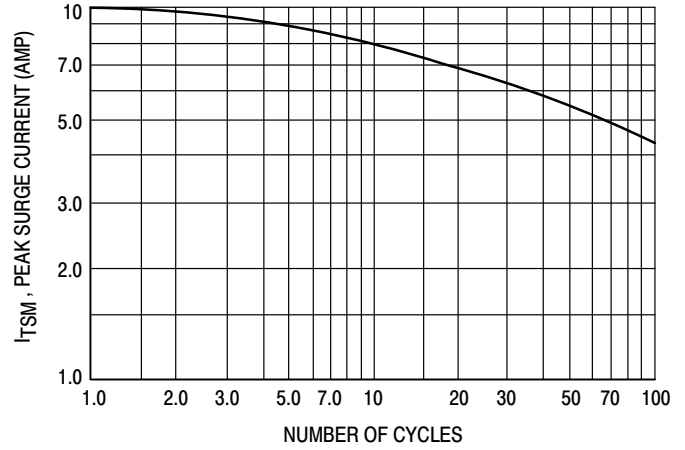


Figure 4. Maximum Non-Repetitive Surge Current

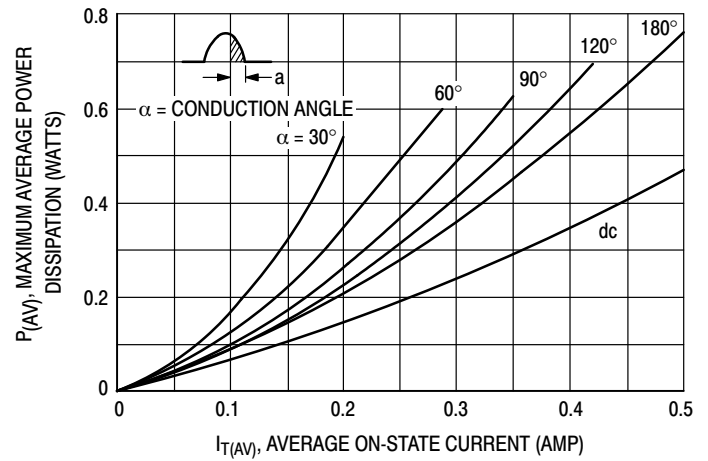


Figure 5. Power Dissipation

## 2N5060 Series

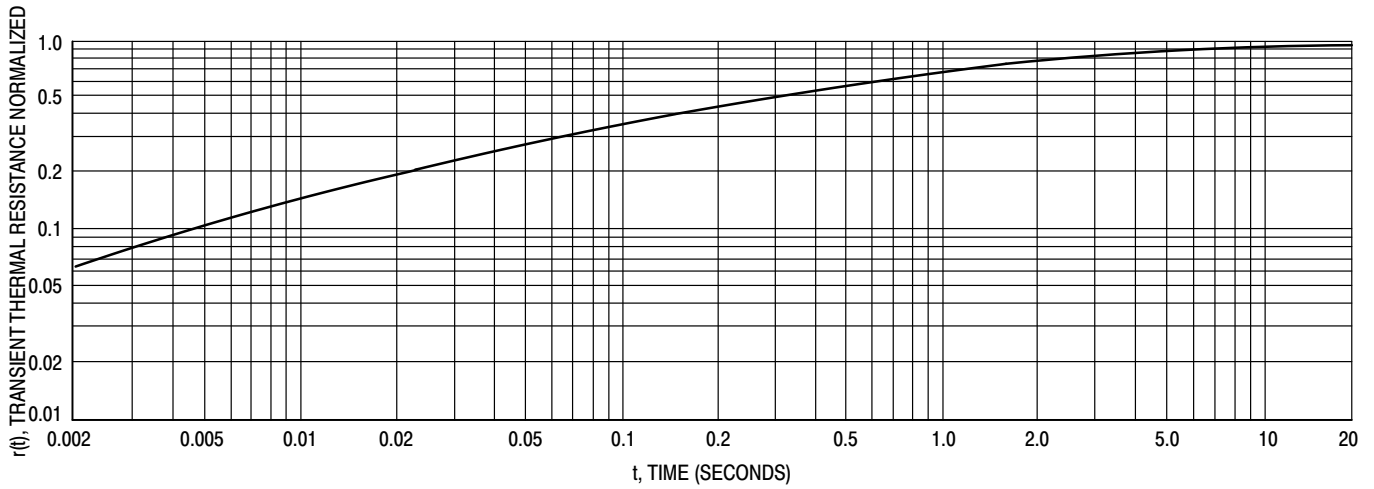


Figure 6. Thermal Response

### TYPICAL CHARACTERISTICS

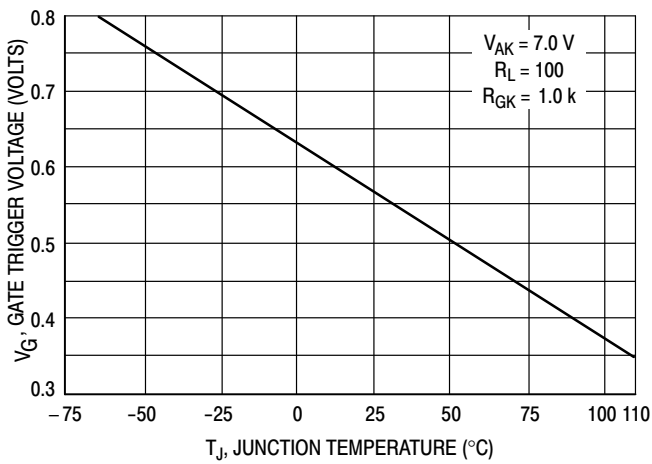


Figure 7. Typical Gate Trigger Voltage

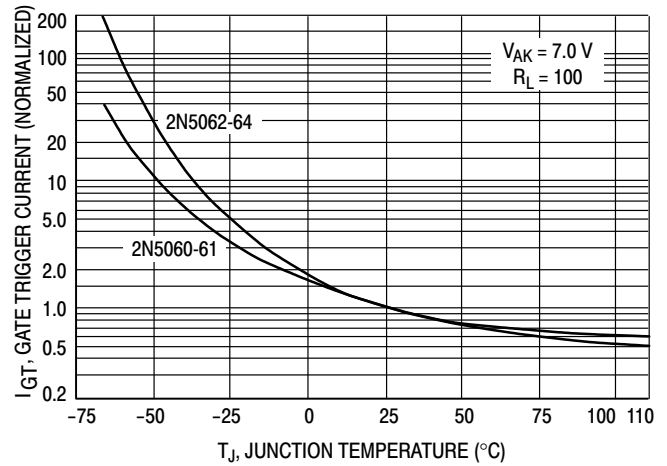


Figure 8. Typical Gate Trigger Current

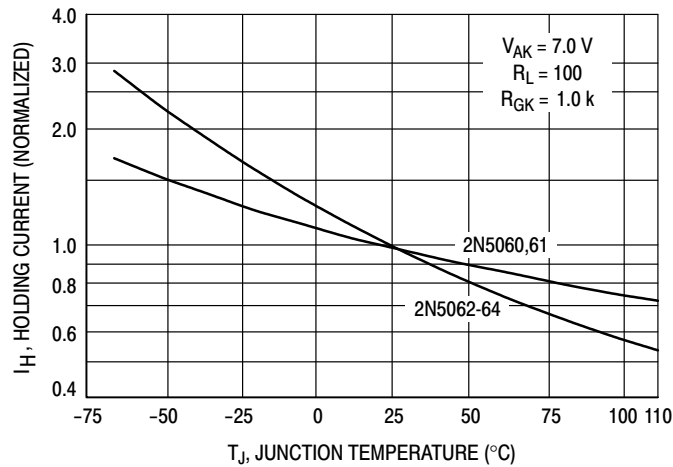


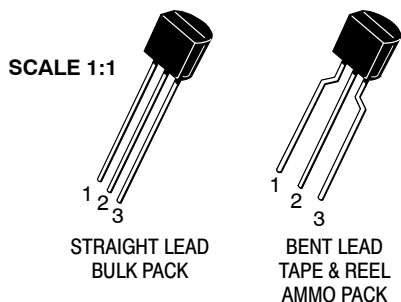
Figure 9. Typical Holding Current

## 2N5060 Series

### ORDERING INFORMATION

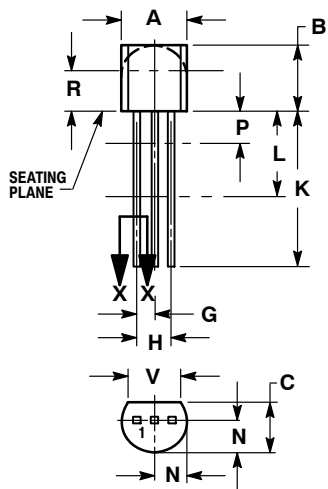
Device	Package	Shipping†
2N5060G	TO-92 (Pb-Free)	5000 Units / Box
2N5060RLRA	TO-92	2000 / Tape & Reel
2N5060RLRAG	TO-92 (Pb-Free)	2000 / Tape & Reel
2N5060RLRMG	TO-92 (Pb-Free)	2000 / Ammo Pack
2N5061G	TO-92 (Pb-Free)	5000 Units / Box
2N5061RLRAG	TO-92 (Pb-Free)	2000 / Tape & Reel
2N5062G	TO-92 (Pb-Free)	5000 Units / Box
2N5062RLRAG	TO-92 (Pb-Free)	2000 / Tape & Reel
2N5064RLRMG	TO-92 (Pb-Free)	2000 / Ammo Pack
2N5064RLRAG	TO-92 (Pb-Free)	2000 / Tape & Reel
2N5064G	TO-92 (Pb-Free)	5000 Units / Box

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

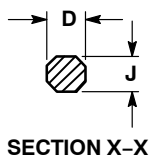


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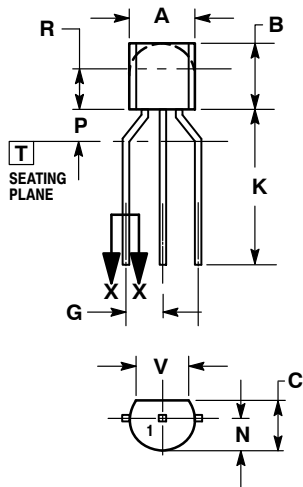
STRAIGHT LEAD  
BULK PACK



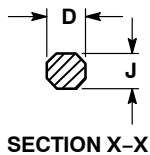
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---



BENT LEAD  
TAPE & REEL  
AMMO PACK



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	MILLIMETERS	
	MIN	MAX
A	4.45	5.20
B	4.32	5.33
C	3.18	4.19
D	0.40	0.54
G	2.40	2.80
J	0.39	0.50
K	12.70	---
N	2.04	2.66
P	1.50	4.00
R	2.93	---
V	3.43	---

STYLES ON PAGE 2

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**CASE 29-11**  
**ISSUE AM**

DATE 09 MAR 2007

STYLE 1: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 2: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 3: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 5: PIN 1. DRAIN 2. SOURCE 3. GATE
STYLE 6: PIN 1. GATE 2. SOURCE & SUBSTRATE 3. DRAIN	STYLE 7: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 8: PIN 1. DRAIN 2. GATE 3. SOURCE & SUBSTRATE	STYLE 9: PIN 1. BASE 1 2. EMITTER 3. BASE 2	STYLE 10: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 11: PIN 1. ANODE 2. CATHODE & ANODE 3. CATHODE	STYLE 12: PIN 1. MAIN TERMINAL 1 2. GATE 3. MAIN TERMINAL 2	STYLE 13: PIN 1. ANODE 1 2. GATE 3. CATHODE 2	STYLE 14: PIN 1. EMITTER 2. COLLECTOR 3. BASE	STYLE 15: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2
STYLE 16: PIN 1. ANODE 2. GATE 3. CATHODE	STYLE 17: PIN 1. COLLECTOR 2. BASE 3. EMITTER	STYLE 18: PIN 1. ANODE 2. CATHODE 3. NOT CONNECTED	STYLE 19: PIN 1. GATE 2. ANODE 3. CATHODE	STYLE 20: PIN 1. NOT CONNECTED 2. CATHODE 3. ANODE
STYLE 21: PIN 1. COLLECTOR 2. EMITTER 3. BASE	STYLE 22: PIN 1. SOURCE 2. GATE 3. DRAIN	STYLE 23: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 24: PIN 1. EMITTER 2. COLLECTOR/ANODE 3. CATHODE	STYLE 25: PIN 1. MT 1 2. GATE 3. MT 2
STYLE 26: PIN 1. V <sub>CC</sub> 2. GROUND 2 3. OUTPUT	STYLE 27: PIN 1. MT 2. SUBSTRATE 3. MT	STYLE 28: PIN 1. CATHODE 2. ANODE 3. GATE	STYLE 29: PIN 1. NOT CONNECTED 2. ANODE 3. CATHODE	STYLE 30: PIN 1. DRAIN 2. GATE 3. SOURCE
STYLE 31: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 32: PIN 1. BASE 2. COLLECTOR 3. EMITTER	STYLE 33: PIN 1. RETURN 2. INPUT 3. OUTPUT	STYLE 34: PIN 1. INPUT 2. GROUND 3. LOGIC	STYLE 35: PIN 1. GATE 2. COLLECTOR 3. EMITTER

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