Cascode Primer

Operation of the SiC Cascode JFET

AND90328/D

SCOPE

This document explains the operation of **onsemi** SiC cascode FETs to facilitate their use in both hard-switched and soft-switched applications. Included is a description of cascode construction, key parameters, unique features, and design support.

REFERENCED DOCUMENTS

onsemi SiC FET User Guide

Switching Fast SiC FETs with a Snubber

INTRODUCTION

The SiC JFET has some significant advantages over competing technologies, particularly low on-resistance for a given chip area, known as $R_{DS}{\cdot}A$. A tradeoff for minimal $R_{DS}{\cdot}A$ is a normally-on characteristic, meaning if there is no gate-source voltage, or if the JFET gate is left floating, then the JFET is fully on. Switch-mode applications generally require normally-off operation. Therefore, the SiC JFET is combined with a low-voltage silicon MOSFET in cascode configuration to make a normally-off switch-mode "FET", which retains most of the benefits of the SiC JFET.

CASCODE CONSTRUCTION

The cascode is made by series-connecting a SiC JFET with a low-voltage, normally-off Si MOSFET, with the JFET gate connected to the MOSFET source. The MOSFET drain-source voltage is the inverse of the JFET gate-source voltage so that the cascode has a familiar normally-off characteristic. The cascode blocks current up to a rated drain-source voltage, but reverse current can always flow, as with a MOSFET, be it made of silicon or silicon-carbide.

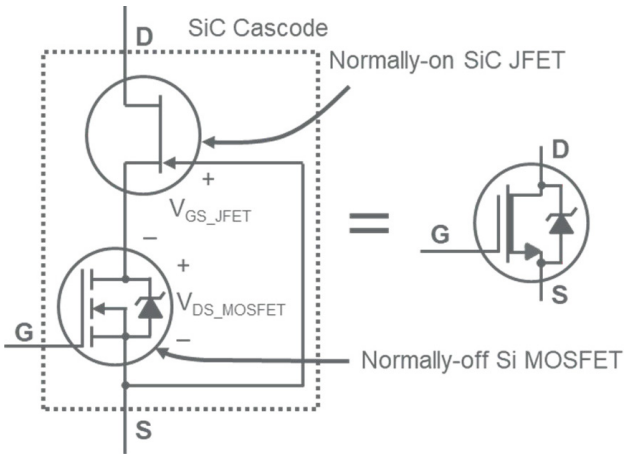
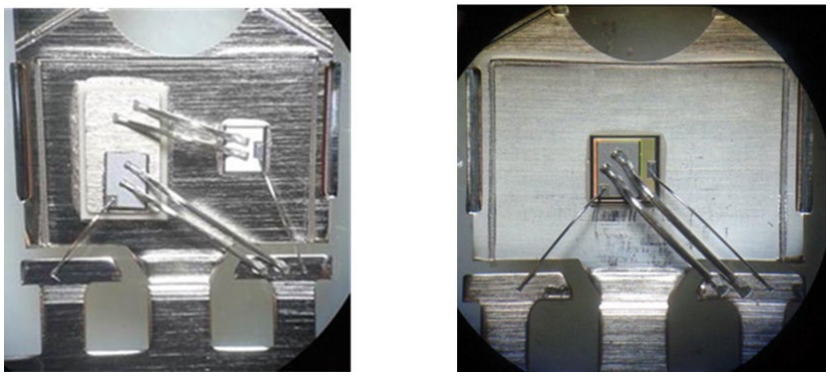


Figure 1. Cascode Configuration

With the internal MOSFET on or with reverse current flowing regardless of the cascode's gate voltage, the JFET gate-source voltage is nearly zero and the JFET is on. With the MOSFET off and positive V_{DS} across the cascode, the MOSFET V_{DS} increases while the JFET gate-source voltage decreases past the JFET threshold voltage, which turns the JFET off. See Figure 1.



(a) (b)

Figure 2. Discrete Cascode Construction

Discrete cascode construction is either side-by-side chips, as shown in Figure 2(a), or stacked chips as in Figure 2(b). In both cases, the SiC JFET is usually silver-sintered to the package leadframe. In the side-by-side configuration, the MOSFET is attached onto a metal-plated ceramic isolator, and there are two sets of source bond wires: one between JFET source and MOSFET drain (topside of the metal-plated ceramic), and one between the MOSFET source and the source pin. In the stacked-chip configuration, the bond wires between JFET source and MOSFET drain are eliminated, thus reducing the stray inductance. The smaller diameter bond wires attach the JFET and MOSFET gates.

The MOSFET is designed for cascode operation with an active-area avalanche set at about 25 V. Being based on a 30 V silicon process, the MOSFET has low $R_{DS(on)}$, usually 10% that of the JFET, and low reverse recovery charge Q_{RR}. The JFET blocks the high voltage. Most of the switching and conduction losses are in the JFET.

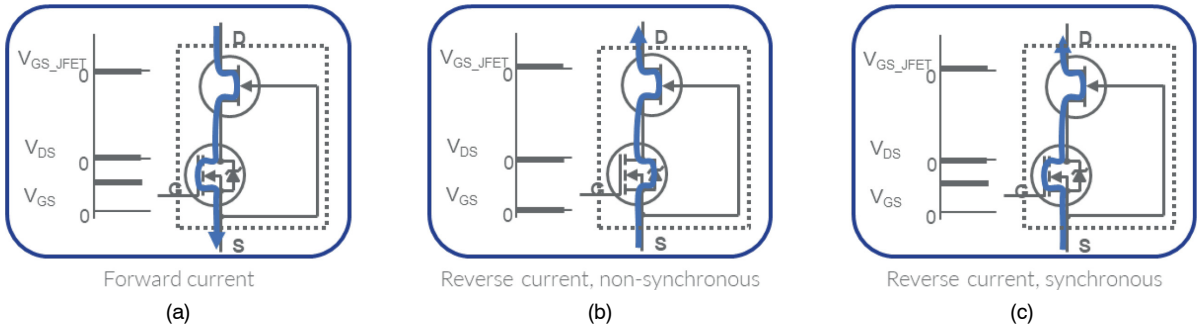


Figure 3. Cascode Forward and Reverse Current Operation

The cascode $R_{DS(on)}$ includes the on-resistance of both the SiC JFET and the low-voltage silicon MOSFET. With the cascode gate off, reverse current flows through the MOSFET body diode, which automatically turns on the JFET, as depicted in Figure 3(b) with non-synchronous reverse current. In this case, the source-drain voltage is the MOSFET body diode drop plus JFET on-resistance. Because the MOSFET inside the cascode is made of silicon, the source-drain voltage with the gate off is less than half that of a competing SiC MOSFET. With the gate on, the cascode has the same conduction loss for both forward and reverse current.

The gate voltage range of the cascode is very flexible for two reasons. First, the gate is the MOSFET gate that has a threshold voltage near 5 V at room temperature, eliminating the need for negative gate voltage. The gate voltage range is ±20 V without risk of threshold voltage drift or hysteresis, and there are built-in gate protection Zener diodes. Second, the cascode has high gain. Figure 4 shows the 25 °C output characteristics of UJ4SC075005L8S, a 750 V, 5.4 mΩ, Gen 4 stacked-chip cascode in TOLL (MO-229) package.

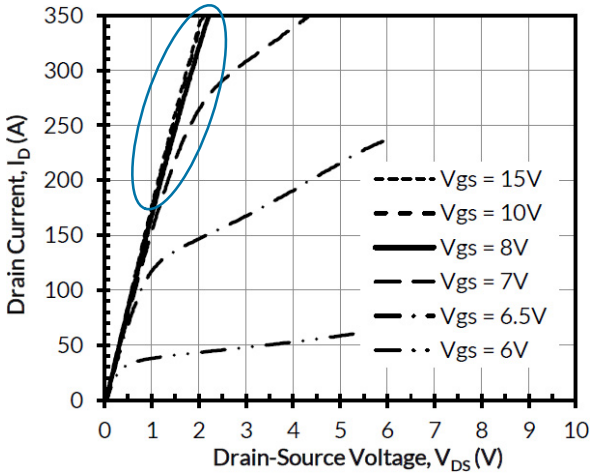


Figure 4. Cascode's High Gain Enables 10 V Gate Drive

Notice how little the conductivity changes as the cascode gate-source voltage exceeds about 8 V. Once the MOSFET is on, the JFET is fully on. This means that the cascode can be driven with 0 to 10 V bootstrap for example to minimize gate driver power and cost. On the other hand, there is no harm from wider gate voltage ranges, such as −5 to +18 V.

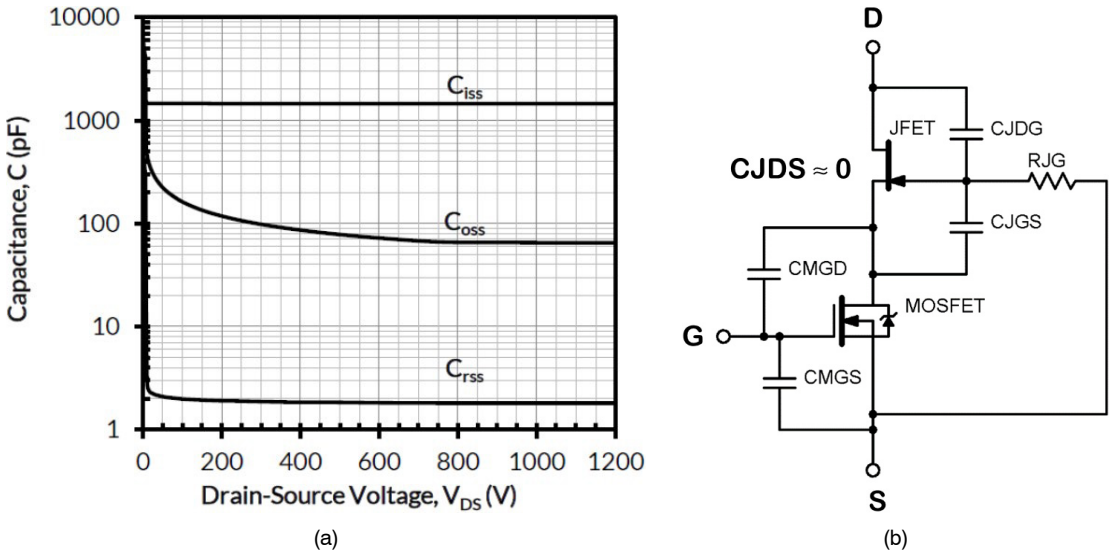


Figure 5. Cascode Capacitances

Figure 5(a) shows the chip capacitances of the MOSFET and JFET. Note that the JFET gate resistance RJG in Figure 5(b) is not a separate resistor, but rather is part of the JFET chip. A key difference between the cascode and other power transistors is the lack of gate-drain capacitance. Once V_{DS} exceeds the JFET threshold voltage, C_{rss} drops practically to zero. This is because the JFET has no drain-source capacitance – there is no PN junction nor body diode feature to create such capacitance. This means that during the switching voltage transition, the cascode's dV_{DS}/dt is largely determined by the external circuit instead of the cascode gate resistance. The switching speed of the cascode's MOSFET is controllable by the cascode gate resistance, whereas the JFET switching speed is partially determined by the cascode's MOSFET and otherwise by the external circuit. This is the reason the cascode benefits from a drain-source snubber to control turn-off switching speed and voltage overshoot when hard switching, as will be explained. All the JFET output capacitance (gate-drain plus drain-source capacitances) is gate-drain capacitance. The cascode output capacitance C_{oss} is approximately equal to the JFET gate-drain capacitance. The cascode input capacitance C_{iss} is mostly from the cascode's MOSFET gate-source capacitance.

CASCODE SWITCHING CHARACTERISTICS

Hard Switching

Most cascodes have lower turn-off versus turn-on switching energy, E_{off} versus E_{on}. This is evident in the switching energy versus current graph in datasheets, see Figure 8(a). The cascode inherent switching speed is mostly determined by the JFET capacitances and JFET on-chip gate resistance, which is set by design for competitive total switching loss $E_{total} = E_{off} + E_{on}$. Much of the effort in applying the cascode is to slow the turn-off switching to limit voltage overshoot and ringing. Here an understanding of the cascode capacitances is valuable. Figure 6 shows a cascode switching off with an inductive load, with the cascode output capacitance (equal to the JFET gate-drain capacitance) and on-chip JFET gate resistance depicted in the cascode along with the SiC JFET and Si MOSFET.

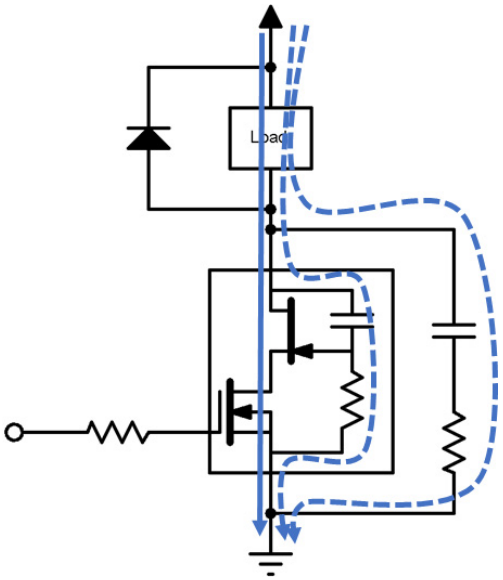


Figure 6. Cascode Turn-off with Snubber

The solid arrow in Figure 6 depicts the current flowing through the inductive load and the cascode while the cascode is on. As the cascode switches off, it becomes resistive, and current diverts to the output capacitance and JFET gate resistance as the cascode drain-source voltage increases. Only load current charges the cascode output capacitance because of the lack of gate-drain capacitance; no current is forced through the cascode gate. This results in low gate charge and immunity from dV/dt induced (parasitic)

turn-on, which are attractive features of the cascode. It creates however a challenge for speed control because gate current is not involved in charging the cascode output capacitance, and therefore adjusting the cascode gate resistance has no direct effect on the cascode switching voltage slew rate dV/dt. The gate resistance adjusts the switching speed of the cascode's MOSFET, so the switching current slew rate di/dt can be adjusted. (This is somewhat a simplified explanation because with high enough cascode gate resistance, the dV/dt can be regulated, but then the switching delay time would be excessive.) Because of the faster turn-off versus turn-on speed of the cascode, see Figure 8(a), a turn-off snubber is recommended for hard-switching, usually in the form of a resistor-capacitor (RC) snubber connected across drain and source. The cascode's fixed output capacitance is augmented with additional output capacitance plus damping resistance, both of which are adjustable based on the application requirements. Figure 6 depicts additional current diverted away from the cascode during turn-off, thus reducing dV/dt and di/dt of the cascode. In this way, the snubber compensates for the limited switching speed control provided by the cascode gate resistance.

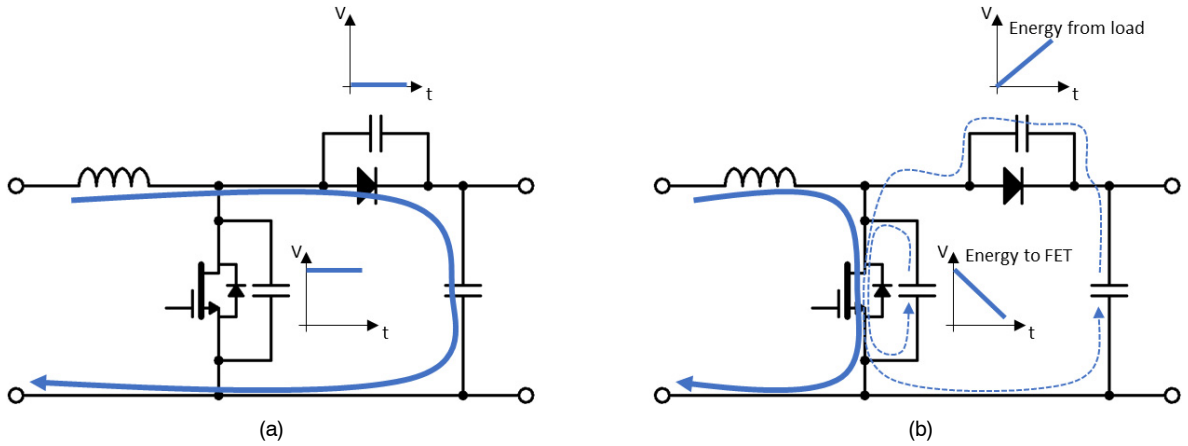


Figure 7. Energy Stored in C_{oss} and Partially in Snubber Capacitance is Dissipated in the Cascode During Hard Turn-on

In Figure 7, the output capacitance plus additional snubber capacitance is represented by a drain-source capacitor. The energy stored in C_{oss} and partially in snubber capacitance is dissipated in the cascode during turn-on. The remainder of the snubber capacitance energy is dissipated in the snubber resistor (if installed). This results however in only a slight increase in the total switching loss.

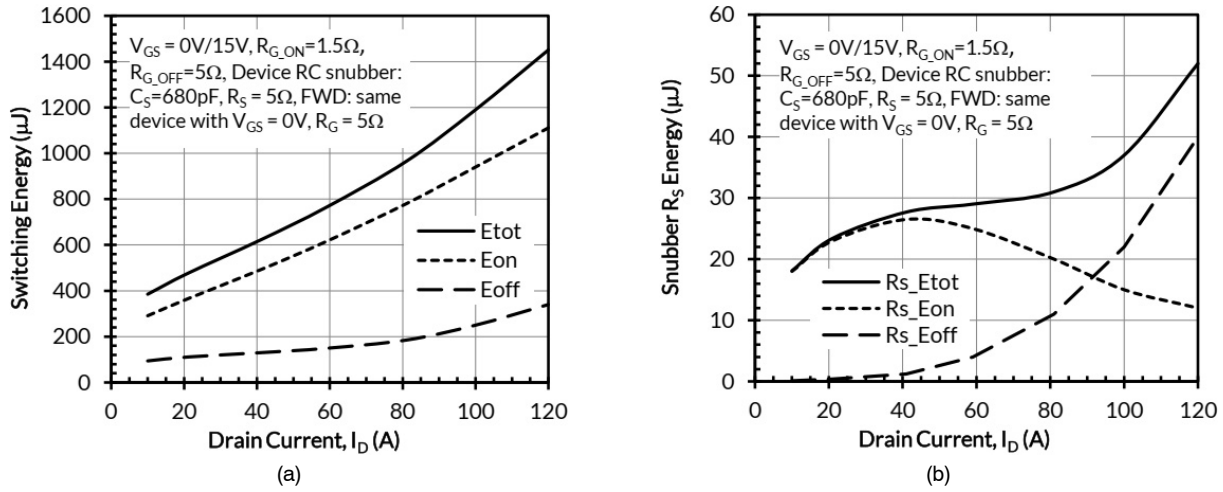


Figure 8. (a) Switching Energy versus Current, and (b) Snubber Resistor Energy versus Current for UJ4SC075005L8S

Figure 8(a) shows the hard-switching loss versus current for the UJ4SC075005L8S cascode. Here you can see the significantly higher turn-on versus turn-off switching energy, which is typical of many cascode parts. Figure 8(b) shows the corresponding snubber resistor energy for this same part. Total snubber loss is 3 to 5% of the total hard-switching loss. Remember however that without the snubber, there is often excessive turn-off voltage overshoot and ringing. With the snubber, all waveforms are damped both at turn-on and turn-off: cascode V_{DS}, V_{GS}, and I_D. The snubber has proven to be the most efficient way to regulate the cascode switching. The total switching loss is lower with a snubber and less gate resistance versus no snubber and more gate resistance. This is true of both SiC JFET cascodes and many SiC MOSFETs.

Soft Switching

Soft switching generally includes zero-voltage switching (ZVS) resulting from a FET switching on after reverse current flows through it, thus the drain-source voltage is nearly zero.

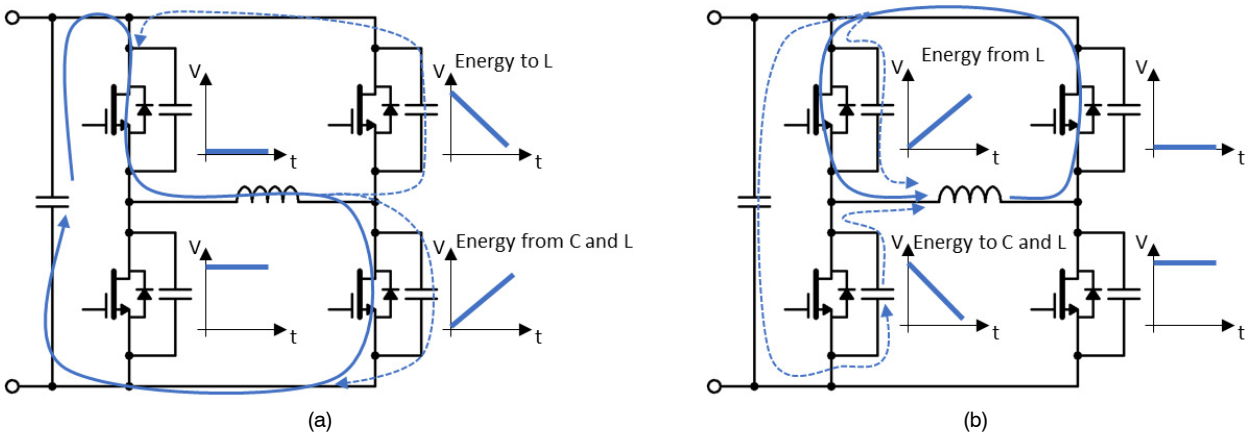


Figure 9. Energy Stored in C_{oss} and in Snubber Capacitance is Recycled with ZVS Turn-on

In Figure 9(a), the lower right cascode is turning off while the upper right cascode begins to freewheel. Drain-source charge is recycled from the upper right cascode to the load. Similarly in Figure 9(b), the upper left cascode is turning off while the lower left cascode begins to freewheel. Drain-source charge is recycled from the lower left cascode to the input and to the load. Thus, with ZVS, not only is the turn-on switching loss eliminated, but also the turn-off loss is reduced because of the recycling of energy stored in C_{oss} and snubber capacitance if installed. If a snubber resistor is included, then of course some of the energy in the snubber capacitor is dissipated in the snubber resistor. In the absence of a snubber, the difference between soft-switched and hard-switched E_{off} is the hard-switched E_{off} minus E_{oss}, which is a small difference for fast switching devices.

The fast turn-off speed in combination with the flexible gate drive and low $R_{DS}{\cdot}C_{oss}$ (a consequence of the SiC JFET's low $R_{DS}{\cdot}A$) make the cascode especially attractive for soft switching applications. Depending on the snubbing elsewhere in the circuit (across the transformer and/or output rectifiers for example), a drain-source capacitor may be needed for turn-off snubbing of the cascode, even with ZVS turn-on. If the circuit operates out of resonance and hard switches, then it may be beneficial to add a damping resistance in series with the snubber capacitance.

A Look Inside the Cascode During Switching

Let us consider again the cascode in Figure 6 switching off with an inductive load, redrawn in Figure 10 but including stray inductances. As the cascode's MOSFET turns off, its resistance increases and so does the MOSFET drain-source voltage. In fact, unless the cascode gate resistance is unusually large, the cascode's MOSFET avalanches during turn-off, clamping the JFET gate-source voltage at −25 V. This is completely safe for the JFET because its gate-source avalanche voltage is well below −25 V. It is also safe for the MOSFET because it was designed to withstand repetitive avalanche at high currents, and the duration of the avalanche is short, so the energy is low. The load current diverts from the JFET and MOSFET channel and charges the output capacitance (and snubber capacitance) until the other device in the circuit freewheels the current.

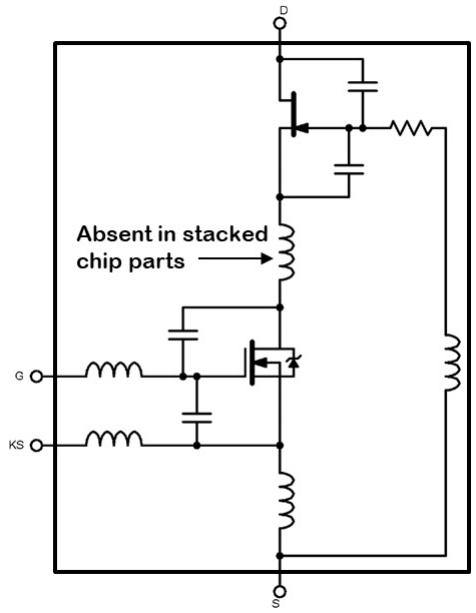


Figure 10. Cascode Including Stray Inductances and Relevant Capacitances

The lower the cascode gate resistance, the faster the cascode's MOSFET V_{DS} rises, and the longer the MOSFET clamps the JFET V_{GS} to −25 V. The difference between the JFET V_{GS} and its threshold voltage is maximum while the JFET V_{GS} is clamped at −25 V, in other words while the MOSFET is in avalanche. This is when the JFET is most immune to noise. The MOSFET comes out of avalanche when the energy stored in stray inductances is sufficiently reduced, and usually there is ringing as this happens. Most of the stray inductance involved is in the source bond wires and package source pins. After avalanche, the MOSFET V_{DS} settles near the JFET threshold voltage as the JFET completes its turn-off transient. This is when noise involving source inductance, if excessive, can exceed the smaller difference between JFET V_{GS} and JFET threshold voltage and cause spurious turn-on of the JFET. The cascode especially benefits from packages with a separate Kelvin-source pin because it reduces the ringing on the gate of the cascode (the cascode's MOSFET gate) and hence the gate of the internal JFET by eliminating load current induced voltages in the gate drive loop. A similar argument holds for turn-on. Fast turn-on of the cascode's MOSFET reduces the time the MOSFET V_{DS} is close in magnitude to the JFET threshold voltage and hence the noise immunity is improved.

Recovery After Freewheeling

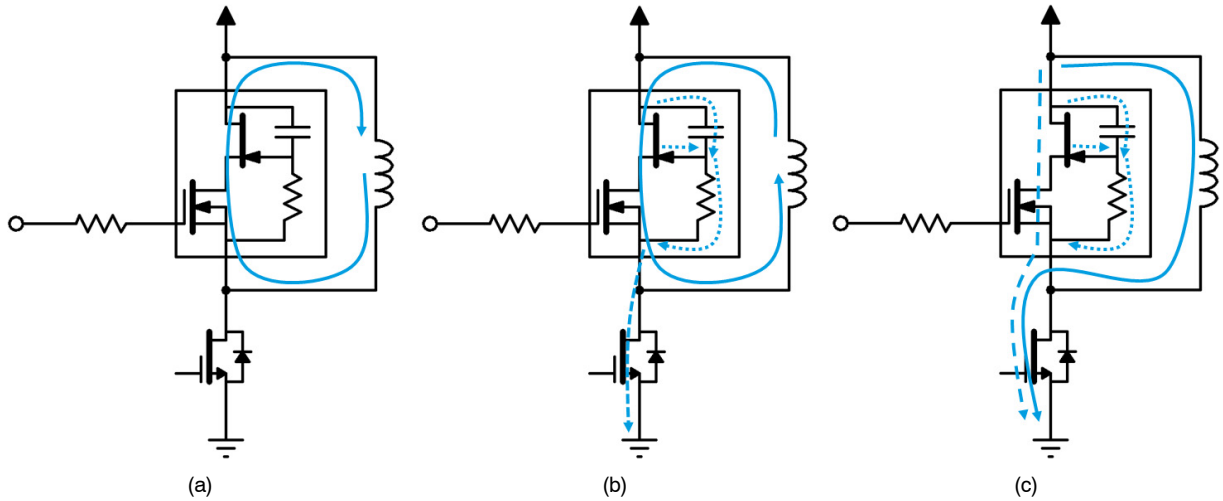


Figure 11. Freewheeling Cascode Transitioning through "Reverse Recovery"

Now let us consider a cascode that is freewheeling as shown in Figure 11(a). The freewheeling cascode's MOSFET keeps the JFET on even after the MOSFET is gated off during the deadtime. Current must commutate to the other (lower in this case) cascode and reverse direction before the upper cascode can support drain-source voltage. The V_{GS} of the JFET in the freewheeling cascode must transition from slightly positive to more negative than the JFET threshold voltage. First the freewheeling cascode's MOSFET goes through a real reverse recovery, which happens very quickly and with very little charge due to the short minority carrier lifetime in the 30 V MOSFET, as depicted in Figure 11(b). Then, typically, the MOSFET avalanches, just as in the hard-switched turn-off previously discussed. The JFET V_{GS} transition depends on the JFET output (gate-drain) capacitance and the on-chip gate resistance. Meanwhile, current continues to flow through the freewheeling JFET and its MOSFET until the JFET completes its turn-off sequence, as indicated in Figure 11(c). Only a small portion of this current is from the freewheeling cascode's MOSFET body diode. Most of the cascode's reverse recovery charge is from current flowing while the JFET in the freewheeling cascode turns off. This cascode reverse recovery effect is independent of temperature and largely independent of current because it depends on the JFET gate-drain capacitance and the JFET gate resistance.

The recovery charge is about the same regardless of current, which makes switching waveforms at high current look quite good but causes a relatively high E_{on} at low currents.

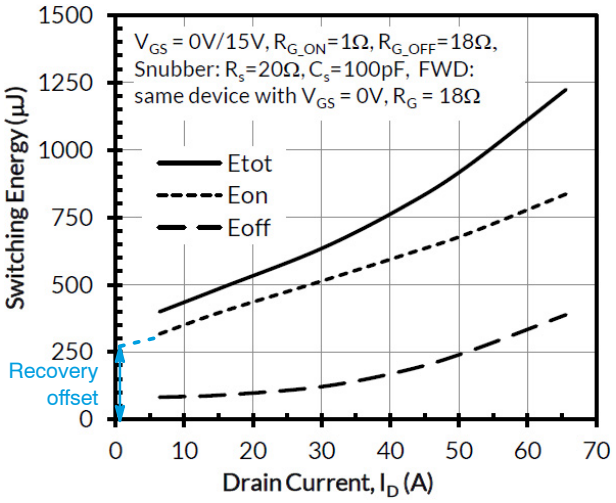


Figure 12. Switching Energy versus Current for UF4SC120023K4S, a 1200 V, 23 mΩ Gen 4 Cascode

This recovery effect is evident in the offset of the E_{on} versus current curve in the cascode datasheets, which show data from an inductively loaded hard-switched half-bridge. Figure 12 shows an example of an extrapolated E_{on} curve, where if it were possible to measure E_{on} at nearly zero current, the resulting E_{on} would be almost entirely due to the recovery of the freewheeling cascode.

THE CASCODE TRADEOFF

The SiC JFET cascode has a completely different tradeoff circle from SiC MOSFETs. Challenges related to manufacturing a MOS gate on SiC are irrelevant to the cascode. The fundamental cascode tradeoff is the reverse recovery charge effect and the associated hard-switched turn-on energy versus voltage overshoot at turn-off and the tendency to ring and oscillate. The main “knob” to regulate this tradeoff is the cascode’s JFET gate resistance, but this is inside the part and is therefore not adjustable, hence the reliance on external snubber components and gate resistor to tune the switching. Higher JFET gate resistance slows the cascode switching slew rates, which makes the part easier to use but at the expense of higher reverse recovery charge and hard-switched turn-on loss. This option is available in the Gen3 ‘UJ3’ series parts, which have higher internal JFET gate resistance than all other **onsemi** cascode products. These UJ3 parts are especially well suited to soft-switching as well as lower frequency applications. The **onsemi** Gen3 ‘UF3’ series and all Gen4 cascode products are optimized for industry leading total switching loss and have correspondingly high switching slew rates.

APPLICATION SUPPORT

The SiC FET User Guide and Snubber Application Note are the result of extensive testing and provides gate drive and snubber guidance for all released cascode products. Find more information and view additional application notes about **onsemi** SiC JFET at SiC JFET Technical Documents. SPICE and XML files are available on each JFET, cascode, and diode product page; look for ‘Simulation Files’ on the Documents tab. Elite Power Simulator also supports all released power devices and is a quick and easy way to evaluate both topologies and part number selection. Finally, expert technical support is available.

SUMMARY

- The cascode configuration is a way to exploit the low R_{DS}·A of the normally-on SiC JFET in switch-mode applications.
- Flexible gate drive, fast turn-off, and low R_{DS}·C_{oss} make the cascode excel in soft-switched applications.
- Absence of gate-drain capacitance brings low gate charge but also limited switching speed control by gate resistance, so the cascode benefits from a snubber to regulate the inherently fast turn-off speed.
- Cascode hard-switched reverse recovery effect is mostly independent of temperature and current.
- Cascodes work best with a Kelvin-source connection and minimum possible gate resistance.
- User Guide, application notes, videos, simulation files, free online simulator & calculator software, and expert technical support are available.

ADDITIONAL INFORMATION

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