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AND8254/D

Avalanche TVS Diode SPICE Macro-Models

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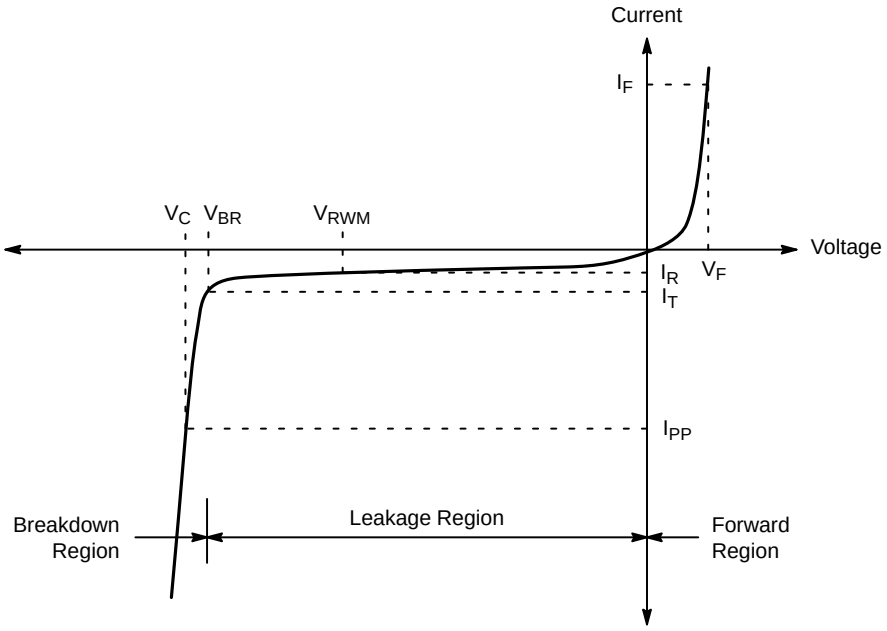
APPLICATION NOTE

Introduction

SPICE macro-models provide an accurate simulation of a TVS avalanche diode's current versus voltage characteristics. These models can be used to analyze and optimize the performance of surge protection circuits. TVS macro-models are created by combining standard SPICE devices into a sub-circuit.

Data Sheet Specifications

The first item required to analyze the TVS macro-models is to review the device specifications listed on the data sheet. Figure 1 provides the current and voltage definitions of a unidirectional avalanche TVS diode.



I_F	Forward current	V_{BR}	Breakdown voltage @ I_T
V_F	Forward voltage @ I_F	I_{PP}	Maximum reverse peak pulse current (typically specified with either the 8 × 20 μs or 10 × 1000 μs surge pulse)
I_R	Reverse leakage current	V_C	Clamping voltage @ I_{PP}
V_{RWM}	Reverse working voltage @ I_R ($V_{RWM\ (typ.)} \cong 0.8 \times V_{BR}$)		
I_T	Test current		

Figure 1. Definition of the Current and Voltage Data Sheet Specifications

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Other important data sheet specifications include the capacitance and peak power rating. The capacitance of the diode is typically specified at a bias voltage of 0 Vdc, with an AC signal of 50 mV at 1.0 MHz. The power rating is typically defined for a small package with the 8 × 20 μs (rise time × pulse duration), while the 10 × 1000 μs surge pulse is often used for defining devices in large packages. The peak energy in Watts is measured by multiplying the surge current (I_{PP}) and clamping voltage (V_C) waveforms together.

Macro-Model Sub-Circuit

The TVS diode's macro-models are created by combining standard SPICE devices into a sub-circuit. Figure 2 shows a schematic of the macro-model. Appendix I provides the PSPICE netlist's of the 1SMB28A and NUP2105 macro-models. The TVS macro-model is based on the Zener diode model documented in references [3] and [4]. References [1] and [2] provide alternative TVS diode SPICE models.

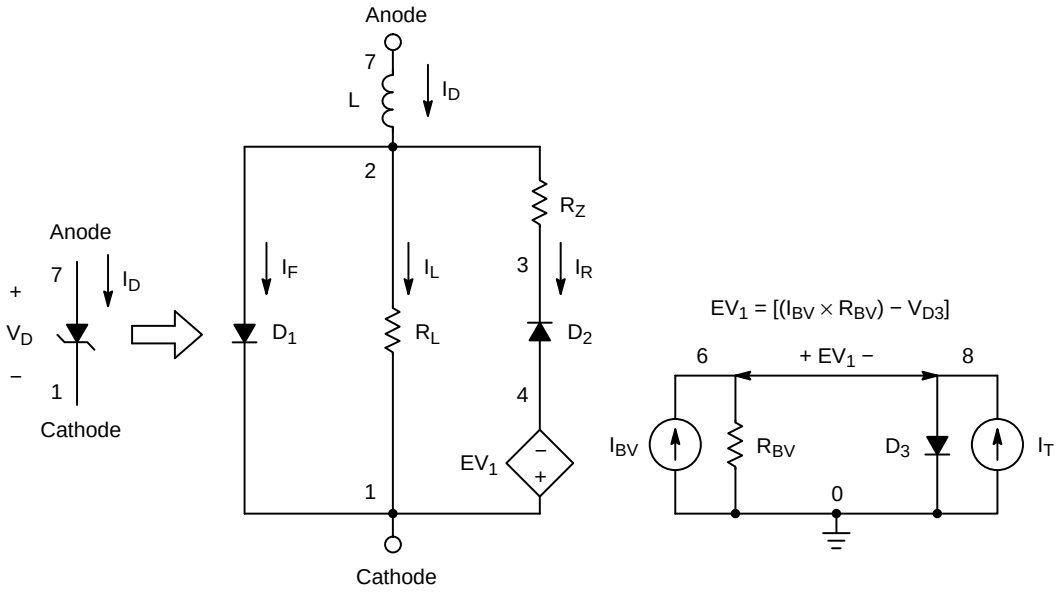


Figure 2. TVS Avalanche Diode SPICE Macro-Model

Forward Region

Diode D_1 is the key component when voltage V_D is greater than zero. The TVS diode's forward bias characteristics are controlled by D_1's saturation current (IS), emission coefficient (N) and series resistance (RS) variables. The current equations for the forward bias region are listed below.

$$I_D = I_F + I_L + I_R$$

$$= I_{F\_D1} + \frac{V_D}{R_L} + I_{S\_D2}$$

$$I_L \,\&\, I_R << I_F$$

$$\therefore I_D \cong I_{F\_D1} \cong I_{S\_D1}\left[e^{\wedge}\left(\frac{V_{D1}}{\eta V_T}\right) - 1\right] \cong I_{S\_D1}\left[e^{\wedge}\left(\frac{V_{D1}}{\eta V_T}\right)\right]$$

Where:

$$V_T = \frac{kT}{q} \cong 26\ \text{mV @25}^{o}\text{C}$$

k = Boltzmann's constant
= 1.38×10^{-23} joules/5K
q = Electronic charge
= 1.6×10^{-19} coulombs
T = Absolute temperature (Kelvin)

Leakage Region

The leakage or reverse bias region is defined when voltage V_D is between 0 V and the breakdown voltage (V_{BR}). Currents I_F and I_R are small in comparison to I_L because diodes D_1 and D_2 are reverse biased; thus, the leakage current can be approximated by V_D/R_L.

$$I_D = I_F + I_L + I_R$$

$$= I_{S\_D1} + \frac{V_D}{R_L} + I_{S\_D2}$$

$$I_F \,\&\, I_R << I_L$$

$$\therefore I_D \cong \frac{V_D}{R_l}$$

Breakdown Region

The breakdown region is modeled by EV_1, D_2 and R_Z. Current flows through this path when the voltage exceeds EV_1 plus the forward voltage of D_2. Breakdown voltage V_{BR} is specified at test current I_T and is equal to the product of I_{BV} and R_{BV}. D_3 is used to compensating for the voltage drop of D_2. The clamping voltage (V_C), specified at current I_{PP}, is equal to the sum of the voltages of EV_1, R_Z and D_2 as shown below.

$$I_D \cong I_S \left[e^{\wedge} \left(\frac{V_D}{\eta V_T} \right) \right] \quad \therefore V_D \cong \eta V_T \left[\ln \left(\frac{I_D}{I_S} \right) \right]$$

$$V_C @ I_{PP} = V_{EV1} + V_{D2} + V_{RZ}$$
$$= \left[V_{BR} - \eta_3 V_T \ln \left(\frac{I_T}{I_{S3}} \right) \right] + \eta_2 V_T \ln \left(\frac{I_{PP}}{I_{S2}} \right)$$
$$+ (I_{PP} R_Z)$$

$$V_{EV1} = V_{BR} = V_D @ I_T = I_{BV} R_{BV}$$

Impedance Characteristics

The TVS diode impedance consists of an inductive, capacitive and resistive term. Modeling the inductance ensures that the magnitude of the overshoot pulse due to the inductance (V = L (ΔI/Δt)) of the IC package is simulated. Matching the capacitance helps to predict the shape of the clamped waveform. Including an accurate resistance term is important to predict the power capability of the device.

AC Model

The impedance of a TVS diode can be measured using a network analyzer. The real and imaginary portions of the measured impedance are then used to provide an equivalent small signal or AC model. The AC model consists of a resistor (R_S), inductor (L_S) and capacitor (C_S) connected in series. R_S is equal to the real portion of the complex impedance and is measured at the resonant frequency (f_R). At f_R, the impedance is purely resistive because the impedance of L_S and C_S are equal in magnitude but opposite in polarity. C_S is typically obtained by measuring the capacitance at 1.0 MHz. L_S is obtained from the resonant frequency, which corresponds to the minimum impedance. Table 1 shows how the AC model impedance terms are integrated into the SPICE macro-model. The design equations for the AC model are listed below.

$$Z_R = R; \quad Z_C = \frac{-j}{\omega C}; \quad Z_L = \omega L; \quad \omega = 2\pi f$$

$$Z = R_{eqv.} + jX_{eqv.}$$

$$Z = \sqrt{R_{eqv.}^2 + X_{eqv.}^2}$$

$$= \sqrt{R_S^2 + \left(2\pi f L_S - \frac{1}{2\pi f C_S} \right)^2}$$

$$@ f_R \; |Z_L| = |Z_C|$$
$$= R_S \Rightarrow @ f_R; \quad Z = Z_{Min.} = R_S$$

$$C_S \Rightarrow @ \text{ 1 MHz} \quad Z_{CS} >> \text{ ZsubLS} \quad \therefore C_S \cong \frac{1}{2\pi f Z}$$

$$L_S \Rightarrow f_R = \frac{1}{2\pi \sqrt{L_S C_S}} \quad \therefore L_S = \frac{1}{4\pi^2 f_R^2 C_S}$$

Table 1. CORRELATION OF THE AC AND MACRO-MODEL COMPONENTS

AC Model Component	Equivalent Macro-Model Component	Comments
R_S	$R_Z + D_{2\_RS}$	• Typically D_{2_RS} = 0; thus, $R_S = R_Z$ • $R_Z \propto$ clamping voltage V_C • $R_Z \propto$ 1/power rating
L_S	L	• L produces a short overshoot pulse due to V = L (ΔI/Δt)
C_S	D_{1_CJ0}	• D_{1_CJ0} is specified at a 0 V and decreases as the reverse bias voltage increases

Measured Test versus AC Model Impedance Data

Figures 3 and 4 show the impedance of the 1SMB28A and NUP2105. A TVS diode's impedance is a function of the bias voltage, as shown in Figure 3. Also, the capacitance decreases if the DC bias voltage increases, which produces a higher resonant frequency (f_R). A TVS diode can be modeled as a capacitor at relatively low frequencies; however, the inductance of the IC package must be included as the frequency approaches the resonant frequency. Table 2 provides a summary of the measured impedance and the AC model parameters for the 1SMB28A and NUP2105.

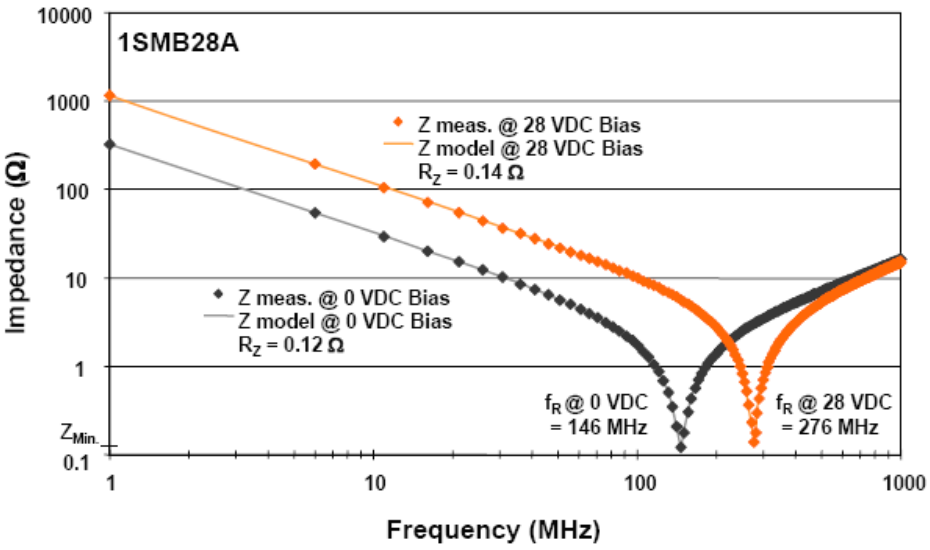


Figure 3. Impedance Characteristic of the 1SMB28A Unidirectional TVS Diode

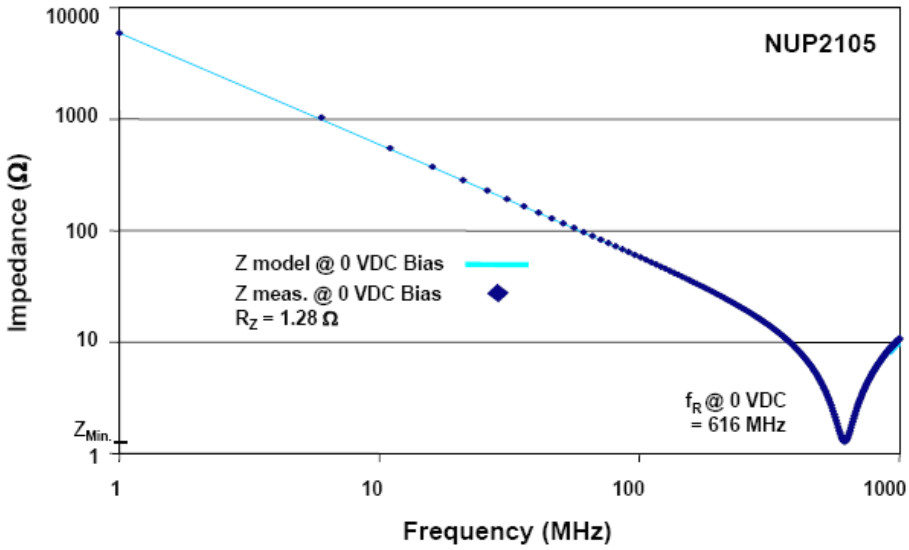


Figure 4. Impedance Characteristic of the NUP2105 Bidirectional TVS Diode

Resistance

The real or resistive portion of the impedance is modeled by R_S in the AC model and R_Z in the SPICE model. Resistance is a key factor in determining the power rating of the device and is a function of the method used to attach the IC package leads to the silicon die. The relatively large pad size of a SMB lead produces a large contact area at the lead-to-silicon connection that reduces the resistance. In addition, the large lead size of the SMB lowers the thermal resistance and increases the amount of thermal energy that can be dissipated through the leads onto the mounting pads of the PCB. In comparison, a SOT−23's lead-to-silicon connection has a relatively high resistance compared to a SMB device.

The high energy of a surge pulse can increase the TVS diode's junction temperature to a value that can be an order of magnitude larger than the ambient temperature. TVS diodes are designed to withstand high junction temperatures; however, the breakdown voltage (V_{BR}) and resistance are increased to a value higher than their nominal values. One option to simulate a high die temperature is to increase the macro-model's R_Z value so that the simulated clamping voltage matches the bench test value at a specific pulse, such as either the 8 × 20 μs or 10 × 1000 μs surge tests. Increasing R_Z raises the simulated minimum impedance ($Z_{Min.}$) as shown in Figure 5, but does not change the resonant frequency.

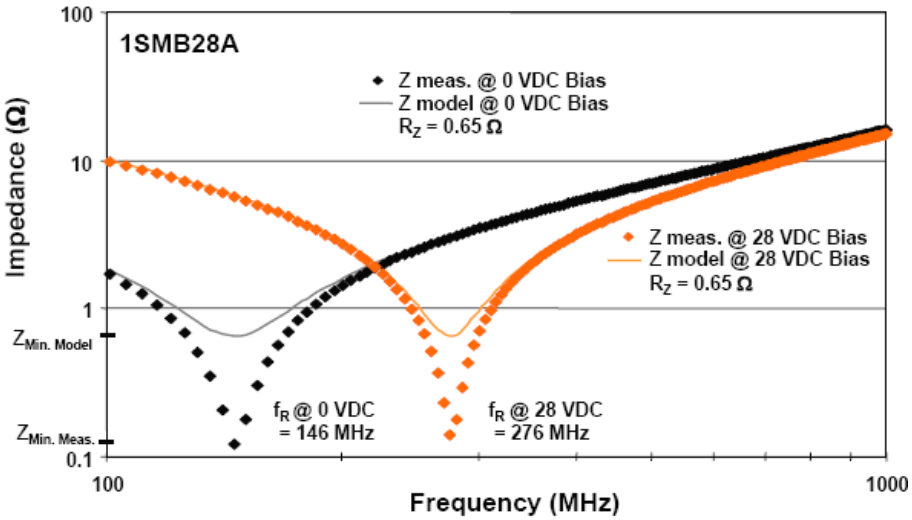
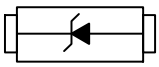
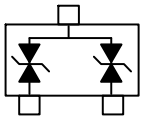


Figure 5. The Increase in the 1SMA28A's Junction Temperature Produced by a High Energy Surge Pulse can be Modeled by Increasing the Magnitude of R_Z from the Nominal Value of 0.1 to 0.65 Ω

Capacitance and Inductance

The capacitance (C_S) and inductance (L_S) form the imaginary or reactance portion of the TVS diode's impedance. The capacitance is proportional to the size of the silicon junction area. The SMB device houses a larger die than a SOT−23; thus, a SMB device will typically have a lower resonant frequency than a SOT−23 device. In addition, a bidirectional diode has a capacitance that is equal to half of the capacitance of an equivalent unidirectional device. Bidirectional diodes are created from two series connected unidirectional diodes; thus, the capacitance is lower than a unidirectional device. The inductance term is produced by the bonding connection between the package lead and the silicon die. The magnitude of L_S is similar for the 1SMB28A and NUP2105 TVS diodes.

Table 2. THE SMALL R_S AND LARGE C_S TERMS OF THE 1SMB28A ACCOUNT FOR THE DEVICES HIGH POWER RATING. THE SMALL CAPACITANCE OF THE NUP2105 RESULTS IN A HIGH RESONANT FREQUENCY

Part Number	Package and Schematic	Power Rating	f_R (MHz)	Bias Voltage	AC Model (R_S L_S C_S)		
					R_S (Ω)	L_S (nH)	C_S (pF)
1SMB28A	SMB 	600 W (10 × 1000 μs)	146	0 Vdc	0.12	2.44	486
			276	28 Vdc	0.14	2.44	137
NUP2105	SOT−23 	350 W (8 × 20 μs)	616	0 Vdc	1.28	2.48	26.4

Simulation Test Results

The clamping performance of the 1SMB28A TVS diode for the 10 × 1000 μs surge test is shown in Figure 6. The SPICE simulation used a R_Z value of 0.65 Ω, instead of the 0.1 Ω resistance measured with the network analyzer. The larger resistance results in an accurate clamping voltage (V_C) for high energy surges, but will simulate a V_C that is larger than a bench measurement for relatively low energy pulses. Future enhancements of the macro-model will include the integration of a thermal model to simulate the increase in the TVS device's junction temperature due to self heating.

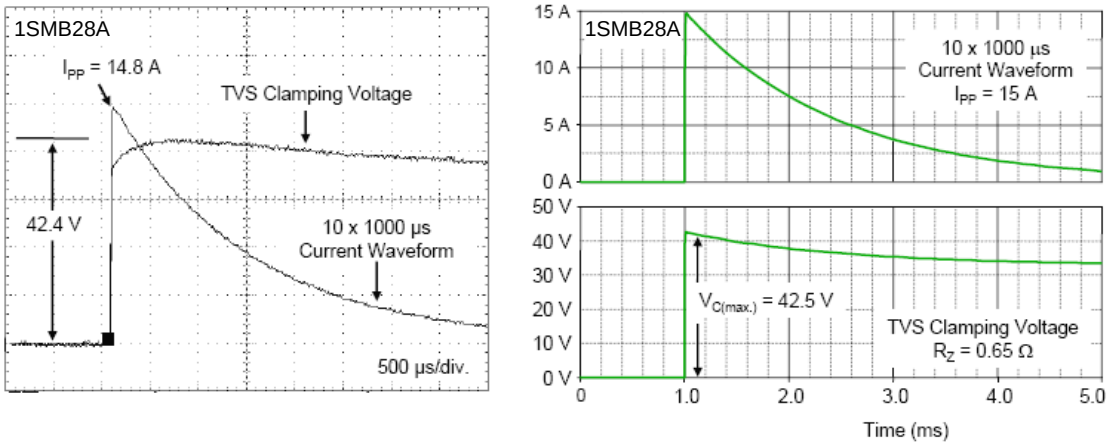


Figure 6. SPICE Predicts a Maximum Clamping Voltage of 42.5 V if R_Z is equal to 0.65 Ω. The Bench Test Value is 42.4 V

Figure 7 shows the clamping performance of the NUP2105 TVS diode for the 8 × 20 μs surge test. The macro-model used a R_Z value of 1.28 Ω that was determined from the AC model. The simulated V_C is relatively close to the measured value because of the shorter duration of the 8 × 20 μs surge in comparison with the 10 × 1000 μs pulse.

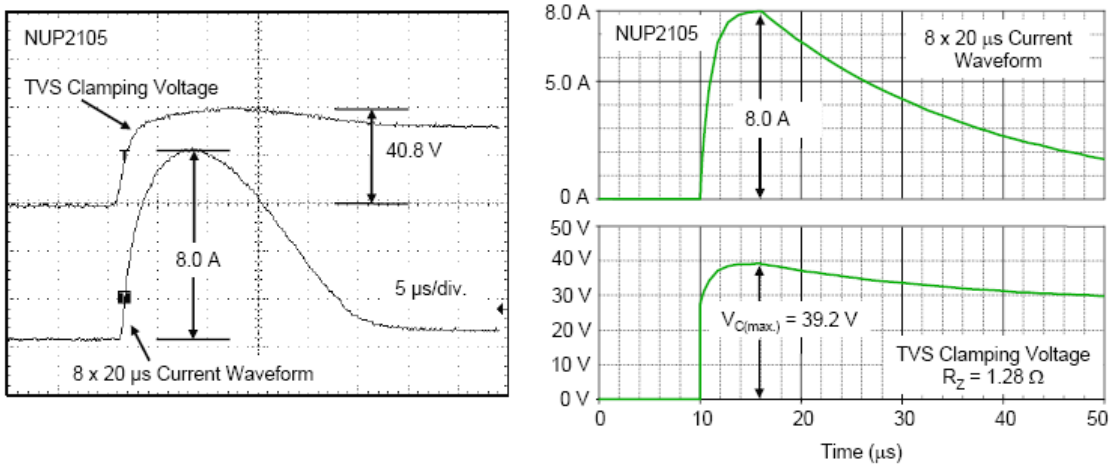


Figure 7. SPICE Predicts a Maximum Clamping Voltage of 39.2 V. The Bench Test Measured Value is 40.8 V

SPICE Limitations

Macro-models provide an accurate SPICE representation of the TVS avalanche diode's current and voltage characteristics for most applications. SPICE serves as a powerful design tool to analyze surge suppression circuits; however, simulation should not be used as a replacement for hardware development tests. A summary of the limitations of the macro-models is shown in Table 3.

Table 3. SIMULATION LIMITS OF TVS DIODE MACRO-MODELS

Region	Key Design Parameter	Limitation
Forward	Forward Voltage (V_F)	• V_F is typically specified as a maximum value at a single current point in the data sheet • The accuracy is enhanced if two typical test points are used
Leakage	Leakage Current (I_L)	• I_L is modeled as a linear function of the bias voltage • Measured I_L data varies as an exponential function of the bias voltage
Breakdown	Clamping Voltage (V_C)	• ΔV_C due to self heating is not modeled • Overcurrent failures are not modeled

References

[1] Bley, M., Filho, M. and Raizer, A., Modeling Transient Discharge Suppressors", *IEEE Potentials*, August/September 2004.

[2] Hageman, S., "Model Transient Voltage Suppression Diodes", *MicroSim Application Notes*, 1997.

[3] Lepkowski, J., "AND8250 − Zener Macro-Models Provide Accurate SPICE Simulations", ON Semiconductor, 2005.

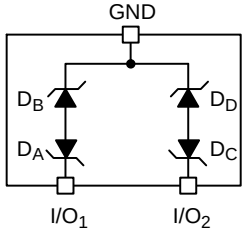
[4] Wong, S.; Hu, C. and Chan, S., "SPICE Macro-Model for the Simulation of Zener Diode Current-Voltage Characteristics", *International Journal of Electronics, Volume 71, No. 24*, August, 1991.

APPENDIX I: MACRO-MODEL SPICE NETLISTS

1SMB28A Macro-Model

```
**************************************************************************************
*       1SMB28A PSPICE macro-model
*       Uni-directional TVS avalanche diode, SMB package, V_BR = 32.75 V
**************************************************************************************
*                       Anode   Cathode
.SUBCKT SMB28A      7           1
**************************************************************************************
*       Forward Region
*       D1's CJO term models the capacitance
D1 2 1 MDD1
.MODEL MDD1 D IS = 1.83708e−14  N = 1  XTI = 1  RS = 0.2
+ CJO = 486e−12 TT = 5e−10
**************************************************************************************
*       Leakage Region
*       RL models leakage current (I_L)
*       MDR temp. coef. model ΔI_L/ΔT
RL 1 2 MDR 5.64e+06
.MODEL MDR RES TC1 = 0  TC2 = 0
**************************************************************************************
*       Reverse Breakdown Region
*       RZ models the ΔI/ΔV slope
*       The small signal impedance is equal to 0.1 Ω
*       A RZ value of 0.65 Ω matches the clamping voltage at max. current
*       Increasing RZ models the self-heating from the energy of a surge event
RZ 2 3 0.65
D2 4 3 MDD2
.MODEL MDD2 D IS = 2.5e−15  N = 0.5
*       Breakdown Voltage (V_BR) = I_BV × R_BV
EV1 1 4 6 8 1
IBV 0 6 0.001
RBV 6 0 MDRBV 32750
*       MDRBV temp. coef. model ΔV_BR/ΔT
.MODEL MDRBV RES TC1 = 0.00098
D3 8 0 MDD2
IT 0 8 0.001
**************************************************************************************
*       L models the lead-to-silicon connection package inductance
L 7 2 2.44e−9
*
.ENDS SMB28A
**************************************************************************************
```

NUP2105 Macro-Model



NUP2105
Dual Line Bi-directional TVS Diodes
SOT−23 Package

```
**************************************************************************************
**************************************************************************************
*       NUP2105 PSPICE macro-model
*       Bi-directional TVS avalanche diode, SOT−23 package, V_BR = 26.4 V
*       Model simulates 1 of the 2 I/O lines
**************************************************************************************
```

```
*                    DA Cathode  DB Cathode   DA,B Common Anode
.SUBCKT NUP2105   1            2              3
*       Bidirectional devices are formed from two uni-directional devices
X1      3          1          HALFNUP2105
X2      3          2          HALFNUP2105
.ENDS NUP2105
********************************************************************************
*       Model HALFNUP2105 represents one bi-directional pair of a dual device
*                              Anode      Cathode
.SUBCKT HALFNUP2105          7              1
*       Forward Region
*       D1's CJO term models the capacitance
D1 2 1 MDD1
.MODEL MDD1 D IS = 1.83708e−14  N = 1  XTI = 1  RS = 0.2
+ CJO = 26.4e−12  TT = 1e−08
********************************************************************************
*       Leakage Region
*       RL models leakage current (IL)
*       MDR temp. coef. model ΔIL/ΔT
RL 1 2 MDR 4.32244e+08
.MODEL MDR RES TC1=0 TC2=0
********************************************************************************
*       Reverse Breakdown Region
*       RZ models the ΔI/ΔV slope
RZ 2 3 1.28
D2 4 3 MDD2
.MODEL MDD2 D IS = 2.5e−15  N = 0.5
*       Breakdown Voltage (VBR) = IBV × RBV
EV1 1 4 6 8 1
IBV 0 6 0.001
RBV 6 0 MDRBV 26357.1
*       MDRBV temp. coef. model ΔVBR/ΔT
.MODEL MDRBV RES TC1 = 0.00096
D3 8 0 MDD2
IT 0 8 0.001
********************************************************************************
*       L models the lead-to-silicon connection package inductance
*       L is distributed between two diodes for bi-directional diodes
L 7 2 1.24e−9
*
.ENDS halfnup2105
********************************************************************************
********************************************************************************
```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