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Application Note 7525

PCB Land Pattern Design and Surface Mount Guidelines for MicroFET™ Packages

Scott Pearson (Fairchild Semiconductor), Jim Benson (Intersil Corporation)

Introduction

Fairchild's MicroFET™ package is a relatively new packaging concept that is currently experiencing rapid acceptance. It offers a variety of benefits including reduced lead inductance, a small sized "near chip scale" footprint, thin profile, and low weight. Its use of an exposed copper die-pad technology (Figure 2) offers good thermal and electrical performance. These features make the MicroFET™ an ideal choice for many new applications where size, weight, thermal and electrical performance are important.

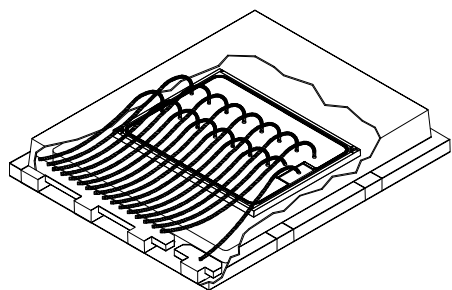


Figure 1. 3D Cutaway of 8 pin MicroFET™

There are general industry references, such as IPC-SM-782, for printed circuit board (PCB) land pattern design. But because the MicroFET™ package style is relatively new, such industry guidelines for it are still in development. This Application Note provides general guidelines for use in developing land pattern layouts and solder mounting processes.

It should be emphasized that these guidelines are general in nature and should only be considered a starting point in this effort. The user must apply their actual experiences and development efforts to optimize designs and processes for their manufacturing practices and the needs of varying end-use applications.

MicroFET™ Package Outline Drawings

Fairchild's individual product data sheets reference the appropriate Fairchild package outline drawings. These in turn reference compliance to any applicable industry standard outlines. For MicroFET™ packages, the JEDEC MO-220 outline series generally applies. The MicroFET™ dimensions used in the land pattern design can be taken from these drawings.

General Design Guidelines

The MicroFET™ die pad and perimeter I/O pads are fabricated from a planar copper lead-frame substrate. This is encapsulated in plastic with the bottom of the die pad and I/O pads exposed to create a very small footprint "exposed-pad" package. Both the I/O pads and die pad should be soldered to the PCB.

The corresponding PCB lands need to be designed to fit well within the PCB assembly process capabilities, as well as promote good long term solder joint reliability. Note that the process of soldering the exposed die pad "anchors" the package and provides important thermo-mechanical temperature cycling stress benefits that improve the reliability of the I/O pad solder joints.

The PCB "thermal land" design for the exposed die pad should include thermal vias that drop down and connect to buried metal plane(s). This combination of vias for vertical heat escape and buried planes for heat spreading allows the MicroFET™ to achieve its full thermal potential.

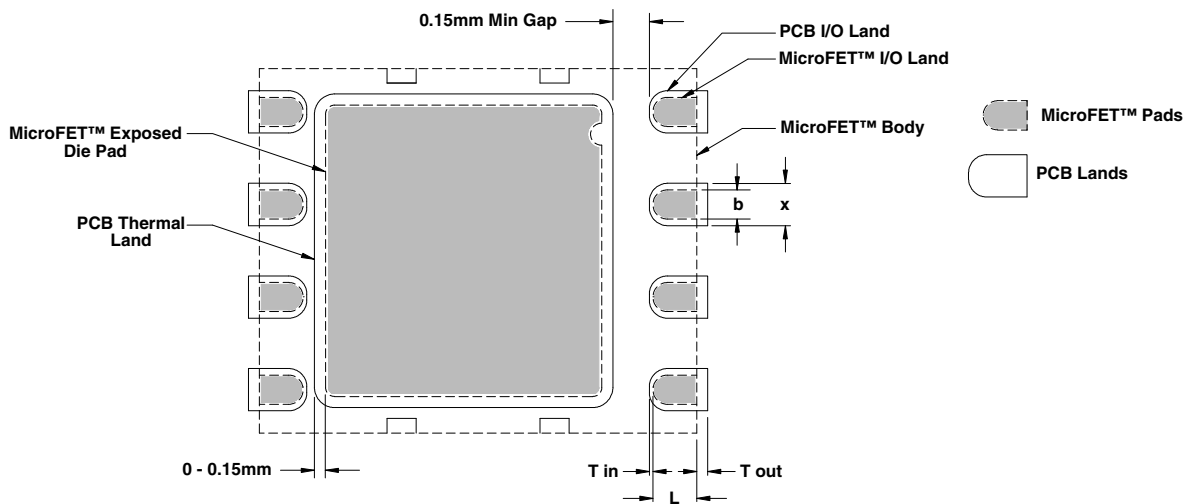


Figure 2. Typical MicroFET™ Land Pattern Layout with Package Overlay

Land Pattern Guidelines

Peripheral I/O Lands

The I/O lands should be a little larger on all sides than the package's I/O pads. Inward corners may be rounded to match the I/O pad shape. Design dimension guidelines are shown in Table 1. Typical package I/O pad dimensions are shown for reference only; and it should be noted that package outline drawings are the controlling specification for such package dimensions.

Table 1. Typical Pad and Land Dimension

Typical Nominal Package I/O Pad Dimensions (mm)			I/O Land "Design Dimension" Guidelines (mm)		
Pad Pitch	Pad Width (b)	Pad Length (L)	Land Width (X)	Outward Extension (T _{out})	Inward Extension (T _{in})
1.27	0.40	0.6	0.49 Nom	0.15 Min	0.05 Min
0.8	0.33	0.6	0.42 Nom	0.15 Min	0.05 Min
0.65	0.28	0.6	0.37 Nom	0.15 Min	0.05 Min
0.5	0.23	0.6	0.28 Nom	0.15 Min	0.05 Min
0.5	0.23	0.4	0.28 Nom	0.15 Min	0.05 Min
0.4	0.20	0.6	0.25 Nom	0.15 Min	0.05 Min
0.4	0.20	0.4	0.25 Nom	0.15 Min	0.05 Min

With available PCB area, the outward extension (T_{out}) can be increased beyond 0.15mm as this could potentially improve this external solder joint. Any increase in the inward extension (T_{in}) above 0.05mm must consider the effect on the isolation gap to the thermal land.

PCB Thermal Land

The thermal land should be designed 0 to 0.15mm larger per side (0 to 0.30mm larger overall) than the package's exposed die pad. "Larger than", as opposed to the same size, is preferred.

But for package designs with die pad sizes near the maximum available for that package, whether or not the thermal land should be designed larger, or by how much, depends on your requirement for the isolation gap to the I/O lands. The recommended design gap is 0.15mm minimum. When space is available, a gap of 0.25mm or more is preferred. Don't make the thermal land so large that your desired gap is compromised.

Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drop down and connect to buried copper plane(s), should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter, with the barrel plated to about 1.0 ounce copper.

Although adding more vias (such as by decreasing via pitch) will improve thermal performance, diminishing returns will be seen as more and more vias are added. Therefore, simply use as many vias as practical for the thermal land size and your board design groundrules.

Solder Mask Design

Two types of land patterns are used for surface mount packages:

- 1) Solder Mask Defined (SMD): Solder mask openings smaller than metal pads.
- 2) Non-Solder Mask Defined (NSMD): Solder mask openings larger than metal pads.

Better control of the copper etching process as compared to the solder masking process makes NSMD preferable. Also, the SMD pad definition can introduce stress concentrations near the solder mask overlap region that can result in solder joints cracking under extreme fatigue conditions. Using NSMD instead improves the reliability of solder joints as solder is allowed to "wrap around" the sides of the metal pads on the board.

For these reasons, NSMD is recommended for the perimeter I/O lands and generally for the thermal land; however SMD should be used on the thermal land when it is relatively large as discussed below.

For NSMD pads, the solder mask opening should be about 120 μ m to 150 μ m larger than the pad size, providing a 60 μ m to 75 μ m design clearance between the copper pad and solder mask. Rounded portions of package pads should have a matching rounded solder mask-opening shape, especially at corner leads to allow for enough solder mask web to prevent solder bridging.

Typically each pad on the PCB should have its own solder mask opening with a web of solder mask between adjacent pads. However for 0.4mm pitch parts with an I/O land width of about 0.25mm, space may not be available for solder mask web in between the pads. In that case, use one big opening designed around a whole strip of pads (for instance all the pads on one side of a package) with no solder mask in between the pads.

For package designs with exposed die pad sizes near the maximum available for that package, the gap between the thermal land and I/O pads may be small. In this case there may be more potential for solder bridging, so the thermal land should be solder mask defined (SMD). The mask opening should be approximately 100 μ m smaller than the thermal land on all four sides, which increases the solder mask web between the thermal and I/O lands.

Solder masking is also required for thermal vias to prevent solder wicking inside the vias, drawing solder away from the thermal land-to-die pad interface. The solder mask diameter should be about 100 μ m larger than the via diameter. The vias can be plugged or tented with solder mask, either from the bottom or top surface of the PCB. Tenting from the top is considered a better option as it results in smaller voids under the die pad. Solder masking of vias from the bottom side can result in increased outgassing during reflow, creating bigger voids around vias. But note that small voids in this area are not unusual and will have little effect on thermal or electrical performance or on the reliability of the perimeter I/O pad solder joints.

Stencil Guidelines

Stencil Design for I/O Lands

Re-flowed solder joints on the perimeter I/O lands should have about a 50 μ m to 75 μ m (2 to 3 mil) standoff height and a good-sized fillet on the outside. The solder paste stencil design is the first step in developing such optimized, reliable joints.

Stencil aperture size-to-land size should typically be a 1:1 ratio. For finer pitch parts, especially as tight as 0.4mm, the aperture width may need to be reduced slightly to help prevent solder bridging between adjacent I/O lands.

Stencil Design for Thermal Land

To reduce solder paste volume on the thermal land, it is recommended that an array of smaller apertures be used instead of one large aperture. The smaller apertures can be circular or square and of various dimensions and array sizes; but the main goal should be a dimensional combination that results in 50 to 80% solder paste coverage. This reduced coverage on the thermal land is important in achieving good solder joints at the perimeter I/O lands.

Stencil Type and Thickness

A laser-cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing "smooths" aperture walls, resulting in reduced surface friction, good paste release and void reduction. Using a trapezoidal section aperture (TSA) promotes paste release and also forms "brick-like" paste deposits that assist in firm component placement.

A 0.125mm stencil thickness is recommended for finer pitch packages (0.5mm and smaller), and this may be increased to 0.15mm to 0.2mm thickness for greater than 0.5mm pitch packages.

Solder Paste and Reflow Profile

Due to the low mounted height of the MicroFET™, "No Clean" Type 3 paste per ANSI/J-STD-005 is recommended. Nitrogen purge is also recommended during reflow.

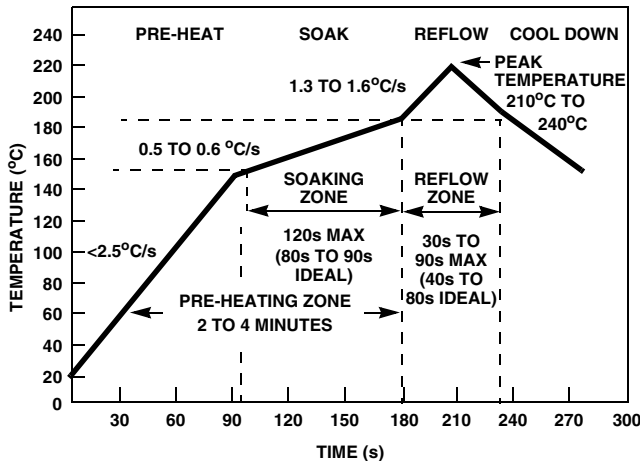


Figure 3. Typical Lead-Tin Solder Reflow Profile

Removal and rework of MicroFET™ packages can be a challenge due to their small size and since they are commonly mounted on smaller, thinner, and denser PCBs. The following steps are provided as a guideline – a starting point in developing a successful rework process.

Bake

Before rework, bake the PCB assembly at 125C for at least 4 hours to remove any residual moisture.

A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the MicroFET™. The following profile is provided as a guideline, to be customized for varying manufacturing practices and applications.

Rework Guidelines

After PCB assembly, the package should be inspected in transmission x-ray for the presence of voids, solder balling, or other defects underneath the package. Cross sectioning may also be required to determine the fillet shape and size, and the joint standoff height. In a MicroFET™, only the external side-fillet solder joint is exposed and any retouch is limited to this area. For rework of defects underneath the package, the whole package needs to be removed.

Component Removal

Ideally, the reflow profile for part removal should be similar to that used for part attachment. However, the time above liquidus can be reduced as long as the reflow is complete.

It is recommended that the board be heated from the bottom side using convective heaters and from the top side with hot gas nozzles directing heat at the component to be removed. Heating of adjacent components should be minimized. The MicroFET™ is small and light, so avoid excessive flow.

Once the joints have reflowed, remove the MicroFET™ with a vacuum lift-off. Because of the small package size, the vacuum pressure should be kept below 15" of Hg to help prevent premature lift-off (and possible PCB damage) before all joints have fully reflowed.

Site Redress

Clean the site properly, removing residual solder with a combination of a blade-style conductive tool and desoldering braid. After residual solder removal clean the lands with a solvent specific to the type of paste used in the original assembly.

Solder Paste Printing

Use a miniature stencil specific to the component and align the stencil aperture under appropriate magnification (~50 to 100X). Lower the stencil onto the PCB and deposit the paste with a small squeegee blade. The blade width should be the same as the package width to ensure single pass paste deposition, avoiding any overprinting.

Component Placement and Reflow

Due to its small mass, the MicroFET™ has good self-centering abilities during solder reflow, so the placement of this package should be similar to that of BGAs. The placement machine should have fine adjustment capability in the x, y, and rotational axes. Since the pads are on the underside of the package, use an optical system that can overlay an image of the solder paste pattern to aid in component alignment, which should be done at 50 to 100X magnification. Reflow the PCB using the same profile as that developed for the initial attachment.

Acknowledgements

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