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Designing with TTL

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54/74 series TTL has been used for more than a decade with excellent results, and continues to be a standard choice for design engineers because of the wide performance range and system optimization possible from the different families available. 54/74 logic comes in 8 different speed/power families (standard TTL, LS, S, ALS, AS, L, and F) that allow a design engineer to select device performance to suit his needs. Understanding the differences and the general limitations of all these families will go a long way toward insuring that a system will operate as intended with the minimum of corrections and redesigning.

FAMILY COMPATIBILITY: Intermixing Logic Types in One Design

Family interchangeability is a beneficial characteristic of the different TTL families and provides the designer with the ability to customize specific areas of his design in order to accomplish the task of achieving both high performance and the lowest power consumption possible. However, interchangeability is not simply a matter of replacing, say, an S00 for an LS00 to improve the speed and replacing an LS00 for an S00 for power savings. One must also look at the DC and AC characteristics to insure that the replacement device will be compatible with the existing circuit. The DC problems include input loading and compatible output drive capabilities. The AC problems include insuring that the new device speeds will be acceptable to the rest of the system. The different logic families also generate different amounts of noise and have different noise immunity. Finally, measure points for the AC parameters of the different families, although very similar, do vary some, and this will require attention.

SUPPLY RAILS: Why Not to Exceed the Specs

All bipolar logic (both junction and oxide isolated) is made up of selectively located regions of differently doped materials that form transistors, resistors, and diodes. Because of this, certain overall requirements are necessary to insure that the IC will be able to perform its task without interference from its environment. The first characteristic of bipolar devices is that the two power rails (V_{CC} and ground) represent the two voltage extremes that should be used in any system. Certain exceptions exist, primarily inputs and open-collector outputs that are pulled up to higher voltages than V_{CC}. However, while it is occasionally permissible to exceed the V_{CC} specification, it is never permissible to drive any input or output more than 0.5V below the ground reference. This limitation is due to the method used to electrically isolate the many circuit elements that are present on a bipolar IC. Oxide isolated devices use an oxide layer surrounding the various transistor and resistor tanks to provide an insulating barrier, while the original junction isolated devices use reverse biased PN junctions to provide that barrier. In both cases, the circuit is built on a P-type substrate that uses reverse biased PN junctions to separate the different circuit elements. The ground pin is electrically connected to the substrate and must be the most negative voltage on the device. When an input or output pin is taken below ground, the normally reverse biased isolation regions between the elements become forward biased and electrically connect these elements together, thus eliminating the integrity of the circuit. This may or may not result in actual damage to the device depending upon the magnitude of the violating signal and the specifics of the device being violated. This holds true for both junction and oxide isolated logic. Oxide isolated logic may provide more margin before failing (thereby "working" in some marginal designs), but it is nevertheless subject to the same kind of limitations as junction isolated logic.

IMPROPER GROUNDING: Noise Immunity, Floating Grounds

Bipolar logic uses the ground rail as the signal reference. Consequently, any modulation on the ground line will be directly added to the signal voltage. The logic "0" input noise margin is guaranteed as the difference between the V_{OL} and V_{IL} specification, and the logical "1" input noise margin is guaranteed as the difference between the V_{OH} and V_{IH} specification. This noise margin is intended to be protection against a reasonable amount of noise present. Insufficient grounding techniques can cause significant I_R and I_L drops on the ground line between two ICs and result in a "floating" ground line. This is due to the large currents that are present on ground and V_{CC} during high speed switching and means that the two devices are not using the same reference point. Any voltage drop in the ground line is added to the signal and ends up consuming some of the noise margin. Eventually, the mismatch caused by the floating ground will exceed the total noise margin and cause erroneous data to propagate through the system. The solutions to this problem are many and varied, but all of them revolve around improving the system grounding and include such ideas as providing separate signal and power grounds.

V_{CC} NOISE AND DECOUPLING: Providing Clean Power

The V_{CC} power rail is also susceptible to both I_R and I_L voltage drops. The problems that arise from the V_{CC} line are not the same as the problems that arise from the ground line. Since the V_{OH} level tracks the V_{CC} almost exactly, any voltage loss on the V_{CC} line is directly transferred to the V_{OH} level. However, the noise margin for the logic high state is typically 700 mV for commercial and 500 mV for military product, versus 400 mV and 300 mV for commercial and military product, respectively, for the logic low level. The main consequences of a drooping V_{CC} line now become I_{OL}/I_{OH} drive capability, and the AC performance in critical applications. Although bipolar devices are only guaranteed to operate over a given V_{CC} range (5V ± 10%), these devices typically function to V_{CC} values as low as 4V. Be aware that if the device does indeed function down to 4V, the AC and DC characteristics will be compromised, some quite severely.

Designing in a good power distribution system will insure that all the devices in the circuit will perform the same, regardless of their physical location. Properly decoupling the V_{CC} against both high and low frequency noise will help eliminate any problems with individual device operation.

High frequency noise (100 MHz and above) comes primarily from two sources, while low frequency noise (less than 25 MHz) results from primarily one source.

SOURCES OF HIGH FREQUENCY NOISE ON THE V_{CC} LINE

1) High frequency noise results from the device rapidly switching logic levels. The bulk of the switching current from a low to high transitions shows up in I_{CC} current surges, while the bulk of the switching current from a high to low transition shows up in ground current surges.

2) Noise is transmitted through the changing magnetic fields that result from the changing electric fields in a switching line and are picked up on adjacent signal paths.

Note that the frequency causing the noise is not the signal's frequency, but the frequency of the signal's slew rate. For instance, in an S00 that is switching 0V to 3V at 1 MHz, the slew rate of the output is typically about 1 ns/V, which is a frequency of around 160 MHz. The faster the slew rate, the higher the frequency, until one has an ideal square wave with infinite frequency. It is this frequency component that gives rise to the strong magnetic fields associated with switching bipolar devices.

SOURCES OF LOW FREQUENCY NOISE ON THE V_{CC} LINE

1) Low frequency noise results from the change in the I_{CC} current demand as devices change state. For instance, gates, flip-flops, and registers will draw different I_{CC} currents, depending upon the state of the outputs.

The most commonly used method for countering these noise problems is to decouple the V_{CC} line. With this approach, capacitors are used to stabilize the V_{CC} line and filter out the unwanted frequency components. A small value capacitor (i.e., 0.1 µF) is used near the device to insure that the transient currents arising from device switching and magnetic coupling are minimized. A large value capacitor (i.e., 50 µF to 100 µF) is used on the board in general to accommodate the continually changing I_{CC} requirements of the total V_{CC} bus line. The following table shows a rough "rule of thumb" approach to determining how many capacitors to use for a given number if ICs. Be aware that the table is not a hard and fast rule, and that you must always evaluate your particular application to insure that there is sufficient V_{CC} decoupling. When using these guidelines, be sure that the devices are located near each other and near the capacitor. If the capacitor is too far away, I_R and I_L drops will diminish the capacitor's effect. All capacitors (especially the 0.01 µFs) must be high frequency RF capacitors. Disk ceramics are acceptable for this application. Keep in mind that, in synchronous systems, since a majority of the devices will be switching at once, alter your power distribution system accordingly.

Device Family	Number of Capacitors
AS, S, ALS, LS, H	1 Cap per 1 device
TTL, L	1 Cap per 2 devices

TYING ALL UNUSED INPUTS TO A SOLID LOGIC LEVEL

Unused inputs on TTL devices float at threshold, anywhere from 1.1V to 1.5V, depending upon the device and its family. While this usually simulates a "high", many application problems can be traced to open inputs. Inputs floating at threshold are very susceptible to induced noise (transmitted from other lines) and can easily switch the state of the device. A good design rule is to tie unused inputs to a solid logic level. Inputs are usually tied to V_{CC} through a 1 kΩ to 5 kΩ resistor, since tying them to ground means supplying the I_{IL} current instead of the I_{IH} current. I_{IL} is several orders of magnitude greater than I_{IH}. The resistor is recommended to protect the input against V_{CC} voltage surges and to protect the system against the possibility of the input shorting directly to ground. A single 1k resistor can handle up to 10 inputs.

TERMINATIONS: Why Terminate a Transmission Line?

Whenever signals change voltage levels, a wavefront is created that propagates according to the characteristics of the transmission line being used. If the overall length of the signal path is short compared with the signal's wavelength (1/frequency), then none of the complications of transmission lines are present. However, if the length of the signal path is long in comparison, then the wavefront will be significantly affected by the geometry and composition of that transmission line.

Fortunately, when dealing with a single board layout, the distances are usually short enough that one need not worry about the difficulties of terminating or impedance matching the line. However, if one is driving between boards or over long distances, he must be aware of the characteristics involved. When dealing with transmission lines it is necessary to know the impedance of the line. Every time the signal wavefront encounters a discontinuity (a point where the impedance changes, whether from a branch, junction or because of a change of environment), the opportunity for reflections and standing waves is present. These waves can easily cause the loss of the signal's integrity, having the ability to build voltages that are large enough to destroy an IC. Proper line termination will insure that the signal propagates down the line and is totally absorbed at the receiving end, thus preventing these waves from occurring.

Listed below is a guideline to the types of transmission lines to use when sending signals over various distances.

0" to 12" Single wire conductor OK. Use point-to-point routing and avoid parallel routing if possible. Ground plane recommended, but not mandatory. Space conductors as far apart as possible to reduce line to line capacitance.

12" to 6' Dense ground plane required with wire routed as closely as possible. Twisted-pair lines or coaxial cable mandatory for clock lines and recommended for all sensitive control lines.

Over 6' Use fully terminated transmission lines. Avoid the use of radially distributed lines and avoid sharp bends in the line. Be aware that transmission lines have complex impedances and are not simply resistive in nature.

BUS DRIVERS: On Board vs Off Board

Many of the 3-STATE buffers and flip-flops are intended to connect directly to the system bus and must be able to drive heavily capacitive loads. Keeping this in mind, all of Fairchild's LS 3-STATE devices have "triple-sink" capability; that is, the I_{OL} and I_{OH} drive currents have been tripled. However, these devices are intended to drive single board buses. Driving off the board with these devices can easily lead to serious problems.

When using standard logic bus drivers on a single board, be aware that many of the octal and bus oriented devices have PNP inputs to reduce DC loading. PNP inputs on 54S/74S devices tend to be more capacitive than the corresponding diode or emitter inputs, and as such, compromise the AC loading of the bus. Careful attention must be given to both DC and AC loading when driving heavily loaded buses. PNP inputs on LS/AS/ALS operate at significantly lower currents and do not significantly increase capacitive load.

It is strongly recommended that any time a bus line leaves a board, interface bus drivers be used. These devices are specifically designed to impedance match different kinds of transmission lines and have the necessary current drive to handle the job. Using an ordinary logic device will usually yield poor results. If one must drive a transmission line with a logic device, there are some guidelines that should be followed to minimize the problems that can result.

1) Take care to properly terminate the bus. Be aware that every time a signal passes through a different impedance, an interface is created and that any impedance mismatch will result in reflections.

2) Never drive off the board with a bistable element like a flip-flop or a latch. This is because those devices are very susceptible to reflected waves changing their state. By buffering the output of the latch with another device, the reflected wave can affect the output of the buffer, but not the latch. This means that when the wave finally dies out, the latch will still have the proper data and the buffer will "snap back" to the proper output.

3) Be sure to carry an adequate ground plan with the signals and to shield the bus. Carrying a good ground plan (use multiple ground lines spaced around the connector if possible) will reduce the problem of floating ground, and the shielding will help protect the signal lines for induced noise. Using twisted-pair transmission lines for critical signals helps to eliminate the capacitive coupling that can degrade signals, or even cause false signals.

4) It is best to buffer any clock or control lines that depend upon fast, clean switching. Buffering at both the sending and receiving end will go a long way toward insuring that the clock can accomplish its goals.

5) Use the devices with Schmitt inputs to add to the noise margin of the receiving device. This will help increase the noise rejection of the system. Decouple each receiver separately, connecting the capacitor directly between ground and V_{CC}. Make sure that the device ground is tied directly to the bus ground.

6) If using open-collector devices to drive the bus, add a pull-up resistor on the input to the receiving device if the I_{OL} current of the driving device can handle it. A resistance in the 300Ω range will significantly improve the signal's rise time.

AC LOADING: What Do AC Loads Look Like, and Why?

The standard AC load for all of the logic families, except ALS and AS, is built around a diode chain to ground and a pull-up resistor to V_{CC} with added capacitance. This load is designed to look like the standard logic circuit input structure, and to simulate the appearance of switching in an actual application. For ALS and AS, the load is built around a resistor to ground and added capacitance. This is primarily for the requirements of high speed device testing. There also exists a set of standardized military AC loads that were designed to approximate the input structure, while using no switches for the 3-STATE parameters. Please see waveforms in this section. In the final analysis of these loads, it must be kept in mind that they represent a standard that can be used to determine the quality of an IC. No load will be able to predict exactly how a device will perform in a circuit or the speeds that a device can achieve in a good test jig with the spec load, as compared to the speeds that a device will produce in an application.

OPEN-COLLECTOR DEVICES: What They Are, How to Use Them

Open-collector devices are totem pole outputs where the upper output (usually a Darlington transistor) is left out of the circuit. As such, these devices have no active logic high drive and cannot be used to drive a line high. The advantage to open-collector devices is that a number of outputs can be directly tied together. If one were to tie two complete totem pole outputs together, then at some time one output would be driving high while the other output was driving low. The result is that one device will be dumping excessive current directly into the other device. The resulting power dissipation in both devices can easily degrade the lifetime of the device. Since open-collector devices only have active drive in one state, if two connected devices drive to opposite states, the low state will always predominate and there will be no degradation to either device. Open-collector specifications are obvious by the lack of a V_{OH} specification. The only V_{OH}/I_{OH} specification is the leakage limits, and these are specified at V_{OH} = 5.5V.

When dealing with open-collector devices, it must be noted that each output requires a resistive pull-up, usually tied to V_{CC}. (By using high voltage outputs, one can tie the resistor pull-up to a voltage higher than V_{CC}.) Designers often try to get away with tying the output to an input and relying on the I_{IL} current to pull up the output. This is unwise, as it is just like leaving inputs floating: the input is very susceptible to noise and can easily give false signals. Shown below are two equations that can be used to determine the min/max range of the pull-up resistor.

$$R_{MAX} = \frac{(V_{CC(MIN)} - V_{OH})}{(N1 \bullet I_{OH} + N2 \bullet I_{IH})}$$

$$R_{MIN} = \frac{(V_{CC(MIN)} - V_{OL})}{(I_{OL} - N2 \bullet I_{IL})}$$

where: N1 = the number of open-collector devices tied together,

N2 = the number of inputs being driven on the line.

If the maximum resistance is exceeded, then it is possible for the total leakage currents from all of the inputs and outputs to pull the V_{OH} level below the spec value. Likewise, if the R_{MIN} value is exceeded, then the driving device may not be able to pull down the signal line to a solid V_{OL}. Either of these two cases can easily result in false logic levels being propagated through the system.

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