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Physically Based, Scalable SPICE Modeling Methodologies for Modern Power Electronic Devices

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Physically Based, Scalable SPICE Modeling Methodologies for Modern Power Electronic Devices

Abstract

Efficient power electronic design hinges on the availability of accurate and predictive SPICE models. This paper proposes novel physical and scalable SPICE models for power electronic semiconductors including wide−bandgap devices. The models are based on process and layout parameters, enabling design optimization through a direct link between SPICE, physical design, and process technology. The models are used as key design components during technology development and for the proliferation of new products.

Introduction

Modern day power electronics encompass a wide spectrum of semiconductor device types, all of which present unique benefits and trade−offs in the design space. Such devices include trench IGBTs, Super−Junction MOSFETs, Trench MOSFETs, GaN HEMTs, SiC MOSFETs and SiC diodes. In order to realize all the various device benefits, efficient power module design hinges on the availability of accurate and predictive SPICE models. In a conventional industry reactionary modeling approach, devices are first designed and fabricated through a combination of time consuming TCAD and fabrication cycles. Once the device design is finalized and qualified, a SPICE model is extracted to the measured characteristics and subsequently made available for application simulation. A physical SPICE model that is sensitive to process parameter and layout perturbations breaks the reactionary cycle, enabling simulation as a key link in the device design process [1−3]. Such physical models stimulate cycle time reduction by bridging the gaps between TCAD, circuit design, and fabrication. Circuit designers can evaluate technologies early in the process development stages in simulation rather than through fabrication iterations.

Historically, power semiconductor models at the SPICE level have been based on simple subcircuit or behavioral models. Simple subcircuit models are often too rudimentary to adequately capture all the device performances such as current−voltage, capacitance−voltage, transient, and thermal behavior. More advanced behavioral models often do not contain direct links to the device layout and process parameters. For example, in recent models for SiC MOSFETs reported in [4−7], simple SPICE level 1 based MOSFET models are used for the channel and fixed linear resistors are used for the clearly nonlinear JFET like drift region. In addition, the all important C_{GD} capacitance is described through unphysical diode networks, empirical fitting functions, or table models as described in [8]. The models are not process and

layout based nor is the scalability apparent. More physical models were reported in [9, 10]. However these models also treat the nonlinear drift region with a linear resistor and the depletion pinching effects in the C_{GD} are not captured. Furthermore, the model in [9] is implemented in a specific simulator language, raising questions about the portability across multiple SPICE simulator platforms. The previous references are just for SiC MOSFET models. A similar situation exists on all power semiconductor device types. This paper advances the state−of−the−art through first time physical, scalable, and robust SPICE agnostic model for multiple power semiconductor devices. SiC MOSFET and Trench IGBT models will be covered in detail though the methods have been applied to a wide range of devices including Super−Junction [1], Trench MOSFET [2], and most recently GaN HEMT devices. Details regarding robust SPICE agnostic model generation is covered in section VI.

SiC MOSFET MODEL DESCRIPTION

Figure 1 illustrates a SiC MOSFET cross section and Figure 2 displays the corresponding SPICE sub−circuit rendition.

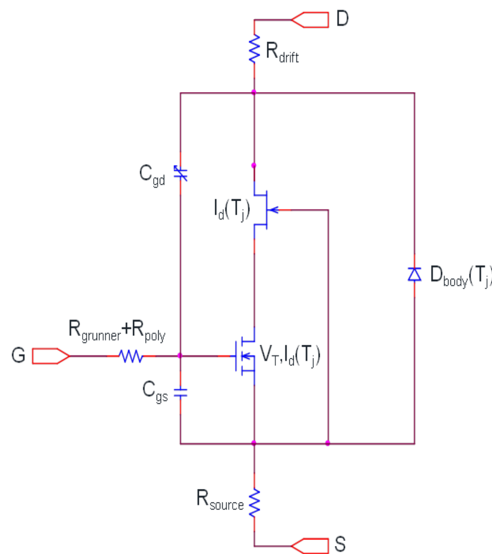

Figure 1. SiC MOSFET Subcircuit Model

Channel

The channel is described by the physically based bsim3v3 model capturing all relevant channel physics [11]. In particular, the transitions through subthreshold, weak inversion and strong inversion regions are captured accurately. The extracted mobility parameter U0 takes on low ranges 10–50 $cm^2/(V–s)$ typical of SiC channels, demonstrating the applicability of the model to SiC MOSFETs. Flexible temperature modeling is included which can be tuned to specific SiC MOSFET behavior. Furthermore, the widely available bsim3v3 model has excellent speed and convergence properties as compared to behavioral models.

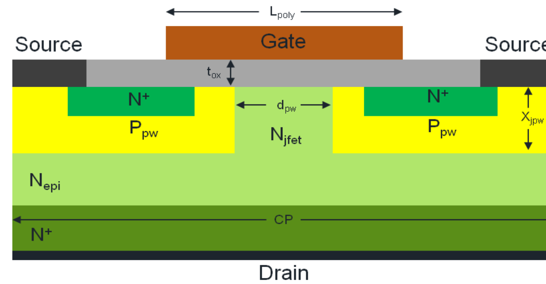

Figure 2. SiC MOSFET Cross Section

Epi–JFET

The epi region between the pwells is captured by the standard SPICE JFET model. Previously derived analytical models of JFET parameters [1] are modified for application to the SiC MOSFET JFET region. Similar to the bsim3v3 model, the spice JFET model is universally available, very fast and has excellent convergence properties. The JFET spice model parameters that capture the linear and nonlinear behavior of the drift region are the current gain factor beta and the threshold or pinch–off voltage vto. These parameters are used in the well known JFET current equations such as equation (1) of the triode region.

$$I_D = \beta \cdot [2 \cdot (V_{GS} - vto) - V_{DS}] \cdot V_{DS} \cdot (1 + \lambda \cdot V_{DS}) \qquad \text{(eq. 1)}$$

Analytical models of the JFET gain (beta) and pinch–off (vto) parameters for the SiC MOSFET have been derived as functions of the physical process and layout parameters using the standard equations for JFET depletion width. Finding the point where the depletion width equals the half width between the pwells, the vto parameter is as follows

$$vto = \phi - \left(\frac{d_{pw}}{2 \cdot \alpha}\right)^2 \qquad \text{(eq. 2)}$$

where d_{pw} is the distance between the pwells, otherwise know as the JFET region. The built–in potential ϕ between the pwell and JFET with associated dopings P_{pw} and N_{jfet} is given by

$$\phi = \phi_t \cdot \log\left(\frac{N_{jfet} \cdot P_{pw}}{n_i^2}\right) \qquad \text{(eq. 3)}$$

where n_i is the intrinsic carrier concentration and ϕ_t is the thermal voltage. The depletion factor α is given by

$$\alpha = \frac{\sqrt{2 \cdot \varepsilon_{SiC} \cdot P_{pw}}}{q \cdot N_{jfet} \cdot (N_{jfet} + P_{pw})} \qquad \text{(eq. 4)}$$

where q is the Coulomb charge and ε_{SiC} is the SiC permittivity.

Further derivation of the beta parameter is given by

$$\beta = \frac{2 \cdot H_{bayeff}}{X_{jpw} \cdot \rho \cdot (-\,vto)} \cdot \left(\frac{d_{pw}}{2} - \alpha \cdot \sqrt{\phi}\right) \qquad \text{(eq. 5)}$$

where X_{jpw} is the junction depth of the pwell. The resistivity ρ as a function of mobility μ is given by

$$\rho = \frac{1}{q \cdot N_{jfet} \cdot \mu} \qquad \text{(eq. 6)}$$

H_{bayeff} is the effective distance between gate runners which will be derived in the scaling section that follows.

The extended drift region beyond the JFET is modeled with R_{drift} which is parameterized according to the epi and N^+ doping and cross sectional area dependent on cell pitch CP.

Body Diode

SiC MOSFETs, like other power MOSFETs, conveniently contain a built in junction diode between the P_{pw} and N_{epi} layers for reverse conduction. It is well known that the simple SPICE diode model does not capture reverse recovery effects. A physical diode model with reverse recovery was proposed in [13]. In this work, this model has been extended to include specific layout scaling for the SiC MOSFET. This diode model presented in [14] is the basis for all **onsemi** fast recovery diode models.

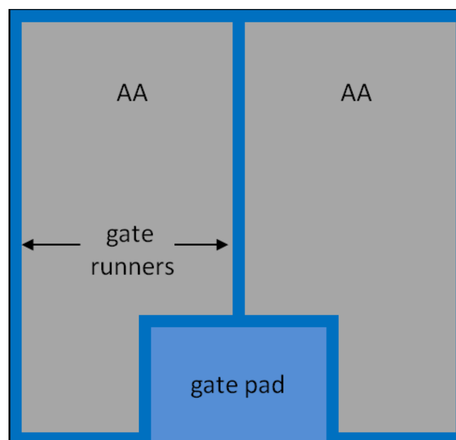

Figure 3. SiC MOSFET Typical Layouts

Capacitances

The C_{GD} capacitance in SiC MOSFET devices is captured by a behavioral MOS−capacitor which depends on process and layout parameters such as gate oxide thickness t_{ox}, d_{pw} and N_{jfet}. As the doping in the JFET region is often engineered to balance capacitance and current nonlinear effects, the measured capacitance exhibits multiple transition regions which are doping and geometry dependent. A base equation for the C_{GD} MOS capacitor is given by

$$C_{GD} = \frac{C_{ox} \cdot C_{dep}}{C_{ox} + C_{dep}} \quad \text{(eq. 7)}$$

where C_{ox} is the oxide capacitance directly determined by the oxide thickness t_{ox}. Further, C_{dep} is given by

$$C_{dep} = \frac{\varepsilon_{SiC}}{W_{dep}} \quad \text{(eq. 8)}$$

where the depletion width W_{dep} becomes a function of doping and JFET pinch−off conditions. The depletion region is obtained through the summation of multiple components. The first two components occur pre−JFET pinch−off and vary due to the changing doping profile from the surface into the JFET region. The first portion is given by

$$W_{dep1} = \left(\frac{2 \cdot \varepsilon_{SiC}}{q \cdot N_{surf}} \cdot \min((V_{DG} - V_{FB}),\ V_{surf})\right)^{mjsurf} \quad \text{(eq. 9)}$$

where V_{FB} is the flatband voltage, N_{surf} is the doping just below the oxide, mjsurf and mj in (10) are grading parameters close to 0.5, and V_{surf} is the effective voltage when the transition occurs in the doping profile to N_{jfet}. The second component is given by

$$W_{dep2} = \left(\frac{2 \cdot \varepsilon_{SiC}}{q \cdot N_{surf}} \cdot \min((V_{DG} - V_{FB} - V_{surf}),\ -vto)\right)^{mj} \quad \text{(eq. 10)}$$

All min and max functions are implemented through square root limiting equations that provide smooth transitions, necessary for data fitting and good convergence. The 3rd depletion represents the drop of the bottom plate of the depletion region once the JFET region pinches off. A smooth step function is implemented that introduces W_{dep3} which is directly related to X_{jpw} at V_{DS} = vto. The additional W_{dep} post pinch−off is then controlled by the N_{epi} and limited by the thickness of the epi region.

The C_{GS} is mostly determined from the bsim3v3 channel model. In addition, a fixed capacitor for the gate poly overlap of N^+ and source metal overlap of gate poly is included in the model.

The C_{DS} capacitance comes through the body diode junction capacitance as previously described.

Scaling

As the model uses lumped components, one needs to derive the effective width and multiplicity factors from the layout parameters for the device components such as the bsim3v3, JFET, diode, and capacitances. First the active area is calculated based on the input layout parameters as follows

$$AA = (W_{chip} - 2 \cdot X_{edge}) \cdot (H_{chip} - 2 \cdot Y_{edge}) - GP_{loss} - GR_{loss} - CNR_{loss} \quad \text{(eq. 11)}$$

where W_{chip} is the chip width, H_{chip} is the chip height, X_{edge} and Y_{edge} are the dimensions from the chip edges to the active area. Equations for GP_{loss} (gate pad area), GR_{loss} (gate runner area), and CNR_{loss} (corner area) are not listed here but are obvious to derive. As not all gate fingers have the same height due to the gate pad, an effective height is derived as

$$H_{bayeff} = \frac{AA}{[(W_{chip} - 2 \cdot X_{edge}) \cdot 2 \cdot (1 + N_{grunner})]} \quad \text{(eq. 12)}$$

where $N_{grunner}$ is the number of internal gate runners, not counting the side runners. The multiplicity factor is given by

$$mult = \frac{2 \cdot (W_{chip} - 2 \cdot X_{edge}) \cdot 2 \cdot (1 + N_{grunner})}{CP} \quad \text{(eq. 13)}$$

where the first 2 factor accounts for the cell symmetry.

Figure 3 displays a typical layout where the non−active regions in the die edges, runners, and gate pad contain distinct parasitic capacitances and resistances. Varying degrees of the proportionality of parasitics to the active device are clear. The model includes physical, scalable components for every parasitic element.

Miscellaneous

The gate poly and metal runner resistances are scalable with device process and layout parameters. The gate poly resistance is given by

$$R_{poly} = \rho_{shpoly} \cdot \frac{H_{bayeff}}{L_{poly} \cdot \frac{mult}{2} \cdot rdist} \quad \text{(eq. 14)}$$

where ρ_{shpoly} is the gate poly sheet resistance and rdist is a distributed fitting parameter typically in the range of 3. Simple SPICE tc1 and tc2 temperature parameters are supported for the gate resistance.

The model is fully electro−thermal, including ambient and self−heating for the channel and JFET regions following [1, 12]. In addition, the diode model has been extended to include self−heating. The device power drives into a thermal impedance network to solve for the junction temperature T_j implicitly in SPICE. Cauer networks are implemented in order to provide physical cascading of the system Z_{TH} networks.

Parasitic inductances are included in the model for discrete packaged components.

SIC MOSFET MODEL VERIFICATION

Benchmark results are presented for **onsemi**'s 1200 V SiC MOSFET Technology.

Current−Voltage (IV)

Multiple facets of the current−voltage relationship are investigated. All IV tests are performed under pulsed conditions with a pulse width of 250 μs. Pulsed transient simulations are run to mimic the test conditions. The currents are sampled at the end of the pulses analogous to the measurements. This ensures consistency between simulated and measured T_j, critical for power semiconductor model extraction. Figure 4 shows the T = 25°C output characteristics. Very accurate modeling of the output conductance is achievable. One can clearly see the effects of the JFET region at high gate and drain biases where the current begins to compress. Figure 5 shows the T = 25°C transfer characteristics at V_{DS} = 0.1 V. A very good match to the current and transconductance through the entire V_{GS} range is realized, including accurate modeling of the subthreshold region previously unreported.

As the robust temperature behavior of SiC MOSFET devices is a key feature to technology adopters, accurate modeling of the device performance over temperature is critical for circuit design. Figure 6 displays the output characteristics for V_{GS} = 20 V over varying temperature. Figure 7 displays the transfer characteristics at V_{DS} = 0.1 V over varying temperature. The threshold voltage at I_D = 10 mA is plotted in Figure 8 over temperature. The R_{DSon} over temperature is plotted in Fig. 9. The temperature parameters associated with the bsim3v3 and JFET models such as KT1, UTE, UA1, AT, BTEE, and VTTC are deployed. Lastly, the body diode current−voltage characteristics over temperature are plotted in Figures 10, 11. The overall temperature results are a clear indication of the model's ability to accurately capture the SiC MOSFET temperature behavior.

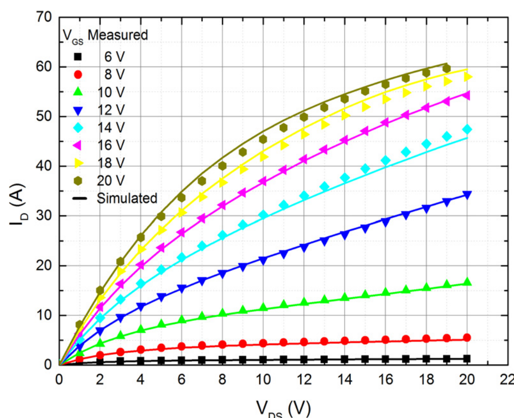

Figure 4. SiC MOSFET Output Current at T = 25°C

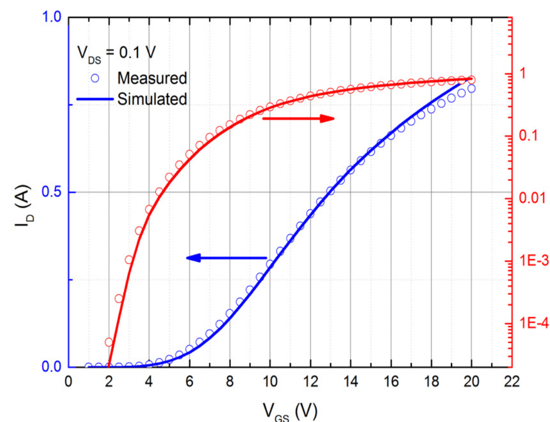

Figure 5. SiC MOSFET Transfer Current at VDS = 0.1 V, T = 25°C

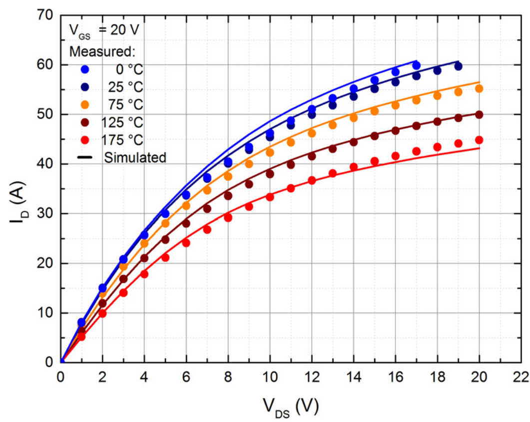

Figure 6. SiC MOSFET Output Current over Temperature

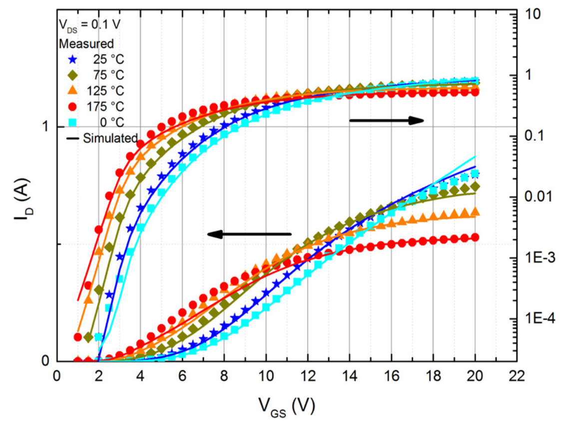

Figure 7. SiC MOSFET Transfer Current over Temperature

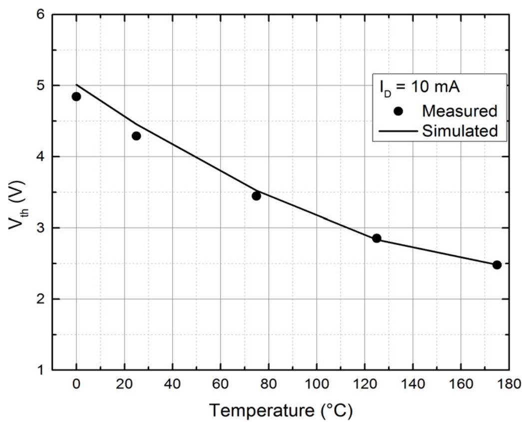

Figure 8. SiC MOSFET Threshold Voltage over Temperature

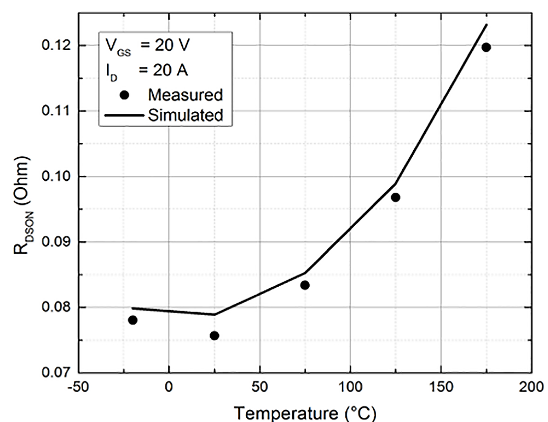

Figure 9. SiC MOSFET RDSon over Temperature

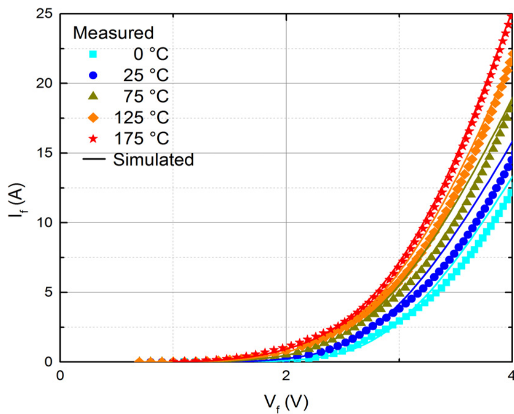

Figure 10. SiC MOSFET Body Diode Current−voltage on Linear Scale

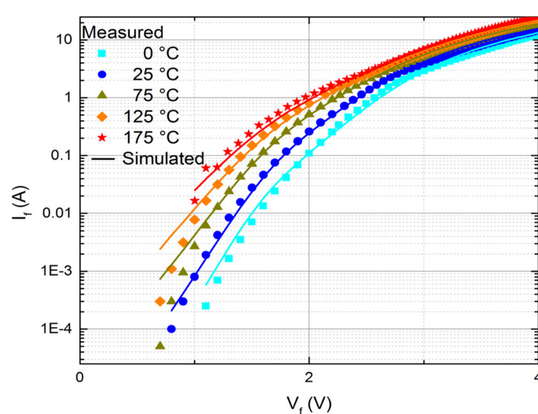

Figure 11. SiC MOSFET Body Diode Current−voltage on Log Scale

Capacitance−Voltage (CV) and Gate Charge

Figure 12 demonstrates the model accuracy for conventional capacitances C_{ISS}, C_{RSS}, and C_{OSS}. The accurate match of the multiple transitioning regions in the C_{RSS} validates the proposed C_{GD} model. The characteristics are shown on log−log scales in order to highlight the highly nonlinear behaviors over multiple orders of magnitude. As a direct consequence of the accurate capacitance simulation, reasonable gate charge results are expected as shown in Figure 13.

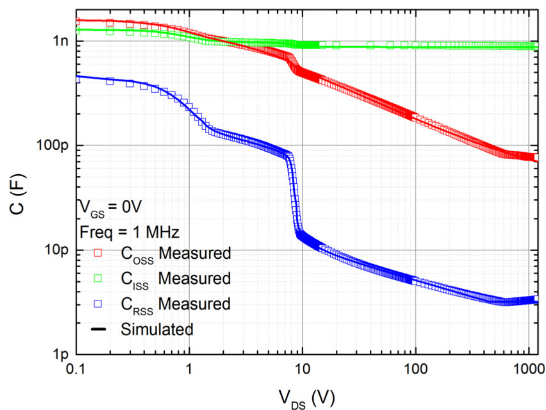

Figure 12. SiC MOSFET Standard Capacitances

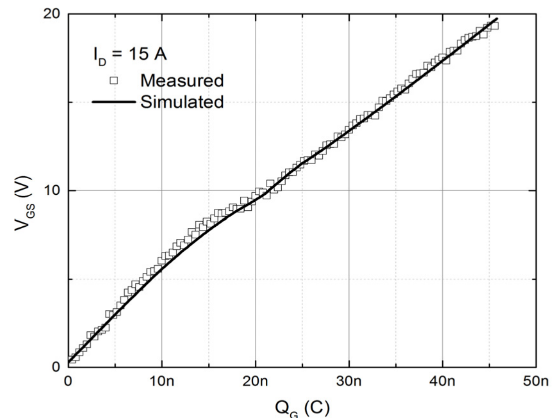

Figure 13. SiC MOSFET Gate Charge, Note the Presence of a Parasitic C_{GS} = 1 nF in Test Setup

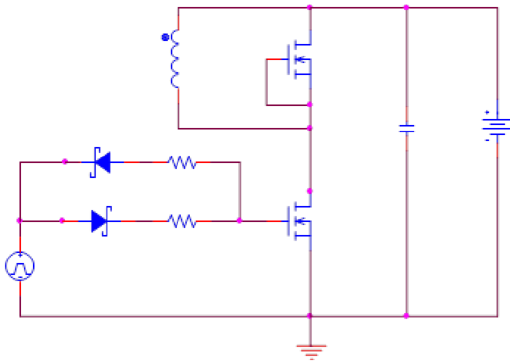

Figure 14. Double Pulse Switching Circuit

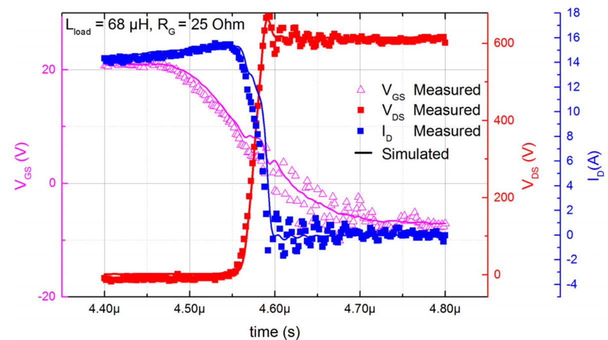

Figure 15. SiC MOSFET Double Pulse Switching OFF at I_D = 15 A

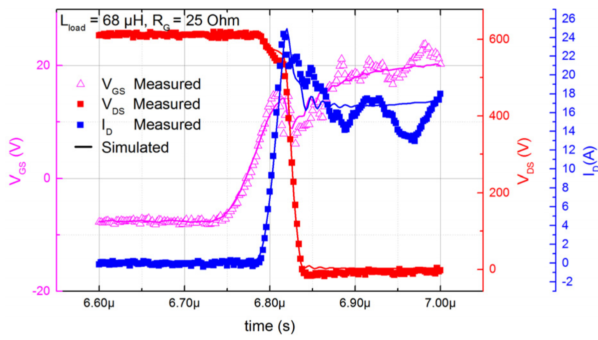

Figure 16. SiC MOSFET Double Pulse switching ON at I_D = 15 A

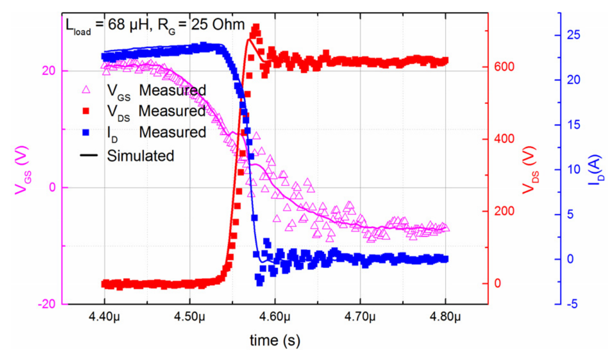

Figure 17. SiC MOSFET Double Pulse switching OFF at I_D = 24 A

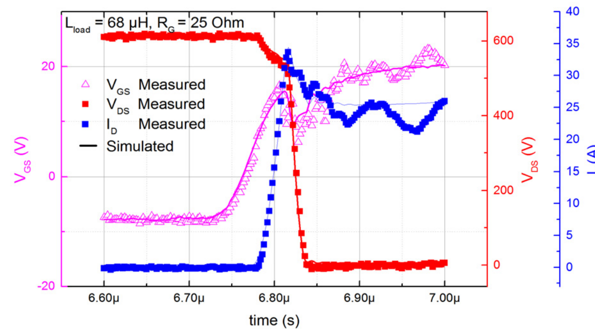

Figure 18. SiC MOSFET Double Pulse switching ON at I_D = 24 A

Double Pulse Switching and Reverse Recovery

The double pulse circuit is widely used to evaluate switching characteristics for power semiconductors. The basic switching circuit is shown in Figure 14 where many of the parasitic elements associated with the passives and the boards are left out for simplicity. The previously characterized SiC MOSFET is incorporated for the high side and low side devices. Figures 15−18 demonstrate the model's ability to accurately capture turn−on and turn−off transient waveforms at two different current levels. The near precise prediction of the highly nonlinear capacitances and miller effects in Q_G leads to reasonable prediction of the switching results with no further tuning required. SiC MOSFETs have fast switching characteristics and low switching losses. Mismatching in oscillations is due to inaccuracies in modeling the test circuit components and their parasitics such as the load inductor, electrolytic capacitors and circuit board routing.

Scaling

A second device is characterized with the same chip dimensions, but with a 42% increase in cellpitch and 12% increase in L_{poly}. The base model is directly simulated with the new layout parameters with no further tuning. Figure 19 shows the capacitance which is a key indicator of correct scaling. Highly accurate results are obtained validating the scalability of the model.

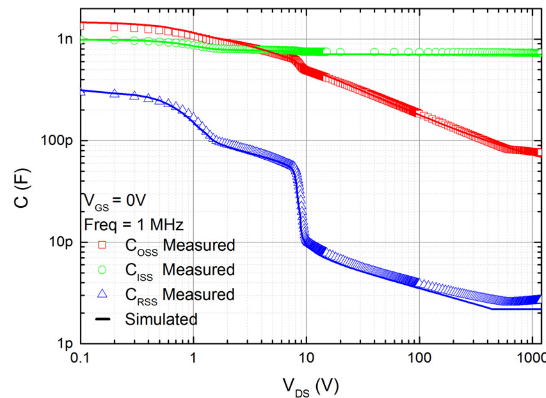

Figure 19. Standard Capacitances for Device with a 42% Increase in CP and 12% Increase in L_{poly}

TRENCH IGBT MODEL DESCRIPTION

Figure 20 illustrates a trench IGBT cross section and Figure 21 displays the corresponding SPICE subcircuit rendition. The starting point for the physical model was the work by Lauritzen in [15] for planar IGBTs. The model contains a solid foundation for the IGBT carrier transport physics. However, it does not contain physical equations for the trench device behavior with varying layout and process parameters. This model was extended in this work with the following attributes:

- Development of physical/scaling equations for trench IGBT process
- Replaced empirical intrinsic MOSFET model with bsim3v3 model similar to SiC MOSFET model
- Added physical/nonlinear dynamic capacitor models for trench technology including pinching effects between the trenches
- Added emitter cell and source blocking modeling for short circuit robust technologies
- Added full electro−thermal effects
- Implementation in SPICE through arbitrary sources
- Numerically robust, good convergence/speed performance

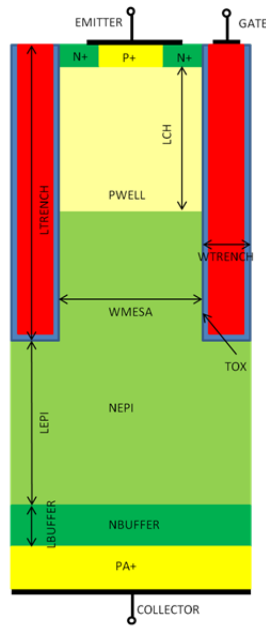

Figure 20. Trench IGBT Cross Section

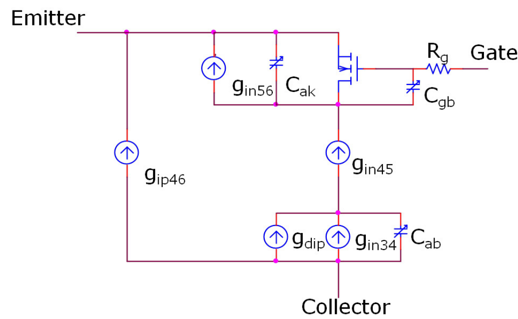

Figure 21. Trench IGBT Subcircuit Model

Details of the subcircuit C_{gb} capacitor associated with the conventional C_{RES} are covered here. The model uses a MOS depletion formulation similar to the SiC MOSFET, however the pinch−off voltage between the trenches follows different physics. The pinch−off voltage equation is given by

$$V_p = \frac{q \cdot N_{jfet} \cdot W_{mesa}}{2} \cdot \left(\frac{1}{C_{ox}} + \frac{W_{mesa}}{4 \cdot \varepsilon_{Si}} \right) + V_j \qquad \text{(eq. 15)}$$

where N_{jfet} is the doping between the trenches underneath the P_{well} and V_j is the junction potential of the anode to buffer layer determined by the layer doping concentrations.

The trench IGBT follows similar layout and gate resistance scaling as previously described for the SiC MOSFET.

TRENCH IGBT MODEL VERIFICATION

Benchmark results are presented for multiple generations of **onsemi**'s 650 V Field Stop Trench IGBT Technology.

Current−Voltage (IV)

Multiple facets of the current−voltage relationship are investigated under pulsed transient conditions as previously described. Figure 22 displays typical output characteristics up to high power levels to show the effects of self−heating at T = 25°C. Figure 23 shows the output current zoomed into the V_{CEsat} region at T = 25°C and T = 175°C. Figure 24 shows the transfer characteristics at T = 25°C and T = 175°C. Both temperature dependent plots show the model's accurate prediction of thermal behavior.

Capacitance−Voltage (CV) and Gate Charge

Figure 25 demonstrates the model accuracy for conventional capacitances C_{IES}, C_{RES}, and C_{OES}. The accurate match of the C_{RES} drop voltage validates the physical model for the pinch off voltage. Accurate gate charge simulation is expected as shown in Figure 26.

Double Pulse Switching

The same switching circuit as shown in Figure 14 is used with the MOSFETs exchanged for co−packed Trench IGBTs. Figures 27 and 28 demonstrate the model's ability to accurately capture turn−on and turn−off transient waveforms. The accurate simulation of the gradual rise in V_{CE} during the off transition is attributed to the dynamic capacitance C_{gb}. The accurate modeling of the collector current I_C throughout the on transition validate the accurate modeling of the reverse recovery of the co−packed diode.

Layout Scaling

In **onsemi**'s most recent Trench IGBT Technology FS4, a 75 A device is used to characterize the base scalable model. The base model is directly simulated with the new layout parameters for a 50 A device with no further tuning. Figures 29 and 30 show the current−voltage and C_{RES} respectively. Highly accurate results are obtained validating the scalability of the model.

Process Scaling

Due to the inherent model physics and process parameterization, key device trade−offs can be evaluated such as the well known trade−off curve in IGBTs (E_{OFF} vs. V_{CEsat}). Typically power semiconductor manufacturers provide products from multiple derivatives of one technology generation. Often, the only difference between an IGBT derivative is the anode doping to control the trade−off curve. The model presented here is able to accurately predict trade−off curve performance through direct adjustment of the anode doping as shown in Figure 31. The scalable process parameters are presented to the designer at the symbol level as shown in Figure 32 where *ncolln* stands for the normalized collector (or anode) doping.

In this mode, designers can run parametric sweeps of the anode doping to understand the design and application sensitivities to key process parameters.

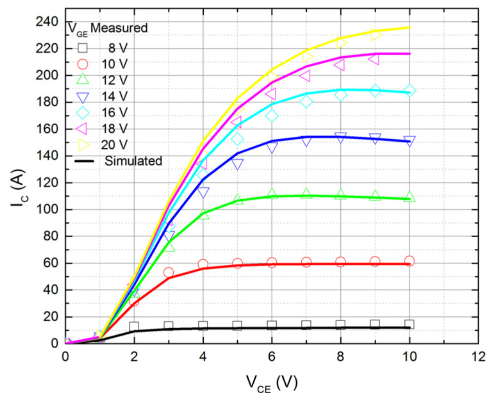

Figure 22. Trench IGBT I_C vs. V_C at T = 25°C

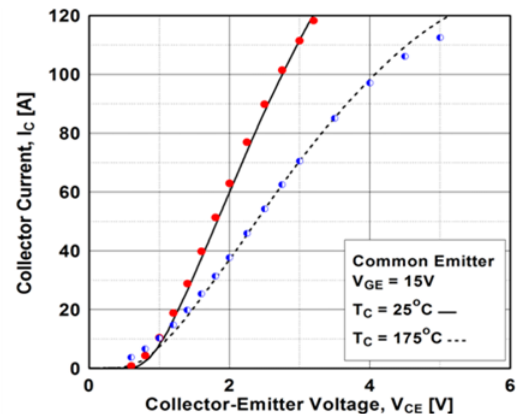

Figure 23. Trench IGBT I_C vs. V_C at T= 25°C and 175°C

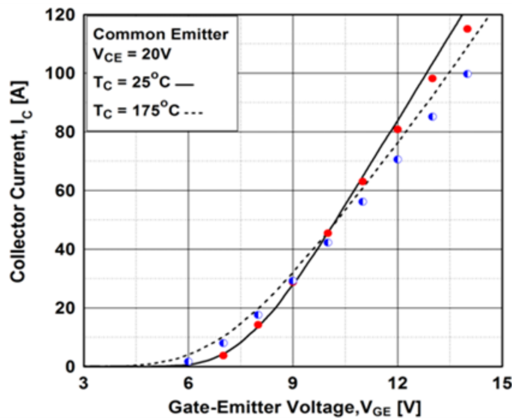

Figure 24. Trench IGBT I_C vs. V_G at T=25°C and 175°C

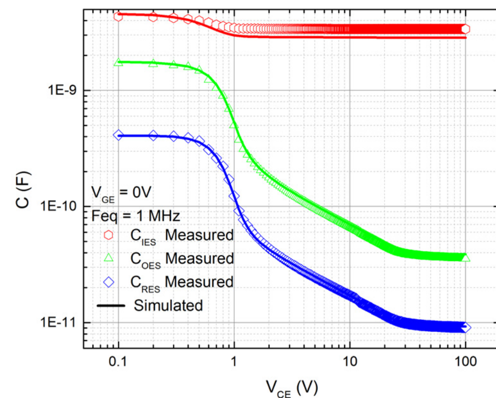

Figure 25. Trench IGBT Standard Capacitances

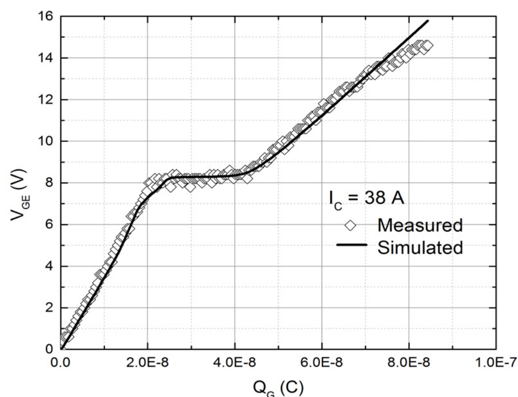

Figure 26. Trench IGBT Gate Charge

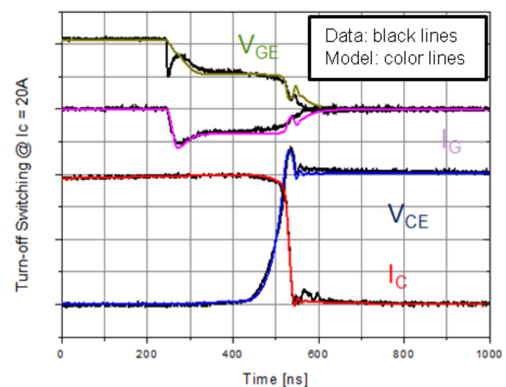

Figure 27. Trench IGBT Double Pulse Switching OFF at I_C = 20 A

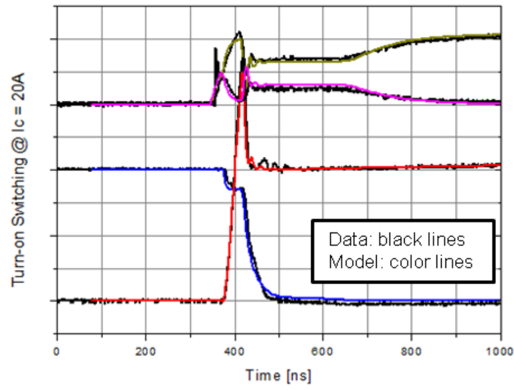

Figure 28. Trench IGBT Double Pulse Switching ON at I_C = 20 A

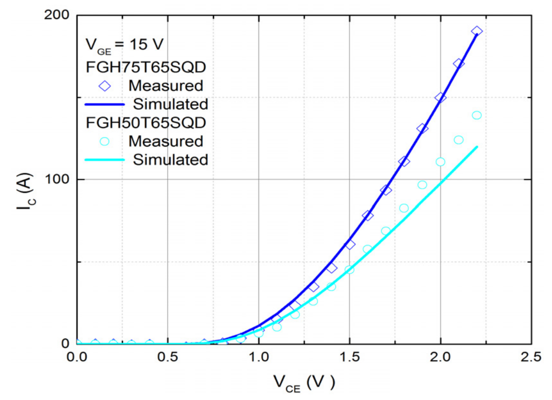

Figure 29. Trench IGBT I_C vs. V_C Scaling

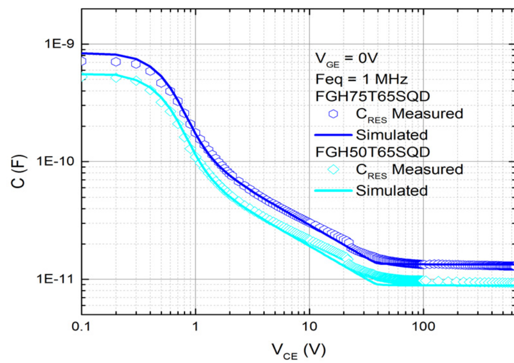

Figure 30. Trench IGBT C_{RES} Scaling

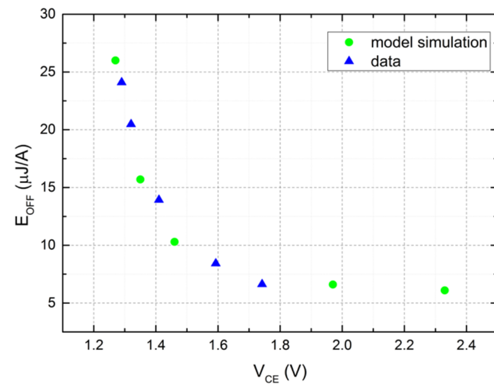

Figure 31. E_{OFF} vs. V_{CE} Trade

ROBUST SPICE AGNOSTIC MODELING

onsemi's models are built as physically based subcircuits. SPICE primitives are used whenever possible for best speed and convergence. However due to the complex physics associated with modern power semiconductor devices, accurate and physical SPICE primitives are largely unavailable. Once the device physics for a particular device is derived, one can use controlled sources (typically G and E) to implement physical temperature dependent equations for currents, charges, and capacitances.

The power semiconductor design community uses a wide range of SPICE like simulators. Thus to minimize multiple simulator specific model support and provide consistent results across simulators, a SPICE agnostic approach is taken. A key component is to use least common denominator SPICE elements and syntax which is generally found in PSPICE. Behavioral languages like Verilog−A and MAST, though very attractive for model implementations, are avoided as they are not supported by all the common simulators.

CONCLUSION

This paper presents a novel approach to SPICE level modeling of power semiconductor devices. Highly accurate results are achievable for current nonlinearity and temperature effects through the subthreshold, linear and saturation regions. In addition, the all critical transfer capacitances associated with MOSFET C_{RSS} and IGBT C_{RES} are captured accurately across the full bias range, enabling precise simulation of typical application circuits. The introduction of scalable modeling of the device layout and process variation enables designers to unlock previously recognized but inaccessible device optimization points. The robust models are valid across multiple SPICE platforms such as PSpice, LTspice, Simetrix, Spectre, ADS, SABER, and Simplorer.

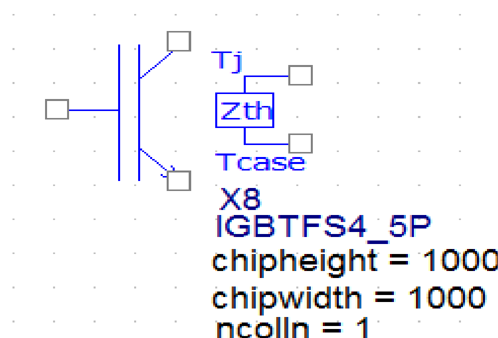

Figure 32. Trench IGBT PSPICE Symbol

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