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AND90006/D

Recommendations for Reliable Switching Performance using ON Semiconductor 40 V and 80 V Automotive Power Modules Using Shielded-Gate MOSFETs

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APPLICATION NOTE

Summary

The ON Semiconductor automotive qualified power module family (AutoSPM) was introduced in 2008 and since then has experienced steady improvements, including most recently shielded–gate MOSFETs in the 40 V and 80 V nodes. These MOSFETs further optimize the figure of merit between on resistance $R_{DS(on)}$ and gate charge Q_g, and thus extends the modules' capability for high frequency and high current switching. This application note provides recommendations on the selection of gate resistors and limits to the dc link bus inductance necessary to obtain the full benefit of this new MOSFET technology while maintaining safe operation in hard–switched inverter system designs.

Safe switching of the very fast shielded–gate MOSFETs requires a good balance of speed and external stray inductance to ensure safe operation, especially as inverter output current levels are pushed to the full capability of the modules. To explore the most effective use of these modules for high current and high speed switching applications, ON Semiconductor has utilized extensive bench testing to provide guidance to our customers. This application note describes the process used to arrive at our guidance, including:

- Running an experimental benchtop inverter system to explore operating limits and create failures to define the critical parameters that lead to the failures
- Identify the root cause of the failures
- Provide guidance on selection of gate resistors for (especially) turn–off and the impact of dc capacitor and bus bar parasitic inductance in order to ensure safe operation at the limits of the data sheet performance

Careful adherence to the guidance provided herein will ensure reliable operation of inverters employing the AutoSPM line of shielded–gate MOSFET power modules.

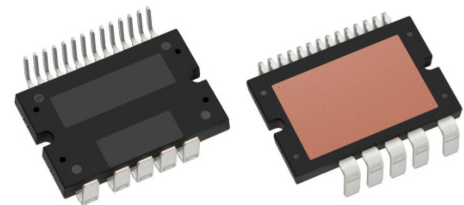


Figure 1. AutoSPM Module Photo

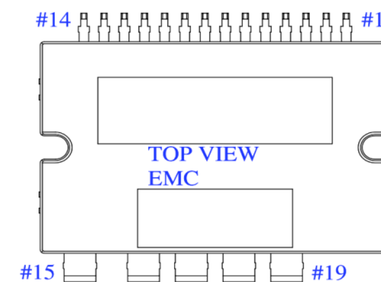


Figure 2. Pin Configuration

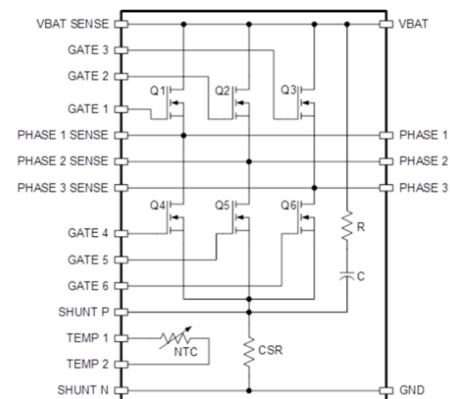


Figure 3. Internal Equivalent Circuit

1. What Can Possibly Go Wrong?

Improper integration of the AutoSPM power modules into an automotive accessory inverter drive can result in exceeding the safe operating limits of the power MOSFETs. Without attention to system level considerations, a user may experience failures during development, with distinctive characteristics, such as:

- The module may operate normally for some time (from minutes to days) until unexpectedly it fails on startup, at relatively low current
- A failure determined to be "EOS" may occur on any one of the six MOSFETs inside the 3−phase module. Through X−Ray scan and microscopy upon decapsulation of the module, the burn mark on the MOSFET may show up at various locations without a regular pattern (Figure 4).

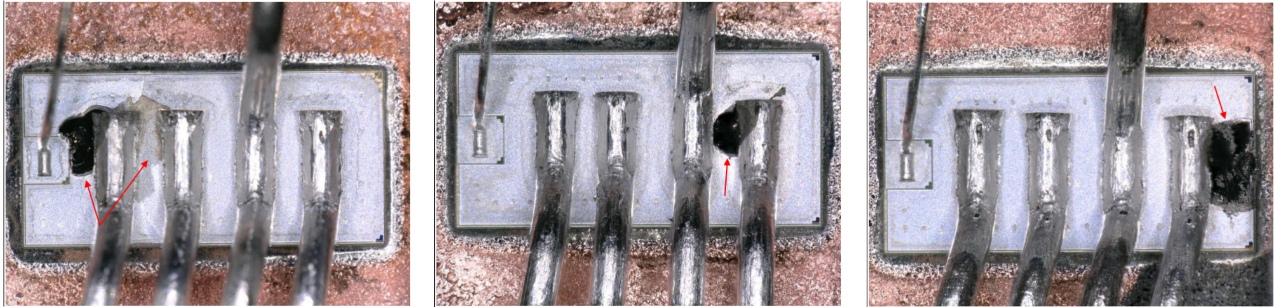


Figure 4. Microscopy Photo of Damaged MOSFET Die

The root cause of such failures can be difficult to determine. When otherwise operating within the data sheet limits, the root cause is likely repetitive avalanche. This can occur under conditions of phase current and junction temperature that are thought to be within the safe operating area of the MOSFET, but actually exceed the avalanche rating of the part. Some comments on this situation are given below:

- Because the failures occur after only a few minutes or days of operation, it is not a normal lifetime reliability issue. These failures typically occur during startup of the inverter, when the electrical stress is not very high.
- Because the damaged MOSFET can be in any location within the module, it does not look like package fabrication (such as bonding wire, die soldering, etc.).
- It does not appear like a failure due to package parasitics or package thermal performance, since these characteristics remain unchanged from part to part and over time.
- For these shielded−gate power trench MOSFETs, the major improvement is reduction in $R_{DS(on)}$ and Q_g, making the module capable of conducting higher current and switching faster. Both of these traits will lead to higher di/dt during the switching event. Meanwhile, it is known that damage related to avalanche occurs due to excessive di/dt interacting with the power loop inductance.

The simplified schematic of one phase of the module shown in Figure 5 illustrates the key parasitic elements, both internal and external to the module. As indicated, the voltage across these parasitic inductances add to the DC bus voltage, and can be expressed as in Equation [1]. Together, they may elevate the voltage across the device (V_{DS}) up to the avalanche break down voltage, which is ~1.3 times the breakdown voltage from device's data sheet (for safety margin). Table 1 lists parameters that have been extracted from an benchtop inverter design. The calculation of V_{DS} during turn off, shown in Equations [2] and [3], demonstrates the danger that the device can be operated very close to the avalanche voltage.

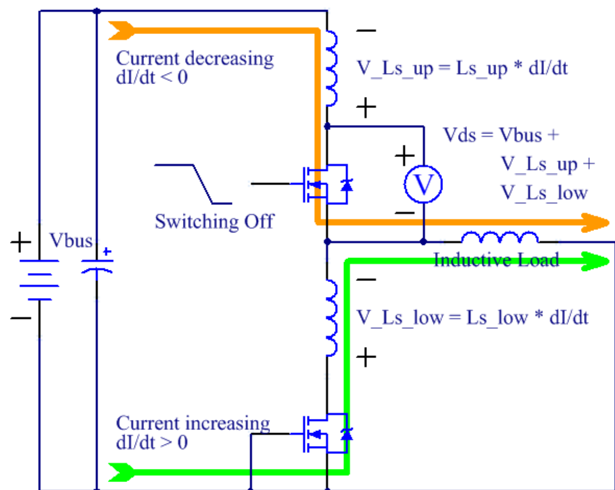


Figure 5. Voltage Polarity of Stray Inductance (same as the polarity of di/dt) during Upper FET Switching Off

$$V_{ds} = V_{bus} + L_s \frac{dI}{dt} \qquad \text{(eq. 1)}$$

$$V_{ds} = 12 + (10 + 15) \times 1.5 = 49.5 \quad \text{(eq. 2)}$$

$$V_{avalanche} = 40 \times 1..3 = 52 \quad \text{(eq. 3)}$$

Table 1. PARAMETERS FROM AN EXISTING INVERTER DESIGN

DC bus voltage [V]	12
MOSFET breakdown voltage [V]	40
Module inductance [nH]	~10
Power loop inductance [nH]	~15
Turn off di/dt [A/ns]	~1.5

In the following sections, to reveal the relationship between excessive repetitive avalanche and module failure, an experimental test setup with fixed loop inductance with controllable di/dt is shown. The di/dt directly determines the amplitude of overshoot voltage during device switching off and the associated avalanche energy. Thus, the setup will allow investigation of the limits of safe operation during switching off, as controlled by the gate resistors, the amplitude of the phase current, and the value of stray bus inductance.

2. Reproduction of Failure Mode and Suggestion of Minimum Gate Resistance

Calculations from the previous section confirm that under worst case operating conditions the device may enter the avalanche region during turn off if stray inductance is high enough. It should be mentioned that most modern power trench MOSFETs are designed to repetitively avalanche without failing, as long as the avalanche energy remains sufficiently low to avoid excessive junction temperature. Many combinations of inductance, phase current amplitude, and di/dt may be encountered in module applications that are in the control of the end user. To illustrate a process by which a user can ensure safe operation of the module, an experimental inverter system has been implemented to represent typical automotive accessory inverters to find the safe limits via long−term tests. This is shown in Figure 6.

An open loop space vector PWM (SVPWM) algorithm was implemented which is sufficient to generate sinusoidal currents through the manipulation of modulation index with an inductive load.

A wye−connected 3−phase line filter was used to represent a set of balanced motor windings, without the complexity of a fully functional motor dyno. The key requirement is for the power module carry reactive and active power. The only difference is that a rotating motor will also generate back EMF which will result in a higher modulation index during motor operation. Such behavior is not accounted here, and is not pertinent to the failure mechanism, so long as the phase current amplitude is representative of a realistic automotive auxiliary motor.

The complete test system is shown in Figure 6. Three inverter systems run concurrently, sharing the same DC power supply while having their own dedicated DC link capacitor bank and busbar structure. This is to increase the number of AutoSPM samples that can be tested at one time.

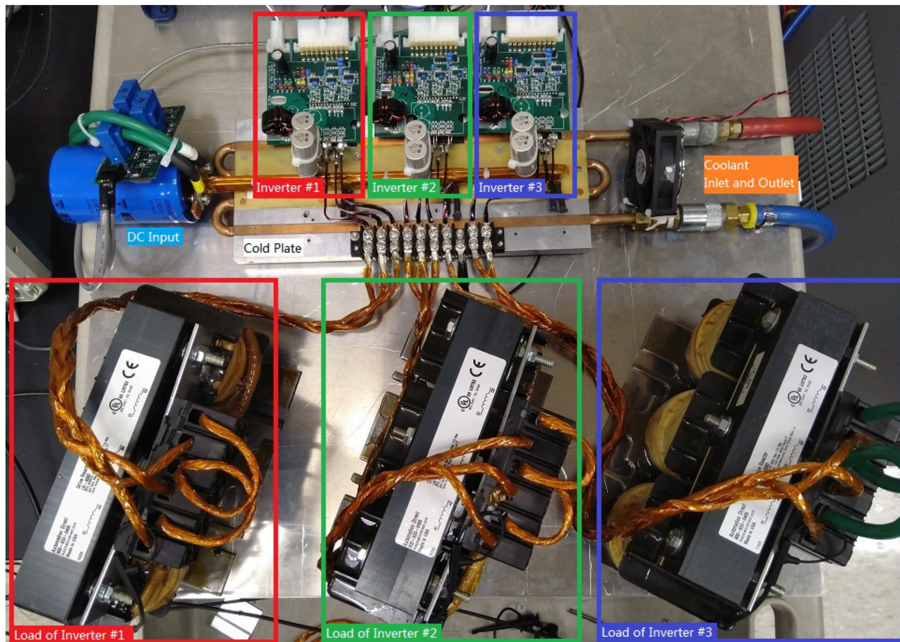


Figure 6. Benchtop Test Setup

Description of the Inverter System & Test Procedure

In a SVPWM inverter, assuming constant torque and constant speed, the phase current is sinusoidal, so the MOSFET instantaneous switching current is varying at the sinusoidal frequency (motor fundamental). Given that switching time of the device is relatively constant, the

resulting di/dt varies across each switching event according to a rectified sinewave. In this test, the V_{DS} waveform has been continuously captured since the purpose of the test is to answer two questions: (1) do the MOSFETs enter avalanche during turn off, and (2) how often do the MOSFETs enter avalanche?

In order to increase progressively the stress on the MOSFETs until failures were observed, our test procedure followed these steps:

1. Choose $R_{g(on)}$ and $R_{g(off)}$ of the gate driver, starting from conservative 50 Ω for low di/dt.
2. Raise the coolant temperature to 80°C (representing automotive cooling conditions) and confirm that the module case temperature reaches 80°C by reading the module's NTC thermistor.
3. Start the inverter, gradually increase modulation index until target load current been reached. Run continuously for 4 hours.
4. Stop the system, set coolant temperature as 20°C, and monitor T_{case} until it cools to 20°C.
5. Re−start the inverter as shown in step (3), and if everything functions correctly, increase coolant temperature up to 80°C again, and continue run the inverter.
6. Repeat (4) and (5). If all 3 modules still function correctly after the total running time reaches 24 hours, then this round of the test will be recognized as a "pass".
7. For the next round, if no failure occurred, reduce $R_{g(on)}$ and $R_{g(off)}$. If current $R_{g(on)}$ and $R_{g(off)}$ value is larger than 10 Ω, then reduce by 10 Ω each time; if current $R_{g(on)}$ and $R_{g(off)}$ value is smaller than 10 Ω, then reduce by half each time. If the module failed during this round, then the gate resistors are increased according to the same logic.
8. Replace with 3 new modules and then start all over from step (1).

Sample Test Results

Two typical turn off events are shown in Figures 7 and 8. The flat top V_{DS} waveform from Figure 7 is a clear sign of the MOSFET entering avalanche, due to the voltage clamping effect of avalanche breakdown. But in Figure 8, we see the peak V_{DS} voltage does not reach avalanche voltage, hence V_{DS} is not clamped. For longer time scales, as show in Figure 9, we see the amplitude of turn off overshoot varies during different switching events, according the sinusoidal phase current. In addition, one interesting finding here is when the sinusoidal phase current reaches its peak value the switching off overshoot is not necessary to reach its peak as well, in other words, the di/dt it not high despite the current is at its peak value. One reasonable explanation here it, since the load is inductive, freewheeling current can leads to soft switching on or off with help of device's body diode.

During the sequence of tests, $R_{g(on)}$ and $R_{g(off)}$ values were reduced round after round until some modules failed to complete the whole 24 hours duration. With this failure information, the last known R_g value for all modules to pass the test should be its minimum allowed value. After adding necessary margin, the recommended minimum R_g values for several AutoSPM part numbers are shown in Table 2.

One thing to be mentioned here is, based on the customer's design, they may reduce $R_{g(on)}$ for higher turn on di/dt and reduced loss, but for the value of stray bus bar inductance tested, it is required not to reduce $R_{g(off)}$ below the stated value. To do so will lead to MOSFET failure due to high turn off di/dt and associated repetitive avalanche. If higher di/dt is required then efforts must be made to reduce stray inductance. This is a system constraint, not a weakness of the MOSFET.

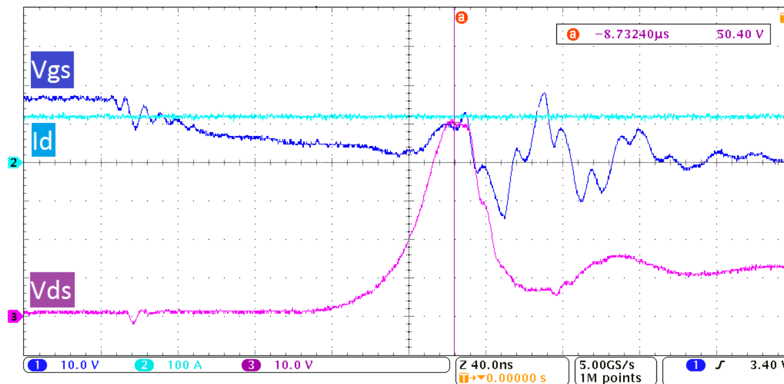


Figure 7. Flat Top Vds Waveform, due to Clamping Effect of Avalanche Breakdown

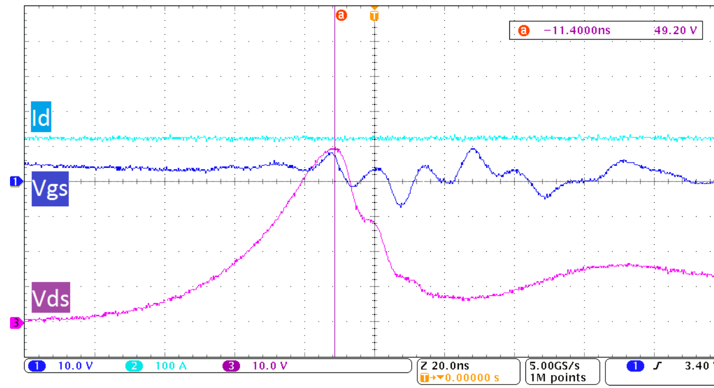


Figure 8. Device does not Enter Avalanche Region

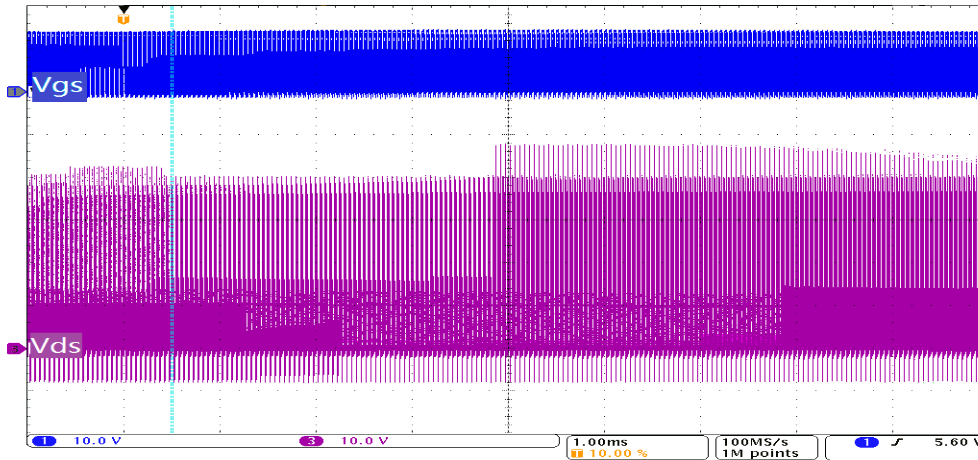


Figure 9. V_{DS} Variation Over Multiple (~200) Switching Periods

Table 2. MINIMUM REQUIRED $R_{g(off)}$ VALUES FOR AutoSPM SHIELDED–GATE TRENCH MOSFET MODULE FAMILY

Module	Breakdown Voltage [V]	Peak Current Rating [A]	Minimum $R_{g(off)}$ [Ω]
NXV04V120DB1	40	160	7.5
NXV08V080DB1	80	130	2.5
NXV08V110DB1	80	190	2.5

3. Recommendations for Bus Structure Improvement

In this application note, by means of a specific bench test setup, we are able to provide guidance and emphasis on some critical aspects that should always be considered during an inverter system design, particularly the selection of suitable turn off gate resistors and dc link filter capacitors and bus bar. But, in realistic automotive applications, some suggestions here may not be feasible due to space and cost limitations, thus system designers will have to rely on their own judgement and detailed analysis of their bus structure. As a general and theoretical instruction, which is based on well known design rules, the following aspects should always be considered first while improving bus structure design.

First, series resistance and inductance are the two major aspects for the bus structure designer to consider, since lowering these values will be beneficial for the whole system's efficiency and reliability. From Equations [4] and [5], it is clear that shorter length and larger cross–sectional area will be preferable.

$$L_{series} = \frac{\mu L}{A} \qquad \text{(eq. 4)}$$

μ: Permeability, L: Length of conductor, A: Cross section area of conductor.

$$R_{series} = \frac{\varrho L}{A} \quad \text{(eq. 5)}$$

ϱ: Resistivity, L: Length of conductor, A: Cross section area of conductor.

Second, in shielded gate MOSFETs, the switching time can be as low as ~50 ns. Combined with their current rating over 100 Amps, a di/dt higher than 2A/ns can be expected in real applications. Referring to Equations [1] to [3], it is clear that by using existing bus structure design and switching off at 2 A/ns, the avalanche voltage will definitely be reached. To avoid this outcome the bus inductance must be reduced, mainly by downsizing it. But, as the most visible component in a bus structure, the electrolytic capacitors dominate the geometry. They are intended to supply lower frequency, higher power (i.e. DC−AC inverter outputs 60 Hz/160 A sinusoidal current) to stabilize DC bus voltage. However, the negative effect is that the bus bar connecting them to the module will add length, which leads to higher series inductance. By comparison, to stabilize the DC voltage during the very short (~50 ns) switching transient when avalanche occurs, small ceramic capacitors with low ESR/ESL are more suitable, and should be placed very close to the module.

Finally, system assembly such as alignment of switching devices is also important. The hardware setup which provided data for this document had to be renovated several times during the failure investigation to achieve minimal stray inductance. Without any surprise, the R_g values provided in Table 2 were based on results from the final version of bus structure design. It achieved the lowest loop inductance (~7.5 nH, measurement shows in Table 3). In comparison, the previous version was much higher (~20 nH), and the V_{DS} waveforms captured on the oscilloscope proved that the MOSFET entered avalanche region during every turn off event. Under such conditions, if we want the module to pass the test, turn off di/dt had to be reduced through increased $R_{g(off)}$ values. However, following this strategy, test results showed the required $R_{g(off)}$ to be at least 50 Ω, which is impractical for real applications, due to unacceptably high switching loss.

In specific, the following steps were taken to improve this test setup, the final version of which is shown in Figure 10. These recommendations are valid for user's inverters as well.

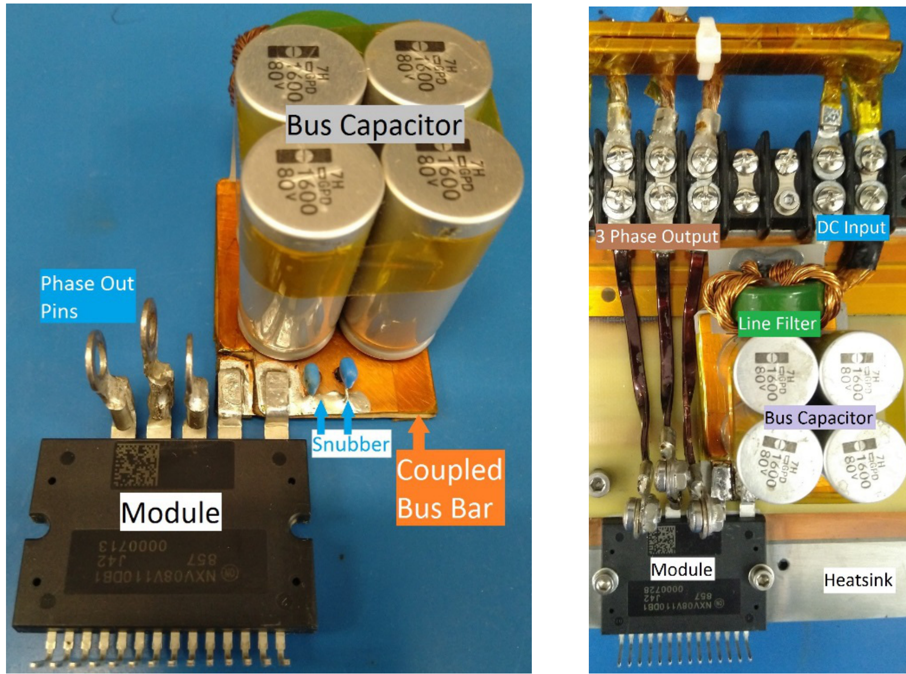
1. Maximize the contacting surface area between the module's power leads and bus bar and keep them near to reduce series inductance. In automotive assembles, the module power leads are usually welded to the busbar. So the suggestion here is to enlarge the surface area of the welding spot, and keep the welding spot as close to the module body as possible.
2. In addition to the bulk storage electrolytic capacitors, add a few smaller ceramic capacitors (~10 uF each) very close to the module, between the longer (hence higher inductive) connection of the electrolytic capacitors to the module. This way is more efficient in keeping the DC voltage stiff during the high frequency switching transient.
3. A common−mode line filter was added to each bus structure when connected to the common DC bus, to avoid noise from each module being coupled into the common DC bus, and causing interference to other systems sharing the same bus.
4. By choosing plate shaped bus bar, the series inductance can be reduced through overlaying the positive plate and the negative plate. The reason is current flow in opposite directions through a pair of conductors will also generate opposite electromagnetic fields, and the two fields will cancel out each other when closely coupled. This means the current does not generate any electromagnetic field or, equivalently, that the pair of conductors have zero series inductance. Alternatively, if viewing from transformer design principles, the self−inductances of perfectly coupled windings will be decoupled by their mutual inductances.

Table 3. LOOP INDUCTANCE FROM THE IMPROVED BUS STRUCTURE

Parameter	Sample 1	Sample 2	Sample 3
dI (A)	118	118	116
dt (ns)	50	58	51
V_{DS} (V)	50.4	49.6	53.2
V_{bus} (V)	12		
L_{loop} (nH)	16.3	18.5	18.1
L_{stray} (nH)	11		
L_{bus} (nH)	5.3	7.5	7.1

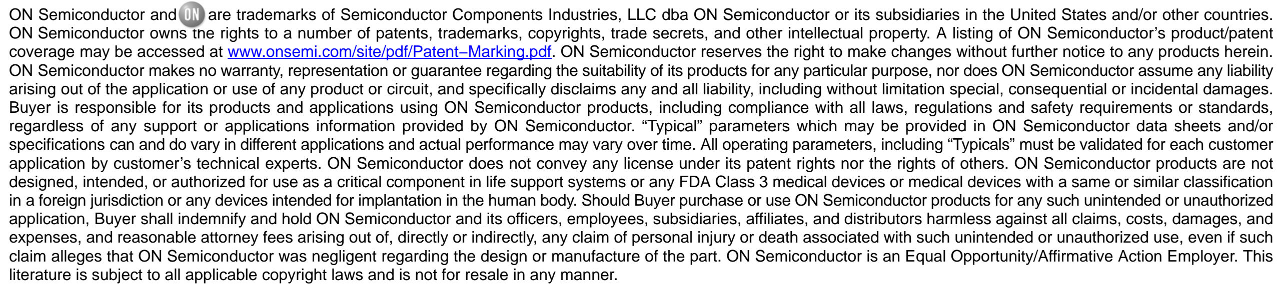
Conclusions

In this document, reasons of potential EOS failure have been investigated, solutions to avoid similar failure have been provided, and additionally, recommendations for inverter system design and implementation have also been provided, as the foundation of further application level optimizations.



Improved bus structure showing: (1) Enlarged contacting surface area between module pins and bus structure to reduce stray inductance from lead pins, (2) Overlay coupled positive and negative power plate to decouple series inductance from bus bar, (3) Parallel multiple electrolytic capacitors for lower ESR and ESL, (4) Ceramic snubber capacitors been put close to module, strengthen DC voltage stiffness during switching transient. (5) Common mode filter to reduce noise interference among different systems.

Figure 10. Improved Bus Structure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