IGBT Basic II

AN-9020/D

SECTION I. GATE DRIVE CONSIDERATIONS
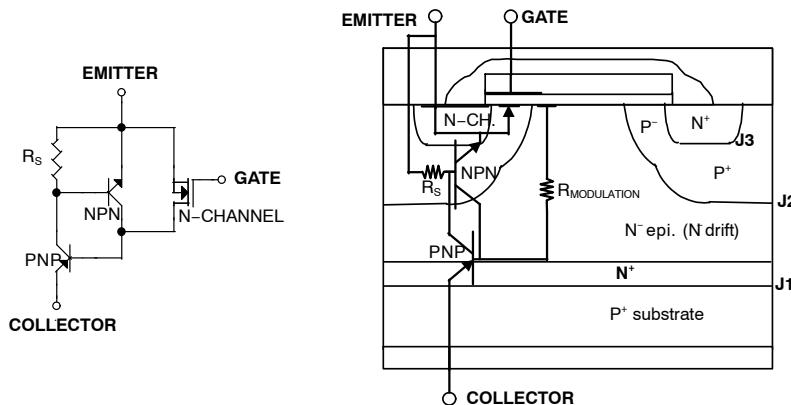
Introduction − IGBT Structure

Figure 1. Structure of IGBT

The structure of the IGBT is the combination of the P+ layer added to the MOSFET structure as shown in Figure 1. The IGBT, constructed by adding the P+ layer, has the characteristics of the power transistor (BJT), which has high conductivity in its n−layer by injecting hole into the n−layer with high resistance. As such, IGBT is easier to drive, and it combines the advantages of MOSFET's faster switching speed and power BJT's lower conduction loss. IGBT is a useful device in that it overcomes the shortfall of MOSFET in that it is not suitable for high voltage, high current applications due to its high conduction loss, while IGBT has the advantage over power BJT, which has limitations in high frequency applications due to its switching speed. Demand for IGBT is increasing in mid to low power applications, and the applications are becoming more varied, as the capacity of IGBT continues to increase. In order to obtain the optimum performance from the IGBT with such characteristics, it is of foremost importance to design a gate drive that is suited for the application. As such, this paper intends to discuss the characteristics of IGBT and some issues to consider in designing a gate drive as well as providing necessary information in designing an application system to help engineers who design systems using IGBT.

Gate Drive Considerations

The IGBT can change its switching properties through the gate drive, so designing a proper gate drive is extremely important to the performance of the IGBT. So−called the "best performance" of the IGBT is different by application,

which means the design of the gate drive must be different depending on the application of each IGBT. For example, hard−switching applications such as motor drives or UPS, the switching waveform must ensure that the IGBT's loci of operation do not exceed SOA, and the gate drive parameters must be set accordingly. This means that it may be necessary to sacrifice switching speed from the loss of switching as well as $V_{CE(sat)}$ from the loss of conduction. On the other hand, in soft−switching applications, there is less burden from SOA, so it is possible to select a device with $V_{CE(sat)}$ and t_f with good char− acteristics, and it is possible to choose the trade−off between $V_{CE(sat)}$ and t_f with gate drive parameter depending on whether switching loss or on−state loss is greater. In this chapter, we would like to examine characteristics of IGBT and gate drive parameter, discuss the relation− ships between the two, and some issues to consider in designing a gate drive.

IGBT Switching Waveforms

Switching waveform of the IGBT in a circuit under a clamped inductive load (CIL) is shown in Figure 2. This waveform can be applied to both inverter and chopper circuits using inductive load. This is a real waveform that reflects the effects of diode recovery and stray inductance, and principles of their operations will be considered by region. Consolidated understanding of IGBT's real application switching waveforms and principles of operation is necessary in designing an IGBT gate drive.
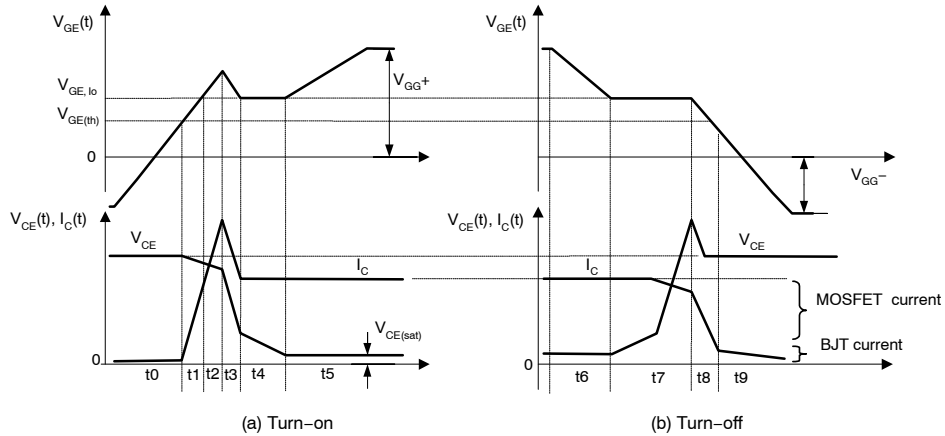
Analysis of Turn−on Transient

(a) Turn−on   (b) Turn−off
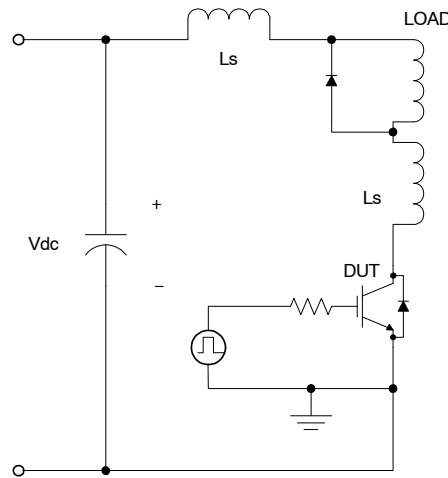
Figure 2. IGBT Switching Waveforms

Figure 3. IGBT Switching Test Circuit

The test circuit illustrating the characteristics of IGBT is shown in Figure 3. In addition, Figure 2 shows IGBT switching waveforms obtained from the test circuit in Figure 3. IGBT's turn−on switching waveform is very similar to MOSFET switching characteristics, and turn−off switching characteristics are similar as well except IGBT's tail current. The following are descriptions of each region shown in Figure 2 and their principle of operation.

Turn−on Transient Region

t0 region

This is a region where i_G (gate current) charges parasitic input +capacitance C_{ge}, C_{gc}, and v_{GE} rises to $V_{GE(th)}$. Waveform of increasing v_{GE} is shown to be linear, but in reality it is an exponential curve with time constant of $R_G(C_{ge}+C_{gc})$. In this region, there is no change in v_{CE} and i_C. Delay time is defined as the time it takes for the gate voltage to go from 10% of V_{GG+} to the moment i_C becomes 10% of I_O. As such, most of turn−on delay falls in this region.

t1 region

As v_{GE} passes $V_{GE(th)}$, a channel is formed on p base region below the gate oxide, and cur− rent begins to conduct. During this time, IGBT is in an active region, and i_C increases in relation to v_{GE}, which rises beyond $V_{GE(th)}$. In this region, i_C increases in relation to the increase in v_{GE} and finally reaches the full load current (I_O). In t1 and t2 region, the value of v_{CE} appears shaved off compared with the value of V_d. This is because $V_{LS} = L_S*di_C/dt$, which is the volt− age across L_S as shown in Fig. 2, while i_C current increases. The amount shaved off is related to the size of di_C/dt and L_S, and its shape changes according to i_C pattern.

t2, t3 region

In i_D pattern, diode current decreases beginning in the t1 region. However, it does not immediately decrease to 0A, but there is a reverse recovery, as it flows in the reverse direction. This current is added to i_C current to show the same pattern as i_C in the t2 and t3 region. At this time, voltage

across the diode recovers and increases, while v_{CE} falls, and it falls rapidly as C_{gc} has small value when v_{CE} has high value. Due to this phenomenon, dv_{CE}/dt is rather large at this time. In t3 region, C_{gc} absorbs and discharges the current from the gate drive and the discharge current from C_{ge}. At the end of the t3 region, reverse recovery of the diode comes to a close.

t4 region

Also in this region, i_G is charging C_{gc}, and v_{GE} maintains $V_{GE,Io}$, and i_C maintains full load current (I_O), while v_{CE} falls at a rate of $(V_{GG}−V_{GE,Io})/(R_G C_{gc})$. By this time, v_{CE} has diminished significantly, and there is a voltage tail, as C_{gc} has a large value when v_{CE} is low.

t5 region

In this region, v_{GE} increases again until V_{GG+} with $R_G(C_{ge}+C_{gc,miller})$ as time constant. $C_{gc,miller}$ is the C_{gc} that rose from low v_{CE} value due to the miller effect. In this region, v_{CE} slowly diminishes to the collector−to−emitter on−state voltage and becomes completely saturated. This is because the IGBT pnp transistor portion is slower than the MOSFET portion in crossing the active region to reach on−state (hard saturation) as well as the effect from $C_{gc,miller}$.

Turn−off Transient Region

t6 region

This is the region of $t_{d(off)}$ (Turn off delay time), where v_{GE} falls from injected V_{GG+} to $V_{GE,Io}$ with a time constant of R_G $(C_{ge}+C_{gc,miller})$. At this time, there is no change in the values of v_{CE} or i_C.

t7 region

v_{CE} increases in this region, and the rate can be controlled with R_G as shown in the equation below:

$$\frac{dv_{CE}}{dt} = \frac{V_{GE,I_o}}{C_{res} \cdot R_G}$$

t8 region

In this region, the value of v_{CE} is maintained at v_d, while i_C decreases at a rate equivalent to the following equations. The rate of increase can also be controlled with R_G.

$$\frac{di_C}{dt} = g_{fs} \cdot \frac{V_{GE,I_o}}{C_{IES} \cdot R_G}$$

Like the turn−on transient region, there is over−voltage in t7 and t8 regions, as the voltage $V_{LS} = L_S \times di_C/dt$, which is injected into the stray inductance from the effect of di_C/dt, is added to the C−E region of the IGBT. t8, which is the first of the 2 regions where i_C decreases, is the region where MOSFET current disappears from the IGBT's i_C.

t9 region

BJT current of the IGBT's i_C disappears in this region, and this current is often called the current tail. It is caused by the recombination of the minority carrier (hole), which is injected into the N− drift region Due to this region, IGBT switching characteristics are inferior to that of the power MOSFET.

Gate Drive Design Basics

IGBT can be made to conduct when appropriate voltage (generally +15V) is introduced to the gate of IGBT, and the current is cut off if v_{GE} is below the threshold voltage ($V_{GE(th)}$, generally, less than 0V). Under the ideal condition, the voltage should be zero between the collector and the emitter (V_{CE}), and it should be zero in blocking, and its switching loss is also zero, since IGBT is generally a device that works in a switch−mode, not as a linear amplifier. Although it is not possible in reality, a good device should approach these conditions in operation. In order to do so, one must select a device that satisfies the ideal conditions as much as possible, then the optimum gate drive must be designed for the system to realize the best performance. V_{GG+} (positive gate bias voltage), R_G, max I_G, drive layout, drive power rating are some of the basic parameters necessary in designing a gate drive. It is necessary to understand each of the parameters as well as the characteristics of IGBT switching in order to design a gate drive. The value of V_{GG+} are related to on−state loss and switching speed, while the value of R_G is related to switching performance. In addition, if the power of a gate drive, or supply capacity of I_G is not enough, then the values of V_{GG+} and R_G become meaningless. At the same time, attention is required in the layout of the gate drive to prevent induced turn−on due to dv/dt. The aforementioned parameters will be discussed in following sections based on the commonly used half bridge topology (Figure 3).

(Devices with better performances, in general, have lower power dissipation. Minimizing power dissipation is directly related to the cost, size, efficiency and fidelity of the overall system. As such, other topics discussed in this chapter must be understood with device power dissipation in mind.)

V_{GG+}

V_{GG+} is the voltage across the gate and the emitter terminal during conduction, and it is one of the most important parameter in designing the gate drive. The value of V_{GG+} must be made with considerations for trans−conductance characteristics or I−V characteristics shown in the data sheet; diagrams of SOA (Forward Bias, Reverse Bias, Short Circuit); maximum values of I_C and V_{CE}; value of t_f, and the interrelationships among these parameters must be considered.

Minimum/Maximum Rating

The maximum value of V_{GG+} is determined by the isolation limit of the gate oxide. If a voltage exceeding the maximum rated voltage between the gate and the emitter, then the gate oxide would be destroyed and become useless. As such, the absolute value of V_{GG+} in application must be smaller than the maximum value. The minimum value of V_{GG+} is the lowest value within the limits of saturation during conduction.

Effect on State

For the same value of I_C, $V_{CE(sat)}$ is inversely related to the value of V_{GG+}. The smaller the V_{GG+}, the thinner the channel between n+ layer and n−drift layer becomes, and the resistance in the channel increases. Due to the conductivity modulation effect not found in MOSFET, volt− age drop in the n−drift region is significantly smaller than in MOSFET. As such, the portion of resistance in the channel increases in the voltage drop between the collector and the emitter during on−state. Considering the aforementioned factors, V_{GE} decreases during IGBT switching, and the channel becomes thinner to increase resistance. This leads to an increase in $V_{CE(sat)}$, and on−state loss becomes greater. As such, it would be better to use the largest possible value of V_{GG+} from the respect of on−state loss. In applications where on−state loss takes a large portion, it is important to increase the value of V_{GG+}, lowering $V_{CE(sat)}$ in order to reduce conduction loss. For more detailed values, refer to the transfer characteristics curve in the data sheet. (Example: Figure 4)
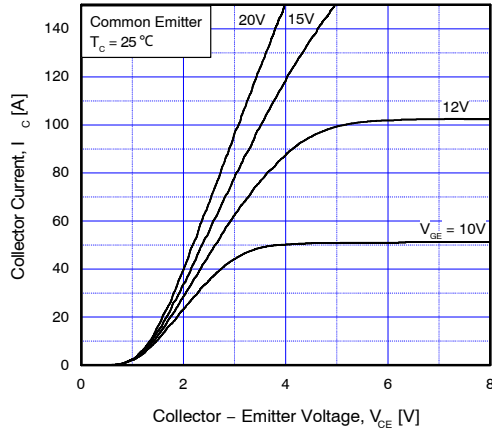

Figure 4. onsemi SGL50N60RUFD Typical Output Characteristics

Effects on Turn−on

As V_{GG+}, ($V_{GG+} − V_{GE(th)}$) increases, switching time decreases and switching loss becomes smaller. Greater the I_G flowing into the gate during turn−on, the quicker it charges C_{ge}, and V_{GE} increases rapidly, which leads to a quicker increase in I_C. As seen in the following equation, I_G increases as V_{GG+} increases, and it leads to an increase in di_C/dt.

$$I_G = (V_{GG+} − V_{GE}) / R_G$$

Since recovery characteristics of the freewheeling diode (FWD) on the opposite side are a function of di_C/dt, peak recovery current (I_{rr}) of FWD (refer to Figure 2) (which is IGBT's over−cur− rent), over−voltage of FWD and dv_{CE}/dt are affected by changes in di_C/dt. When di_C/dt increases, over−current of IGBT and over−voltage stress of FWD increases, while it also causes increases in falling dv_{CE}/dt of IGBT and rising dv_{CE}/dt of diode voltage on the opposite side. Large values of di_C/dt and dv_{CE}/dt indicate that switching speed, or switching loss, is small, which could be an advantage, but from the perspective of limiting EMI

noise, it is necessary to set an upper limit. Fundamental method to limit over−current in I_C is to select a device whose built−in diode has better recovery characteristics. However, once the device has been decided and setup is completed, I_C peak current can be kept below the rated amount by reducing V_{GG+} or by increasing R_G. IGBT's over−current and the FWD's over−voltage on the opposite side can also reduce di_C/dt by limiting V_{GG+} or by increasing R_G. In selecting a device with built−in diode (co−pak IGBT), the peak value of the over−voltage must not exceed the rated voltage of the diode on the specification. The snappiness factor (refer to Figure 2: S=tb/ ta) of the built−in diode must not be too small.

Effect on the Short Circuit Capability

IGBT's short−circuit endurance capability can be controlled with the value of V_{GG+}. The smaller the V_{GG+}, the smaller clamping voltage during short circuit and power dissipation as shown in Figure 3. In another word, short circuit endurance time increases. With these characteristics, short circuit protection can be devised with V_{GE}. However, with increases in V_{GG+}, one must assume increases in on−state losses. RUF Series by **onsemi** can withstand short circuit condition for about 10 μs.

Effect on Turn−off

As the turn−on characteristics of IGBT are largely affected by V_{GG+}, turn−off characteristics of IGBT are affected by $V_{GG−}$ (negative gate bias voltage). However, the tail section of the I_C comes from the BJT characteristics of IGBT, which is an integral nature of the device and can− not be controlled from outside with $V_{GG−}$. As the value of $V_{GG−}$ becomes greater, the turn−off switching loss of I_C decreases. As the value of $V_{GG−}$ increases, di/dt of I_C increases, and di/dt of I_D increases by the same amount. di/dt of I_D and stray inductance L_S is added to V_{DC} according to the equation, $V = L_S * di/dt$ to form over−voltage. As the absolute value of $V_{GG−}$ increases, di_C/dt and dv_{CE}/dt increases, and as di_C/dt increases, the over−voltage of V_{CE} increases. The peak value of this over−voltage must not exceed IGBT's maximum rating, so the value of $V_{GG−}$ can be reduced to control it. On the other hand, as the value of $V_{GG−}$ is increased, the possibility of dv/dt shoot through (R_G: refer to Effect on turn−on) is reduced.

R$_G$

Effect on Turn−on

Series resistance (R_G), which is connected to the gate, is a parameter that has a significant effect on switching waveform. When R_G decreases, di_C/dt and dv_{CE}/dt increases in both turn− on and turn−off, and switching loss becomes smaller. There are some important significant advantages when R_G is smaller, which included improved dv/dt noise immunity. Dangerous surge voltage on the IGBT gate caused by Miller effect or dv/dt coupled noise, which means induced turn−on can be avoided. When one side of IGBT of the half−bridge turns on, then the freewheeling diode

(FWD) of the IGBT on the opposite side recovers reverse voltage and there is dv/dt. This dv/dt can instantly conduct IGBT on the other side. As the parasitic capacitance C_{cg} between the gate and the collector on the other side is charged by dv_{CE}/dt at the IGBT on the other side, this current then flows to the gate to reduce voltage. This leads the gate voltage to exceed the threshold voltage momentarily, then the IGBT is in conduction. This is called dv/dt shoot through. This causes unnecessary loss, but reducing R_G decreases the amount of reduction in voltage at the ends. Increasing the value of V_{GG-} is also effective as it reduces the possibility of IGBT's gate voltage to rise above $V_{GE(th)}$. Despite these advantages, the minimum value of R_G is limited, and it is limited by the FWD recovery characteristics of the IGBT on the opposite side. di/dt and dv/dt stress of FWD on the opposite side change with the value of R_G under hard switching inductive load. If di_C/dt is large there can be oscillation, and when di_C/dt increases, dv_{CE}/dt also increases. As di_C/dt becomes greater, the greater the possibility of dv/dt shoot through on the IGBT on the opposite side. Under this situation, one must assume the turn−on switching loss, and increase R_G to reduce FWD stress.

Effect on Turn−off

Although R_G is small, it has the same effect as increasing V_{GG-}. As R_G becomes larger, turn−off fall time increases and switching loss rises. However, the effect is generally less than during turn−on. Since I_C current is divided into MOSFET and PNP transistor, only the current from MOSFET can be controlled during turn−off. From the perspective of dv/dt noise immunity, dv/dt malfunction from the IGBT on the opposite side can be reduced during turn−on if the value of R_G is large. On the contrary, from the off state, the possibility of dv/dt shoot through during turn−on from IGBT increases. As such, if different values of turn−on R_G and turn−off R_G are used, the values can be adjusted accordingly in consideration of the two cases.

Gate Drive Power Requirement

The proper gate voltage does not mean the proper operation of the IGBT. When IGBT turns on and off, then the gate is either charged or discharged and the current IG flows out of or into the gate. The value of the current should be enough to charge and discharge in order to properly turn on or turn off the IGBT. The waveform is shown in Figure 5.
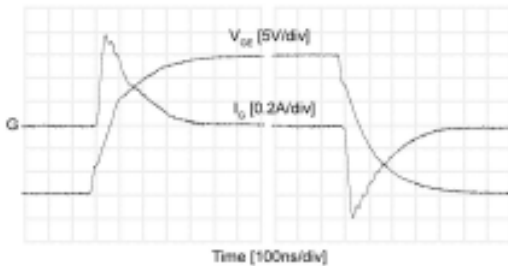

Figure 5. IGBT V_{GE}, I_G Waveform

Ate charge (Q_g) of the IGBT is greater, or smaller value of R_G has been chosen for faster operation of the IGBT, the peak value I_G current becomes greater. According to the value at the peak, it may be necessary to amplify the power at the gate by using push−pull circuit. Q_g is greater for devices with higher rated current, and the amount of necessary gate current increases accordingly. When power amplification is necessary because the necessary value of the current is large, careful selection in the device for push−pull is needed. This device must be able to provide the amount of current demanded by the gate and must have quick response.

One of the most important values necessary in designing a gate drive is the maximum value of I_G, which is provided by the gate drive. Average value of I_G provided by the gate drive can be obtained easily by dividing the average current by the voltage, but the maximum value of I_G is more meaningful. This is because the types and the current rating of the devices that make up the gate drive are determined by the maximum instant current. In general, the amount of cur−rent the gate drive must supply increases in relation to the operating frequency as shown in the following equation, but a gate drive with a few Watts is enough for several Amp IGBT and operating frequency of several 10s of kHz. The total power by the gate drive can be computed with the following equation

$P_{GD\_TOTAL}= f \times P_{SW} + P_{GD\_INTERNAL}$

P_{GD_TOTAL} : Total supplied power to the gate drive

P_{SW} : Sum of the charge and the discharge power respect to pulse $P_{GD\_INTERNAL}$: Power consumed by gate drive itself

$P_{SW} = Q_{IN} \times V_{GG6}$

V_{GG} : V_{GG+} - V_{GG-}

It is possible to use what is generally called gate charge (Q_g) for Q_{IN}, but if in this case, it is possible to use the amount of current the gate drive must provide the IGBT in a single pulse. As such, we can obtain the value by integrating the IGBT I_G curve on the oscilloscope. This becomes a valid value in obtaining gate drive current through the above equation. Gate charge can be obtained from gate capacitance, and its curve is available on the data sheet, but its value would be smaller than Q_g or Q_{IN} if gate capacitance is used simply with the equation $Q = C \times V$. This is because gate capacitance has non−linear dependency on the gate and the collector voltage.

Power consumed by the gate drive itself must also be considered as shown in the above equation, and it must also take into consideration that the amount of power consumed increases as the operating frequency increases. As such, there must be a safety margin in the calculation of P_{GD_TOTAL}. In application, the maximum amount of power may only be a few watts, but the maximum current may be more than a few Amps. The maximum current can be obtained with the following equation:

$I_{G(max)} = V_{GG} / R_{G(min)}$

When the maximum current is actually measured, one must be aware that it may be less than the calculated amount due to the falling voltage on the wire and stray inductance. When IGBTs are connected in parallel and are operated at a low frequency, low RMS current could lead to a mistaken complacency. However, under such situation, the maximum current would be twice as large, since there are 2 IGBTs in operation, and one must be careful that it could lead to the overload of the power supply of the gate drive. Wattage of the R_G can be decided with the maximum calculated amount of current.

Gate Drive Layout Considerations

Effect of Gate Line Inductance on the Induced Turn−on

Possibility of induced turn−on is greater, as the gate drive impedance is increased during turn−on and turn−off transient due to stray inductance from the line connected with the gate. As gate impedance becomes smaller, more current flows through R_G to reduce the charging current of C_{ge}, which causes the amount of increase in V_{GE} to reduce. In order to prevent this, leakage inductance from DC power supply must be minimized, and R_G should be kept at minimum.

Power Source Stabilizing Capacitor

During IGBT switching, current flows to the gate, and at that time, supply voltage of the gate circuit can oscillate. As a result, the gate drive loss can exceed the designed amount, or it could reduce the short circuit capability. In such case, it is advised to keep PCB pattern wide and flat and use enough capacitor for supply voltage stability.

Isolation Problem

In half bridge topology and similar systems, the upper IGBT gate drive circuits must be insulated from the bottom IGBT circuits. The control board and the gate drive must also be insulated because the upper IGBT emitter free floats as the IGBT switches. As the power DC voltage rises, the insulating voltage should also rise accordingly. In general, the insulating voltage should be at least twice the rated voltage for the IGBT. In addition, care has to be taken with the noise that comes about from insulating interface. Immunity to noise differs depending on the how and where the circuits lines are placed, so wiring and placement should be designed to minimize parasitic capacitance. Parasitic capacitance should be minimized to reduce C×dv/dt coupling noise between neighboring drive circuits. When using a common transformer to provide current to both the upper and the lower gate drive, the wire must be wound to minimize combined capacitance. In using opto−coupler, the opto−coupler must have insulating capacity with high common mode voltage and transient noise immunity. Upper and lower, or different types of gate leads of the gate drive must not be wound together.
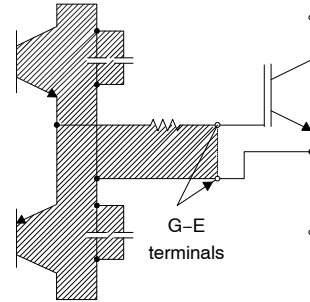
Wiring Pattern

Figure 6. Gate Drive Pattern 6

The final push−pull wiring pattern should be short and thick, and if a direct connection between the gate drive and the IGBT is not possible, then gate wire and the emitter wire could be twisted to reduce stray inductance. In addition, if the area of the loop that encompasses the final push−pull stage, the power source pattern, R_G, and G−E terminals of the IGBT is minimized as shown in Figure 6, effect on the V_{GE}, from di_C/dt could be minimized when V_{GG+} is injected.
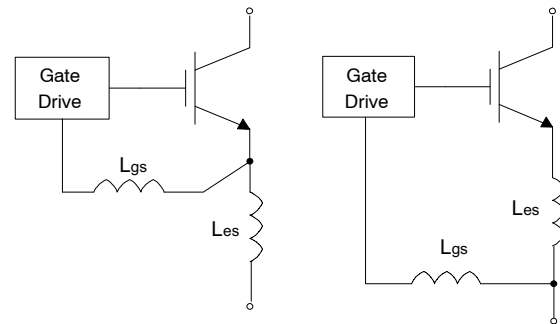
Common Emitter Problems

Figure 7. Common Emitter

At the time of switching, voltage is induced across the stray inductance of the power circuit because of di/dt from the main current. When control signals from the gate drive and the same path as the main current are used, gate voltage decreases during turn−on, and voltage is added to the gate voltage during turn−off to slow the turn−on/turn−off. As such, it is better not to share stray inductance between control emitter terminal and power emitter terminal. As such, control emitter terminal and power emitter terminal should be separate. If the two terminals are together, common emitter inductance increases to slow the switching speed and switching loss.

Voltage oscillation, slow gate voltage rise, noise immunity deterioration, gate voltage reduction, falling gate protection circuit efficiency are some of the effects of the layout. These can be solved with designs to reduce stray

inductance and stray resistance such as making patterns short and thick. In addition, attention must be paid to the power circuit layout to minimize stray inductance. For example, the area of the closed loop must be minimized with DC link capacitor, load, power output, half−bridge leg and snubbers in the case of inverter, and in the case of resistive load, line to the load should be twisted to reduce the stray inductance of the power circuit, while snubber should be strengthened depending on the amount of over−voltage for inductive load. As the frequency increases, voltage could change due to slowing response of the dc link capacitor, so high−speed electrolyte cap for inverter should be used, and capacitor with better characteristics such as film capacitor should be inserted in the main cap in parallel.

Conclusion

We have examined some issues to consider in the gate drive of the IGBT. The gate drive, IGBT's operating circuits, are simple and lends it self easily to miniaturization, so the system designer can design the gate drive, but it is not an easy task to design an optimum gate drive for the system. IC type gate drive solutions are designed to fit the needs of the user's system to customize some significant parameters by linking simple passive devices. Furthermore, they have built−in OCP (over current protection) and SCP (short circuit protection) functions to easily build a more stable system. It is becoming even more popular with the introduction of the IPM (intelligent power module), which puts inverter with gate drive, which is used often in the industrial application, in the same package.

SECTION II. IGBT PROTECTIONS

Introduction − IGBT Failure Mechanism

IGBT applications with power converter received high electrical and thermal stress under short−circuit or turn−off switching of clamped inductive load (CIL). As such, the ability to endure stress is one of the important requirements.

If there is a large power loss within the device due to electrical stress, much heat is generated to the limitations in packaging and due to semiconductor's thermal parameters. It would lead to thermal breakdown if this continues. Hot−spot generation from impact ionization and current crowding are the reasons. The existence of parasitic thyristor also has an effect on the robustness of the device. Latch−up of the parasitic thyristor is also a reason for breakdown. Design for IGBT comes from an understanding of the mechanisms of various stresses that can lead to the destruction of the device, and the IGBT is optimized to withstand stress from a large current. SOA evaluation methods for the device are different for short−circuit in experiment and for clamped inductive switching stress. IGBT's short circuit performance generally determines forward bias SOA, while turn−off at clamped inductive load determines reverse bias SOA. Position of thermal failure

within the latch−up−free PT IGBT chip is known to be different from the two above switching stress.

There have been much research into preventing device destruction from short−circuit and turn−off switching stress of CIL. We would like to discuss them in relation to SOA and protection mechanism.

FBSOA and Short Circuit Destruction

FBSOA

Forward bias safe operating area (FBSOA or SOA) is generally referred to as the current and voltage limits where the device can operate normally during on state. FBSOA of IGBT is illustrated in Figure 8. The SOA of IGBT is nearly a rectangle for a short period of time, but as shown in Figure 8, FBSOA decreases as on−time increases. Lower limit is determined by DC operation. Parasitic thyristor latch−up and thermal breakdown are the two major failure mechanisms of IGBT under extreme stress. Even the device that prevents static latch−up could be prone to dynamic latch−up. In the device that prevents latch−up, carrier multiplication, which was accelerated by thermal effect, becomes the cause of breakdown. It is limited by parasitic thyristor latch−up at high collector current and dynamic avalanche break−up at high voltage region.
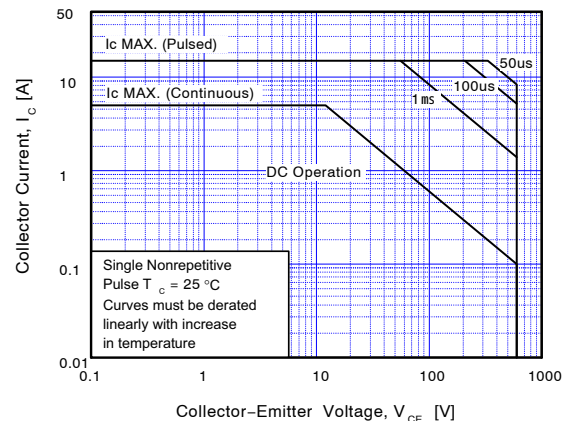
Figure 8. Typical IGBT FBSOA

Short−circuit threatens this FBSOA. If there is a short−circuit, IGBT's I_C increases. However, depending on the IGBT's output characteristics—I_C current is limited by the value of V_{GG+}, but since the voltage is high when the circuits are shorted, the device must withstand extreme loss of power. As time passes, temperature rises from power loss, and the temperature of the device continues to increase. In this case the IGBT must turn off within 10 μs.

In order to protect the IGBT from short circuit situations, the device's short circuit capability must first be known. In general, the simplest short circuit test is testing the IGBT's short circuit capability. However, this is different from real application short circuit conditions. In this test, it is not possible to see the effects of dynamic dv/dt, which induces

IGBT's latch−up. It is possible to obtain short circuit time with short circuit testing of different products from many companies. In general, short circuit time becomes longer with high saturation voltage and $V_{CE(sat)}$. (In measuring $V_{CE(sat)}$, gate voltage should be enough for the minimum value of $V_{CE(sat)}$, and that level must be maintained during fault test.)

Types of Short Circuit

Short circuit can happen while IGBT's normal function. Short circuit can be divided into two different types. The first is short−circuiting when the device was in on state, which is called "fault under load" and the second is a circumstance where the device turns on under short circuit, which is called "hard switch fault".

Type I. Fault Under Load (FUL)
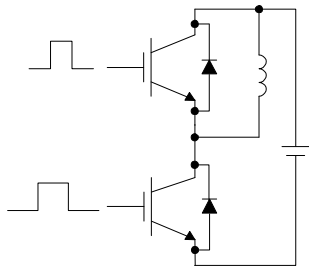
Figure 9. Fault Under Load Test Circuit
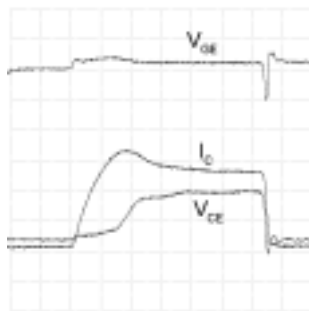
Figure 10. Fault Under Load Waveform

Fault under load (FUL) is a situation where short−circuit takes place when the device is in on state, so the V_{CE} is low before short circuit. In fault under load test circuit, short circuit can happen with a shoot−through when the IGBT on the opposite side turns on while the DUT remains turned on. Current rises quickly, and IGBT escapes from complete conduction and enters the active region. V_{CE} rises, and i_{CG} begins to flow in C_{CG}, which is Miller capacitance. At this time, if the gate resistance is large, it could rise above V_{GG+}. Fault current, $V_{GE}=V_{GG+}$, could rise above the limit for current, and the possibility of device breakdown increases. As such, it is recommended that low gate resistance be used as a way to guard against "FUL". Using low gate resistance would prevent a rise in V_{GE} during FUL to limit short current.

On the other hand, when short circuit is limited, loss is reduced and short circuit endurance time is increased. As short circuit endurance time increases, more time would be secured for the protection circuit to respond. As such, when short circuit is detected through a fault in the sensor circuit, reducing short current by lowering V_{GG+} is a good protection method. Using low value of resistance R_G is effective in reducing short current, but it has the opposite effects on over−voltage, dv/dt during turn−off, especially during short circuit, so the value of the resistance must be set with such trade off in mind.

Type II. Hard Switch Fault (HSF)

In this case, short−circuit is caused when the device is turned on from off state with DC link voltage applied to the device. In such case, di/dt and the value of the fault current are directly proportional to charging speed of the input capacitance. The fault current can be cut off by turning off the gate. The amount of the over−voltage created is directly proportional to "DC loop" inductance and the ratio of the fall in current when the fault current is cut off, which is di/ dt. Since the fault current is significantly greater than the rated current, large value of RG can be used to prevent the creation of large over−voltage due to di/dt.
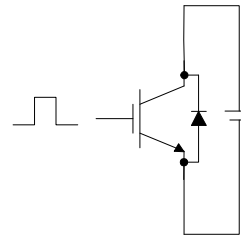

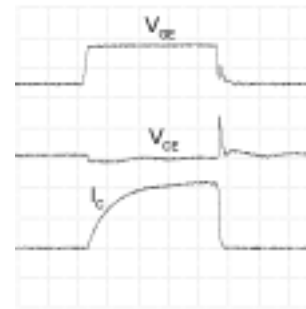**Figure 11. Hard Switch Fault Test Circuit6**

Figure 12. Hard Switch Fault Waveform6

V_{CE} voltage does not change significantly under hard switch fault, so the dv/dt is relatively smaller than in fault under load. Furthermore, Miller capacitance is small under high voltage. As such, Miller effect, which is an important issue for fault under load, is less significant under hard switch fault.

Short Circuit Protection

We have discussed types of short circuits, and several ways to prevent short circuits have been reviewed. However, methods mentioned above are not fundamental ways to deal with short circuit, so there has to be a way to safely turn off the device when it short circuits.

Protecting Against Over−current Condition

Over−current is when more than the rated current flows through the system, and it can be classified into over−load, short−circuit, turn−on over−current. In traditional applications, over−current is possible in several cases. Generally, over−current from over−load comes from inrush current, filter inrush and a rapid change in load during beginning of operation of electrical devices. In this case, we can only rely on short circuit capability of the device. Over−load, in general, lasts much longer than the IGBT's short circuit endurance time. As such, other methods must be sought to remove the overload. Closed loop control moderates the timing signal of the gate drive pulse, to modifies the time of switching, and this is used to keep the current output at a determined level. Response control of the control loop would have to be set to the rate of changes in the current and pace of the electrical devices or filter inductance. Protection from over−current due to short−circuit is different from turn−off over current. In the following sections, protection from short−circuit would be discussed.

Protecting Against Short Circuit Current Condition

In the overload situations mentioned above, removing the closed loop does not considerably shorten the life of the IGBT. On the other hand, short circuit provides worse condition for the life of the device than overload or the over−current at turn−on, and there are ground faults, terminal−to−terminal faults. Such short circuit current bypasses the electrical devices or filter inductance and increases rapidly for IGBT to flow. Conventional PWM loop controls power output, but it has no control over this type of fault. At the beginning of the fault, the IGBT must withstand with its own short circuit capability, and protection mechanism receives the fault signal to reduce the gate voltage while IGBT withstands the short circuit. However, if the fault disappears while during IGBT's endurance time, then the IGBT must continue to function and must not turn off unnecessary devices or turn off the entire system. The most notable is the IGBT turn−on over−current due to the reverse recovery current of the diode. As such, the protection circuit must be designed to return the circuit to normal operation if the fault is removed before the IGBT shuts down the system.

When conduction time increases, the border of SOA (SCSOA) decreases. Junction temperature increases instantly during on state, and as a result, the maximum possible controllable current decreases. As such, short circuit, whose current rises rapidly, must be turned off in a very short period of time, and the time from moment short circuit occurs to the moment it is turned off is should be within 10us. In addition, soft turn−off, which slowly cuts off the short circuit current, is necessary as abrupt turn−off leads to a large dv/dt, which increases the possibility for a latch−up. Principles of short circuit protection circuit design to be added in a gate drive can be summed up as the following:

- Fault must be detected as soon as possible.
- Must suppress fault current to secure more time for the protection circuit to respond, and send the gate off signal as quickly as possible.
- Induce soft turn−off to avoid the dangers of turn−off over−voltage.

We shall discuss the short circuit protection scheme in detail in the following sections.

Short Circuit Protection Scheme

There are certain conditions to be met in constructing a protection circuit. These conditions maximize the efficiency of the protection circuit and minimize the effect on other circuits. In order to obtain the protection function desired by the designer without sacrificing other functions, protection circuit design must satisfy the following conditions as much as possible. The conditions are as follows:

First, the protection circuit must shut down the IGBT before device failure. This is applicable at all times regardless of the conditions of operation for the IGBT. In addition, the protection circuit must limit the maximum fault current, and it must reduce stress on the device and the system, where high current flows. The device would have to be shut down more quickly if the maximum fault current is not limited.

Protection circuit must be responsive to both "fault under load" and "hard switch fault." In addition, it must not degrade switching or conduction characteristics, because this causes temperature to rise, and it is reflected in the efficiency and fidelity of components. Trip point, which is the minimum current recognized as short−circuit, must be easy to manipulate. Production cost must be minimized as it has a significant impact on the viability of the product.

The above conditions for protection circuits could be easy or difficult to meet depending on the fault detection method. The following are some typical fault detection methods and the effects on the conditions mentioned above.

Detection Through Resistance

This is fault detection method is the easiest to understand. Resistance is introduced at the passage of the load current, and it is made to produce voltage that can be monitored by the protection circuit. Sense resistor can measure current precise enough for over−current and fault detection. In addition, it can be used in analog feedback. However, it takes up a lot of space and requires a low inductance resistor, while self−inductance and wiring inductance within the sense resistor makes transient response characteristics get worse. When resistance is inserted into the DC loop, there is an adverse effect of inductance that deteriorates the system's performance. In addition, sense resistor is not insulated from the main power circuit, so the protection circuit must be

insulated from the logic circuit, which processes the sense signals. This can cause the system to become complex. In other cases, sense IGBT, which as a built−in sensing resistor, in the current sense path. This would be easier than installing it in the main current path. However, there are problems with high cost IGBT, limited uses, consistency among sense ratios among devices, and their trade−offs must be considered.
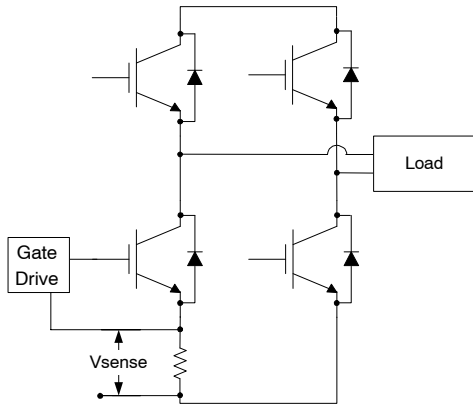

Figure 13. Short−circuit Sensing Circuit with a Sensing Resistor

Current Transformer

This is also an excellent fault detection method. Current transformer is placed on the power output needed to be monitored or on the conductor where short circuit current is expected to flow. This method has an advantage in that it allows the selection of the transformer for precise AC sensing. Since the transformer itself provides insulation between the power circuit and the protection circuit, there need not be additional considerations for insulation. It also provides high−level signal output with noise immunity since the protection circuit is driven by current. However, DC level cannot be detected without the use of the much more complex DC transformers. These are Hall Effect sensors, which are generally expensive. Aside from the Hall Effect sensors, current transformers are expensive in general, so they are not very economical. In addition, it is not an easy task to design a proper transformer since current transformers must operate in a large bandwidth. If a quick response to a rapid rise in fault current is necessary, it must operate in the MHz region as well as the system's minimum operating frequency.
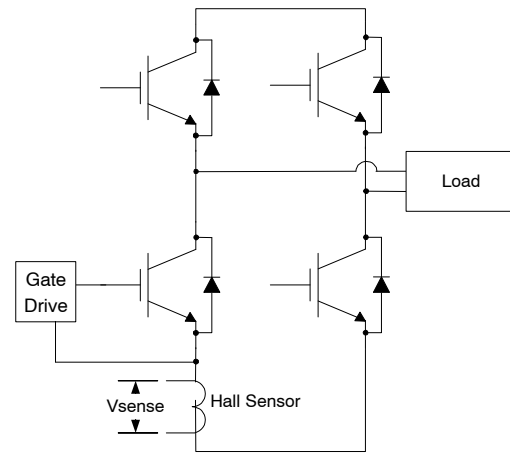
Figure 14. Short−circuit Sensing Circuit with CT

De−saturation Detection

This method detects V_{CE} in its operation. Short circuit has a switching device but no load, so all of the supplied voltage appears across the device. As such, during short circuit, V_{CE} of the IGBT diverges from the low on−state voltage and rise to DC loop voltage following the power output curve. If such high voltage appears in C−E terminal, where low on−state voltage region, then it is detected by the $V_{CE(sat)}$ sensing circuit and protection circuit. This method has no loss from components in detecting the current, which improves the overall efficiency of the circuit. In addition, there is less stray inductance due to the protection current, which enables faster operations. Furthermore, since it uses the characteristics of the device without any additional device in the circuit, it is an effective circuit in both AC and DC circuits. It has reasonable cost, and integration is easier as it uses simple passive devices. However, this method cannot detect exact amount of operating current that has been set, and it provides only fault/no−fault command. In this method, protection circuit is not insulated from the power stage, so gate signals are eliminated by IGBT, and insulation is necessary in the process of sending error mes− sage to the logic circuit. This circuit cannot be left in sensing mode at all times. It is not operational when IGBT off, but it becomes operational with the conduction signal. However, there must be a blanking time in the turn−on transient period to allow turn−on switching process. (refer to AN−9001)
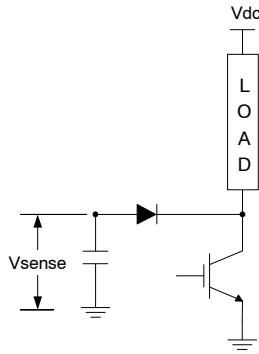
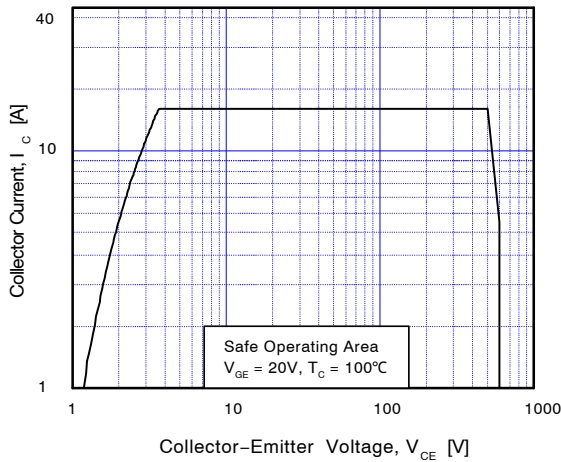**Figure 15. Short−circuit Sensing Circuit using De−saturation Method**

RBSOA

Figure 16. Typical RBSOA of IGBT

During turn−off transient, the gate bias with a positive value is switched to zero or to a negative value, which leaves the device with high voltage and hole current. Safe operating area for such operations is called RBSOA (refer to Fig. 9). Unlike FBSOA, snubber circuit design is important for safe operation during IGBT turn−off. Wider RBSOA can be obtained by reducing PNP transistor's current gain. If RBSOAs of p−channel and n−channel IGBT with identical doping profile and cell structure are compared, n−channel has larger SOA for the collector voltage (avalanche induced SOA limit), but the SOA for the collector current (current induced latch−up limit) is smaller. p−channel, on the other hand, is the opposite of n−channel. The limit of the avalanche induced SOA is affected by the impact ionization coefficient for the carrier of the depletion layer. Impact ionization coefficient of the holes transported from the n−channel IGBT is lower than that of electrons, which

allows n−channel IGBT to have excellent avalanche induced SOA limits. In addition, N base region sheet resistance of the p−channel IGBT is about 2.5 times lower than the P base region sheet resistance of the n−channel IGBT, so p−channel IGBT is superior to the n−channel IGBT in current induced latch−up limit.

Over−voltage Protection
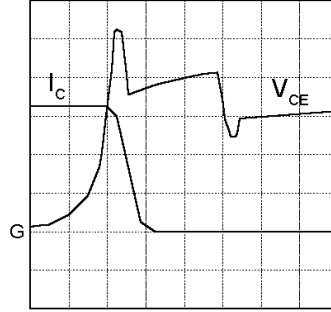
Figure 17. Turn−off Waveform of IGBT with Snubber

When a power device turns off rapidly, energy that has been stored in stray inductance is dissipated in the switching device. Because of this, there is voltage overshoot in either side of the device. The size of this transient voltage is directly related to the size of the stray inductance and the falling rate of the turn−off current. In particular, large capacity IGBT module switches a large amount of energy in a short time, and it is possible for a large current to be injected to lead to the destruction of the device. Such module for a large current is generally made of several IGBT chips. Individual chip switches a portion of the current in the amount equivalent to di/ dt as determined by the gate drive circuit. The total amount of the current and di/dt for the module is equivalent to the sum of the current and di/dt for each chip, respectively. The moment the device turns off to protect the IGBT during short circuit is the most dangerous moment. At this time, di/dt could exceed several thousand A/µs. To shut down the device to protect it from a fault condition, care must be taken to minimize the accompanying over−voltage, or the device could be destroyed. Over−voltage protection circuit optimized for normal switching may not be adequate in fault current shut−off process, so there must be additional response to over−voltage. Snubber circuit is often used as a protection circuit to protect normal switching. Over−voltage at turn−off can be suppressed by controlling the value of R_G or by inserting Cg, but these methods hinders other characteristics. As such, snubber circuit is often used. In the next section, types, characteristics as well as advantages and disadvantages of the snubber circuit are discussed.

Snubber Circuit

Types of Snubber Circuits and their Features

Snubber circuit is a supplementary circuit used in the converter circuit to reduce stress put on the power semiconductor. The ultimate goal of the snubber circuit is to improve the transient waveform. The snubber circuit suppresses over−current or over−voltage or improves dv/dt and di/dt to ease the transient waveform to reduce stress on the device. There are many uses for snubber circuits, but this discussion will center on its ability to suppress over−current at turn−off.

Snubber circuit can be divided into those connected in between the DC power supply bus and ground, and those connected to each IGBT. The first types of circuits include RC snubber circuits, charge and discharge RCD snubber circuits and discharge−suppressing RCD snubber circuits, and the second type includes C snubber circuits and RCD snubber circuits. The following are detailed descriptions of each snubber circuit.

RC Snubber Circuit

This snubber circuit is effective in turn−off surge voltage and is suitable for chopper circuits. It is also effective for oscillation by parasitic reactance and dv/dt noise. However, when it is applied in large capacity IGBT, resistance for the snubber must be set low due to dissipation of heat, so it has the disadvantage of worsening loading conditions at turn−on. Loss at snubber itself is quite large, so it is not suitable for high frequency. In very large capacity IGBT circuit, it is better to use small snubber "RC snubber circuit" along with the main snubber "discharge− suppressing RCD snubber circuit." When used together, it helps parasitic oscillation control of the main snubber loop. Main applications include arc welder and switching power supply.

Charge and Discharge RCD Snubber Circuit

This snubber suppresses over−voltage at turn−off to reduce switching losses at turn−off, and its effectiveness in surge voltage suppression is about average. The snubber capacitor is completely discharged at turn−on, and it is fully recharged at turn−off. Unlike the discharge−suppressing RCD snubber circuit below which acts as a clamp, this circuit reduces IGBT dv/dt during turn−off. As such, soft switching is possible, and IGBT loss is reduced. Since the structure of this circuit is snubber diode added to an RC snubber, snubber resistance can be increased, which alleviates the load problem at turn−on. It is effective chopper applications, which uses large current and low DC link voltage. Its advantage also includes no oscillation at its DC link voltage.

Power loss due to the resistance is as follows:

$$P = (L \times I_O^2 \times f)/2 + (C_S \times Ed \times f)/2 =$$

$$= 1/2 \times C_{sn} \times V_{pk}^2 \times f_{sw} \quad [W]$$

L: wiring inductance of the main circuit
I_O: collector current at IGBT turn−off
C_S: capacitance of snubber capacitor

Ed: DC supply voltage
f: switching frequency

However, losses from this circuit (mostly from snubber resistance) are significantly larger than the same in discharging suppressing RCD snubber circuit. As such, it is not suitable for high frequency switching applications. There is a lot of turn−on losses with bridge configuration. There are the disadvantages of relatively many parts and difficulties in selecting parts.

Discharge−suppressing RCD Snubber Circuit

Functions of this circuit are similar to those of voltage clamp snubber circuit. Snubber capacitor is charged to the DC link voltage while the IGBT is in conduction, and V_{CE} rises rapidly when IGBT is in turn−off. Due to the stray inductance of the DC loop, VCE rapidly rises above DC link voltage. When V_{CE} rises above DC link voltage, snubber diode is in forward biased conduction, and snubber begins operation. Energy stored in stray inductance moves to snubber capacitor. This capacitor absorbs the energy without a rise in voltage.

It has the advantage of small oscillation in DC link voltage, and it is most practical in mid−to−large current applications. Its effect on the turn−on voltage transient is neither large nor small. It is ideal for high frequency switching as its losses from the snubber circuits small. Losses from the circuit is as follows:

$$P = (L \times I_O^2 \times f)/2 \quad [W]$$

Its disadvantages are that it has many necessary parts and is less than effective on turn−off surge voltage. It is often used in inverters.

C Snubber Circuit

This is the simplest snubber circuit, so it has the advantage of suppressing over−current at minimum cost. It is effective in mid−to−low current, low power applications, and as the power level increases, it becomes more likely for the circuit to oscillate as the snubber capacitor and the main circuit inductance form LC resonance circuit. It is often used in inverters.
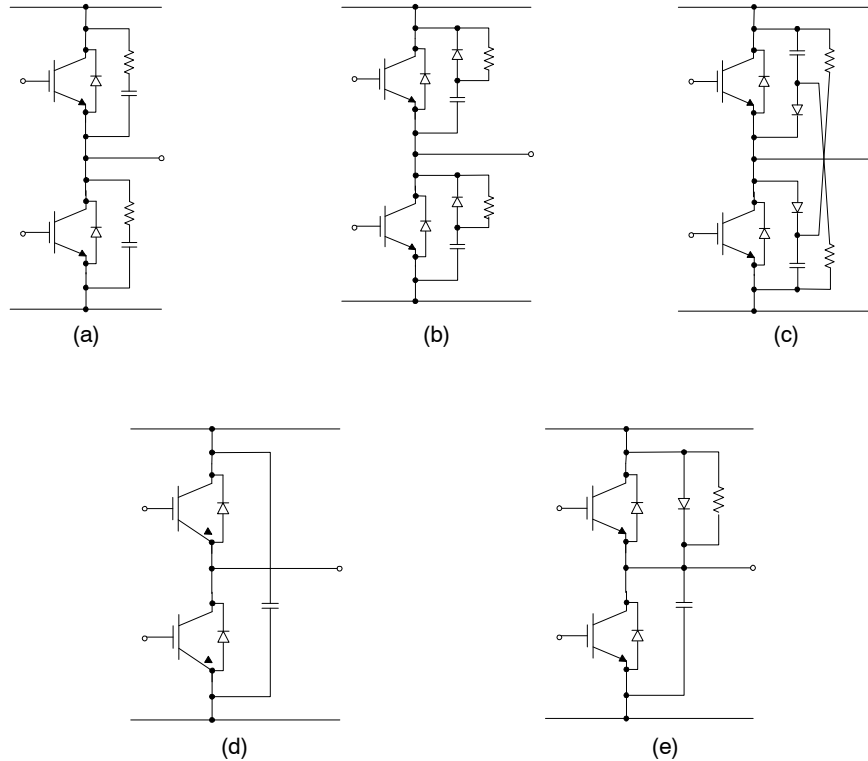
RCD Snubber Circuit

It operates in the same manner as the C snubber circuit, but it is different in that it operates during turn−off switching. It is a circuit that solved oscillation of the C snubber circuit by using the fast recovery diode. Energy that was stored in DC loop inductance moves to the capacitor while the IGBT turns off. The snubber diode prevents oscillation from taking place. Charge from the capacitor is discharged through the snubber resistor. (RC time constant should be about 1/3 of the switching cycle. (τ = T/3 = 1/3f))

This circuit reduces turn−off voltage transient directly. Switching waveform is significantly smoother and snubber loss is small. Effect on the turn−on voltage transient is fine, and it has the advantage of stable wave as the snubber diode blocks oscillation. It is practical in medium current range, but operation in large capacity IGBT, parasitic inductance

increases to present problems in controlling over−voltage. In such large current applications, discharge−suppressing RCD snubber circuits are generally used. Functions of the discharge−suppressing RCD snubber circuit are similar to the functions of the RCD snubber circuits, but the discharge−suppressing RCD snubber circuit has the advantage of smaller loop inductance as it is attached to the collector and the emitter of each device.

This circuit cannot use low inductance snubber capacitors designed to be attached directly to the IGBT, and the blocking diode added to the protection circuit can increase the total snubber inductance. Furthermore, if the recovery characteristics of the diode are not good, V_{CE} overshoot and dv/dt at either sides of the IGBT/diode, or the output voltage can oscillate. Turn−off mechanism is nearly the same as that of the discharge−suppressing RCD snubber circuit.

(a) RC Subber Circuit
(b) Charge and Discharge RCD Snubber Circuit
(c) Discharge−suppressing RCD Snubber Circuit
(d) C Snubber Circuit
(e) RCD Snubber Circuit

Figure 18. Scheme of Each Type of Snubber Circuit

References

[1] Malay Trivedi and Krishna Shenai, "Failure Mechanism of IGBT's Under Short−Circuit and Clamped Inductive Switching Stress", *IEEE Trans. Power Electronics*, vol. 14, no. 1, pp. 108−116, 1999.

[2] Rahul S. Chokhawala and Saed Sobhani, "Switching Voltage Transient Protection Schemes for High−Current IGBT Modules", *IEEE Trans. Industry Applications*, vol. 33, no. 6, pp. 1601−1610, 1997.

[3] Rahul S. Chokhawala, Jamie Catt and Laszlo Kiraly, "A Discussion on IGBT Short−Circuit Behavior and Fault Protection Schemes", *IEEE Trans. Industry Applications*, vol. 31, no. 2, pp. 256−263, 1995.

[4] Malay Trivedi and Krishna Shenai, "Internal Dynamics of IGBT During Short Circuit Switching", *IEEE BCTM*, pp. 77−80, 1996.

[5] J. Yamashita, A. Uenishi, Y. Tomomatsu H. Haruguchi, H. Dakahashi, I. Takata and H. Hagino, "A Study on the Short Circuit Destruction of IGBTs", *ISPSD*, pp. 35−39, 1993.

[6] Rahul Chokhawala and Giuseppe Castino, "IGBT Fault Current Limiting Circuit", *IEEE IAS*, pp.1339−1345, 1993.

[7] Tadashi Miyasaka and Shyuji Miyashita, "Protection of IGBT Modules in Inverter Circuits", Power Conversion, pp. 211−216, 1991.

[8] Hiroyasu Hagino, Junichi Yamashita, Akio Uenishi and Hideki Haruguchi, "An Experimen tal and Numerical Study on the Forward Biased SOA of IGBT's", *IEEE Trans. Electron Devices*, vol. 43, no. 3, pp. 490−499, 1996.

[9] Malay Trivedi and Krishina Shenai, "Trade−Off in IGBT Safe Operating Area and Performance Parameters", *IAS Conf.*, pp. 949−954, 1997.

[10] Yi Zhang, Saed Sobhani and Rahul Chokhawala, "Snubber Considerations for IGBT Applications", *IPEMC*, pp. 261−269, 1994.

[11] Malay Trivedi and Krishina Shenai, "Investigation of the Short−Circuit Performance of an IGBT", *IEEE Trans. Electron Devices*, vol. 45, no. 1, pp. 313−320, 1998.

[12] Malay Trivedi and Krishina Shenai, "IGBT Dynamics For Short−Circuit And Clamped Inductive Switching", *IEEE APEC,* vol. 2, pp. 743−748, 1998.

[13] Rahul S. Chokhawala, Jamie Catt, and Brian R. Pelly, "Gate Drive considerations for IGBT Modules", *IEEE Trans. Industry Applications*, vol. 31, issue 3, pp.603−611, 1995.

[14] Rahul S. Chokhawala, Jamie Catt, and Laszlo Kiraly, "A Discussion on IGBT Short−circuit Behavior and Fault Protection Schemes", *IEEE Trans. Industry Applications*, vol. 31, issue 2, pp.256−263, 1995.

[15] Malay Trivedi and Krishina Shenai, "IGBT Dynamics for Clamped Inductive Switching",IEEE Trans. Electron Devices, vol. 45, no. 12, pp.2537−2545, 1998.

[16] C. Aniceto, R.Letor, "How Short Circuit Capabilities Govern the Desired Characteristics of IGBTs" *Power Conversion − PCIM*, 1992,

[17] R. Locher, "Short Circuit Proof IGBTs Simplify Overcurrent Protection", *IAS*,1991

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