

# Automotive Power MOSFET Module

## NXV08H400XT1

### Features

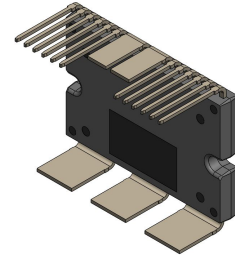
- 2 Phase MOSFET Module  
 At Customer Side this Module Can Be Used as 1/2 Bridge MOSFET Module by Combining 2 Phase Out Power Terminals
- Electrically Isolated DBC Substrate for Low Rthjc
- Compact Design for Low Total Module Resistance
- Module Serialization for Full Traceability
- Module Level AQG324 Qualified. Components Inside are AEC Q101 (MOSFET) & AEC Q200 (Passives) Qualified
- UL 94 V-0 Compliant
- This Device is Pb-Free and is RoHS Compliant

### Applications

- 48 V Inverter, 48 V Traction

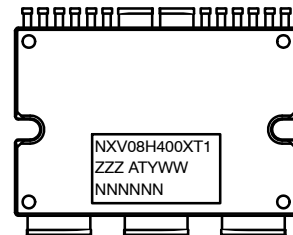
### Benefits

- Enable Design of Small, Efficient and Reliable System for Reduced Vehicle Fuel Consumption and CO<sub>2</sub> Emission
- Simplified Vehicle Assembly
- Low Thermal Resistance to Junction to Heat Sink by Direct Mounting via Thermal Interface Material between Module Case and Heat Sink
- Low Inductance



APM17-MDC  
 CASE MODHH

### MARKING DIAGRAM



NXV08H400XT1	= Specific Device Code
ZZZ	= Lot ID
AT	= Assembly & Test Location
Y	= Year
WW	= Work Week
NNN	= Serial Number

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# NXV08H400XT1

## ORDERING INFORMATION

Part Number	Package	Pb-Free and RoHS Compliant	Operating Ambient Temperature Range	Packing Method
NXV08H400XT1	APM17-MDC	yes	-40~125°C	Tube

## Pin Configuration

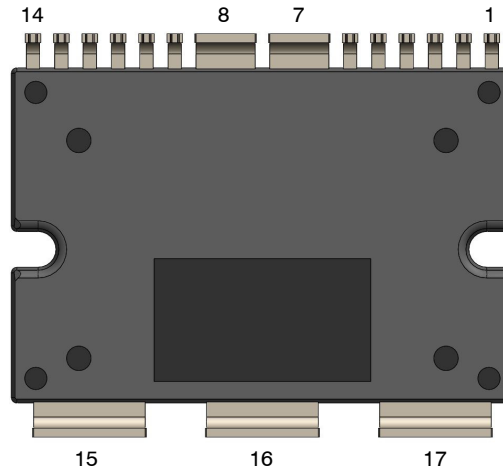


Figure 1. Pin Configuration

## PIN DESCRIPTION

Pin No.	Description	Remark
1	Q2 Gate	
2	Q2 Source Sense	
3	B+ #2 Sense	
4	Q4 Gate	
5	Q4 Source Sense	
6	NTC1	
7	Phase Out2	For 3 phase motor inverter, those 2 pins can be used as one phase out
8	Phase Out1	
9	NTC2	
10	Q3 Source Sense	
11	Q3 Gate	
12	B+ #1 Sense	
13	Q1 Source Sense	
14	Q1 Gate	
15	B+ #1	
16	GND	
17	B+ #2	

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## Block Diagram

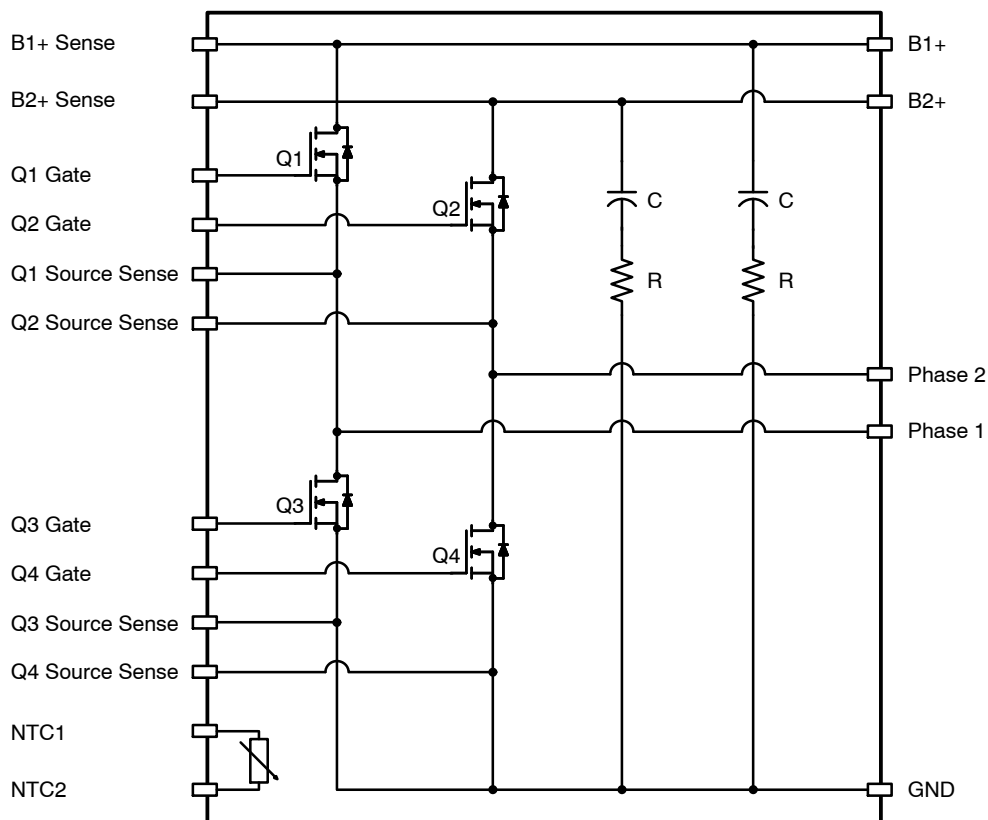


Figure 2. Schematic

### Flammability Information

All materials present in the power module meet UL flammability rating class 94V-0.

### Compliance to RoHS Directives

The power module is 100% lead free and RoHS compliant 2000/53/C directive.

### Solder

Solder used is a lead free SnAgCu alloy.

Base of the leads, at the interface with the package body should not be exposed to more than 200°C during mounting on the PCB, this to prevent the remelt of the solder joints.

### ABSOLUTE MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Max.	Unit
VDS(Q1-Q4)	Drain to Source Voltage	80	V
VGS(Q1-Q4)	Gate to Source Voltage	$\pm 20$	V
EAS(Q1-Q4)	Single Pulse Avalanche Energy (Note 1)	2445	mJ
$T_J$	Maximum Junction Temperature	175	$^\circ\text{C}$
$T_{STG}$	Storage Temperature	125	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.47\text{ mH}$ ,  $I_{AS} = 102\text{ A}$ ,  $V_{DD} = 72\text{ V}$  during inductor charging and  $V_{DD} = 0\text{ V}$  during time in avalanche.

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## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C, unless otherwise noted)

Characteristic		Condition	Min	Typ	Max	Unit
BVDSS	Drain-to-Source Breakdown Voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0 V	80	-	-	
VGS(th)	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 1 mA	2	-	4.6	V
VSD	Source-to-Drain Diode Voltage	I <sub>SD</sub> = 160 A, V <sub>GS</sub> = 0 V	-	0.79	1.1	V
RDS(ON)Q1, Q2	Q1, Q2 (High Side) MOSFET (Note 2)	V <sub>GS</sub> = 12 V, I <sub>D</sub> = 160 A, T <sub>J</sub> = 25°C	-	0.65	0.765	mΩ
RDS(ON) Q3, Q4	Q3, Q4(Low Side) MOSFET (Note 2)	V <sub>GS</sub> = 12 V, I <sub>D</sub> = 160 A, T <sub>J</sub> = 25°C	-	0.46	0.58	mΩ
IGSS	Gate-to-Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V, T <sub>J</sub> = 25°C	-100	-	+100	nA
IDSS	Drain-to-Source Leakage Current	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 25°C	-	-	2	μA
Module RDS(ON) for Q1 and Q2: From B+1 (or B+2), via Q1 (or Q2), to Phase Out 1 (Phase Out 2) (Note 3)		V <sub>GS</sub> = 12 V, I <sub>D</sub> = 160 A, T <sub>J</sub> = 25°C	-	0.96	1.32	mΩ
Module RDS(ON) for Q3 and Q4: From Phase Out 1 (Phase Out 2), via Q3 (Q4), to GND PINs (Note 3)		V <sub>GS</sub> = 12 V, I <sub>D</sub> = 160 A, T <sub>J</sub> = 25°C	-	0.9	1.25	mΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. All bare die MOSFETs have same die size and same level of R<sub>dson</sub> value. However the different R<sub>dson</sub> values listed in the datasheet are due to the different access points available inside the module for R<sub>dson</sub> measurement. Q3 and Q4 (Low side FETs) has the shortest R<sub>dson</sub> measurement path in the layout, in this reason, so Q3 or Q4 R<sub>dson</sub> value can be used for the R<sub>dson</sub> value per switch for simple power loss calculation.

Each R<sub>dson</sub> measurement paths are as below table, "Resistance Measurement Methods"

3. Module R<sub>dson</sub> means total resistance of the measurement path btw Power terminals, referring to the resistance measurement methods table.

## RESISTANCE MEASUREMENTS METHODS

	+ Force Pin#	- Force Pin#	+ Sense Pin#	- Sense Pin#
FET R <sub>dson</sub> Q1	B1+	Phase1	B1+ Sense	Q1 Source Sense
FET R <sub>dson</sub> Q2	B2+	Phase2	B2+ Sense	Q2 Source Sense
FET R <sub>dson</sub> Q3	Phase1	GND	Q1 Source Sense	Q3 Source Sense
FET R <sub>dson</sub> Q4	Phase2	GND	Q2 Source Sense	Q4 Source Sense
Module R <sub>dson</sub> Q1	B1+	Phase1	B1+	Phase1
Module R <sub>dson</sub> Q2	B2+	Phase2	B2+	Phase2
Module R <sub>dson</sub> Q3	Phase1	GND	Phase1	GND
Module R <sub>dson</sub> Q4	Phase2	GND	Phase2	GND

## TEMPERATURE SENSE (NTC THERMISTOR)

Parameter		Min	Typ	Max	Unit
Voltage	Current = 1 mA, Temperature 25°C	7.5	-	12	V

## THERMAL RESISTOR

Parameter		Min	Typ	Max	Unit
R <sub>thjc</sub> : Thermal Resistance Junction to case, Single Inverter FET	Q1, Q2, Q3, Q4 Thermal Resistance J-C	-	-	0.19	°C/W

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**ISOLATION VOLTAGE** (Isolation voltage between the Base plate and to control pins or power terminals.)

Test	Test Condition	Test Time	Min	Max	Unit
Leakage @ Isolation Voltage (Hi-Pot)	VAC = 3 kV	Time = 1 s	-	250	μA

**DYNAMIC AND SWITCHING CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
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**DYNAMIC CHARACTERISTICS**

$C_{iss}$	Input Capacitance	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, f = 750\text{ kHz}$	-	30,150	-	pF
$C_{oss}$	Output Capacitance		-	4,505	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	77	-	pF
$R_g$	Gate Resistance	$f = 750\text{ kHz}$	-	4.3	-	Ω
$Q_{g(tot)}$	Total Gate Charge	$V_{GS} = 0\text{ to }12\text{ V}, I_D = 160\text{ A}$	-	502	-	nC
$Q_{gs}$	Gate to Source Gate Charge		-	193	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	89	-	nC

**SWITCHING CHARACTERISTICS**

$t_{on}$	Turn-On Time	$V_{DD} = 48\text{ V}, I_D = 400\text{ A}$ $V_{GS} = 12\text{ V}, R_G(\text{on/off}) = 15/15\text{ }\Omega,$	-	710	-	ns
$t_{d(on)}$	Turn-On Delay Time		-	235	-	ns
$t_r$	Turn-On Rise Time		-	475	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	608	-	ns
$t_f$	Turn-Off Fall Time		-	290	-	ns
$t_{off}$	Turn-Off Time		-	898	-	ns

**DRAIN-SOURCE DIODE CHARACTERISTICS**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{RR}$	Reverse Recovery Time	$V_{DD} = 48\text{ V}, I_D = 400\text{ A}$ $V_{GS} = 12\text{ V}, R_G(\text{on/off}) = 15/15\text{ }\Omega,$	-	59	-	ns
$Q_{RR}$	Reverse Recovery Charge		-	1433	-	nC

4. Dynamic & Switching characteristics data is by characterization test result and guaranteed by design factors.

**COMPONENTS**

Component	Description	Type	Qty.	Specification
MOSFET	Bare Die	Bare Die	4	80 V 0.58 mΩ
NTC	10 kΩ ±1% 1,600 x 800 μm	Discrete	1	B-Constant B <sub>25/50</sub> = 3380K B <sub>25/85</sub> = 3435K B <sub>25/100</sub> = 3455K
Capacitor (Snubber)	1,800 x 800 μm	Discrete	2	15 nF
Resistor (Snubber)	2,000 x 1,250 μm	Discrete	2	1 Ω

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## TYPICAL CHARACTERISTICS

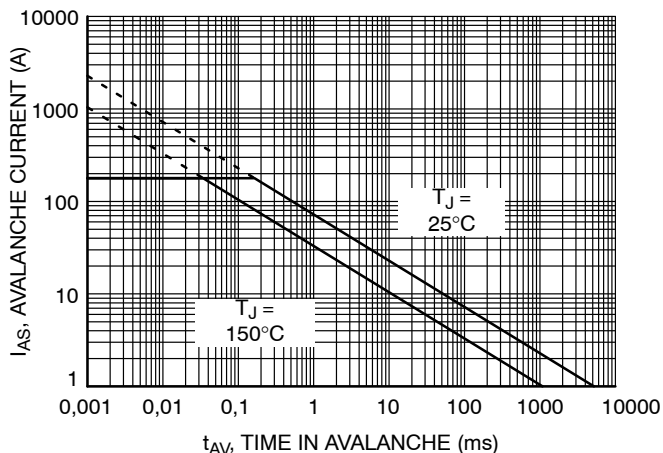


Figure 3. Unclamped Inductive Switching Capability

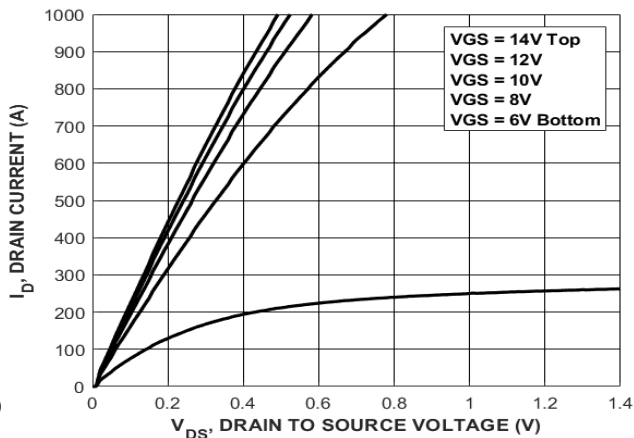


Figure 4. Saturation Characteristics

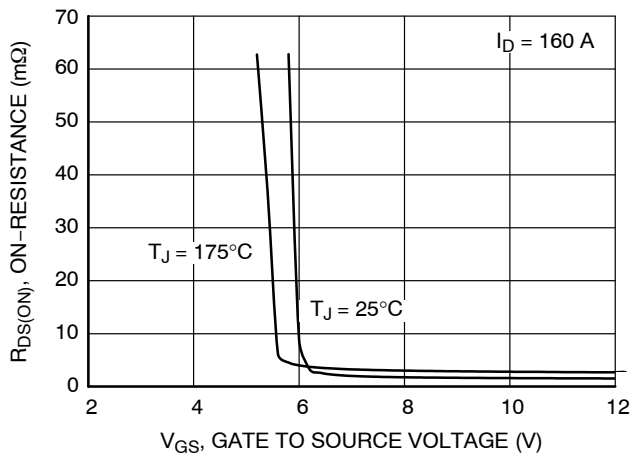


Figure 5.  $R_{DS(ON)}$  vs. Gate Voltage

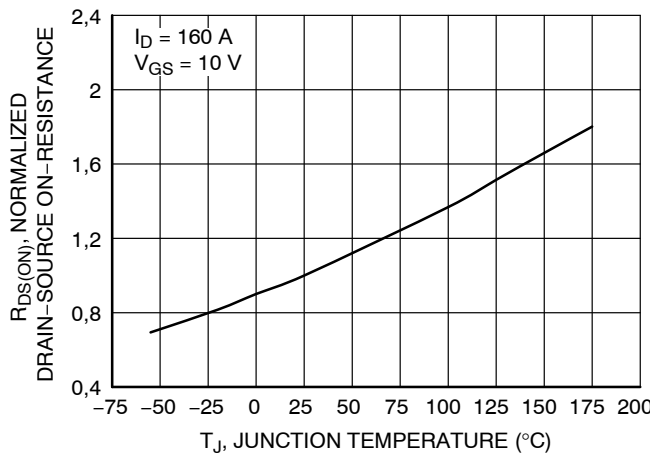


Figure 6.  $R_{DS(ON)}$  vs. Temperature

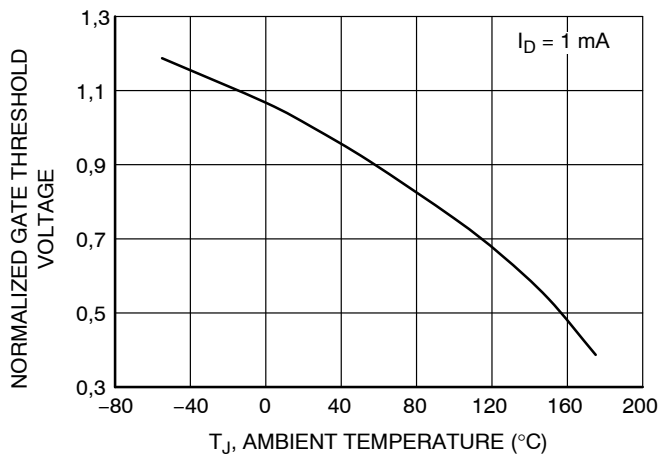


Figure 7. Normalized Gate Threshold Voltage vs. Temperature

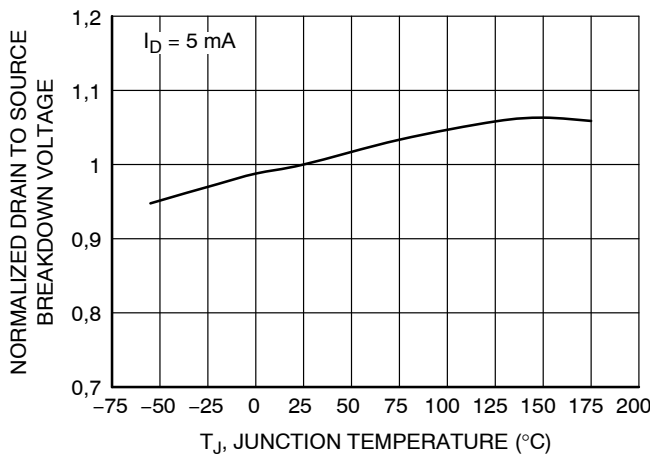


Figure 8. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

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## TYPICAL CHARACTERISTICS (CONTINUED)

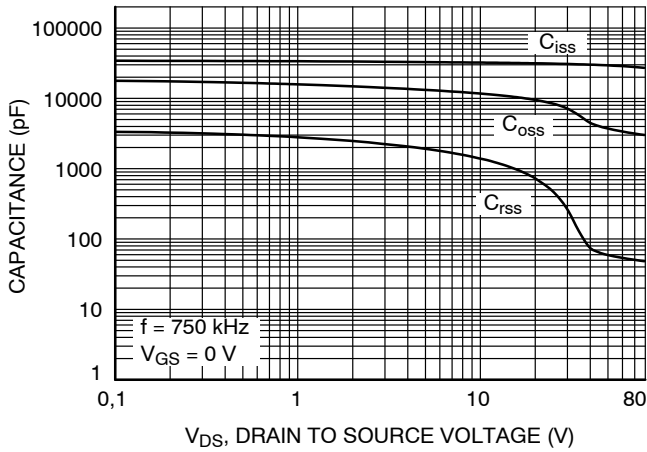


Figure 9. Capacitance vs. Drain to Source Voltage

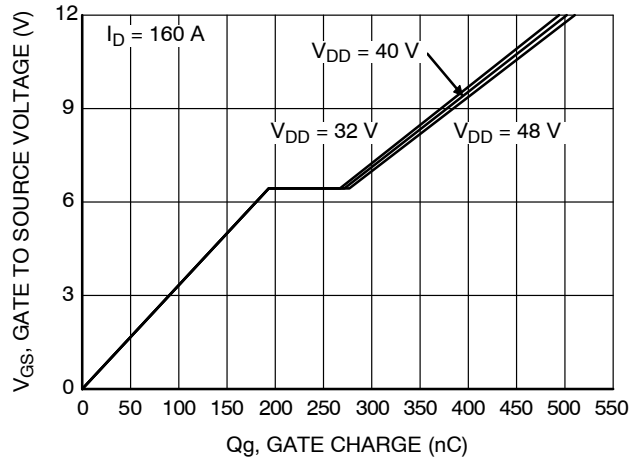


Figure 10. Gate Charge vs. Drain to Source Voltage

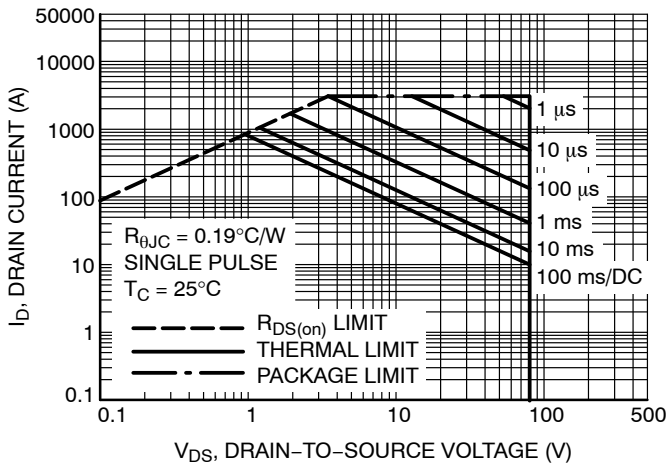


Figure 11. Safe Operating Area

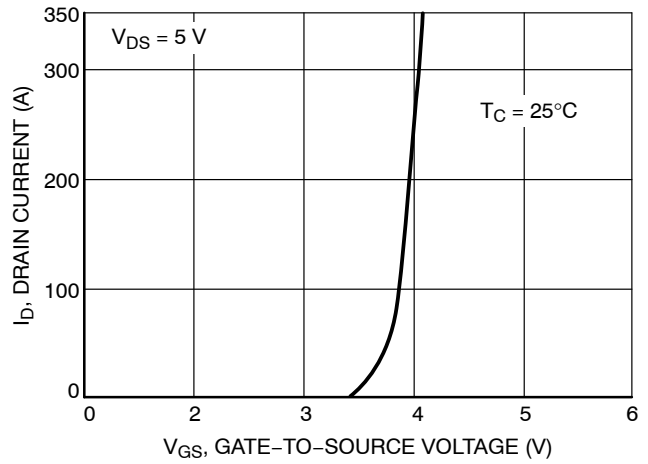


Figure 12. Transfer Characteristics

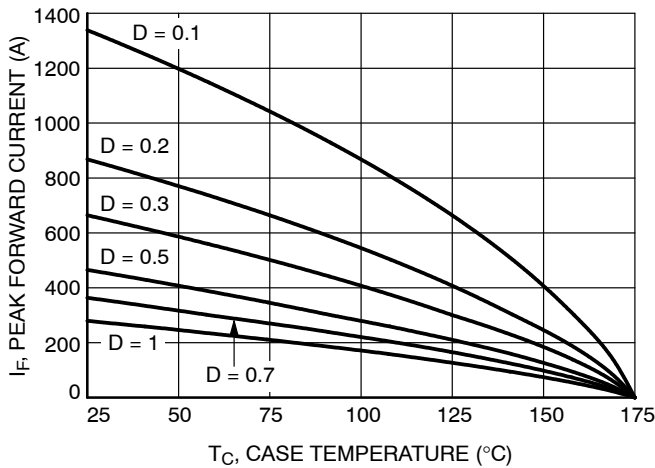
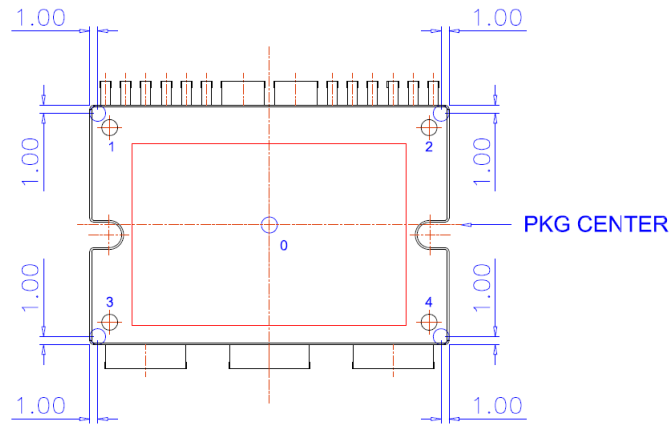


Figure 13. Body Diode Current

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20  
 FLATNESS : MAX. 150um  
 - MEASURING AT INDICATING POINTS  
 1, 2, 3, AND 4 (BASED ON "0")

**Figure 14. Flatness Measurement Position**

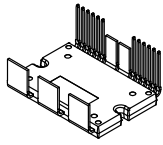
## MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Test Conditions	Min	Typ	Max	Units
Device Flatness	Refer to the package dimensions	0	-	150	um
Mounting Torque	Mounting screw: M3, recommended 0.7 N•m	0.4	-	1.4 (Note 5)	N•m
Weight		-	23.6	-	g

5. Max Torque rating can be different by the type of screw, such as the screw head diameter, use or without use of Washer. In case of special screw mounting method is applied, contact to **onsemi** for the proper information of mounding condition.

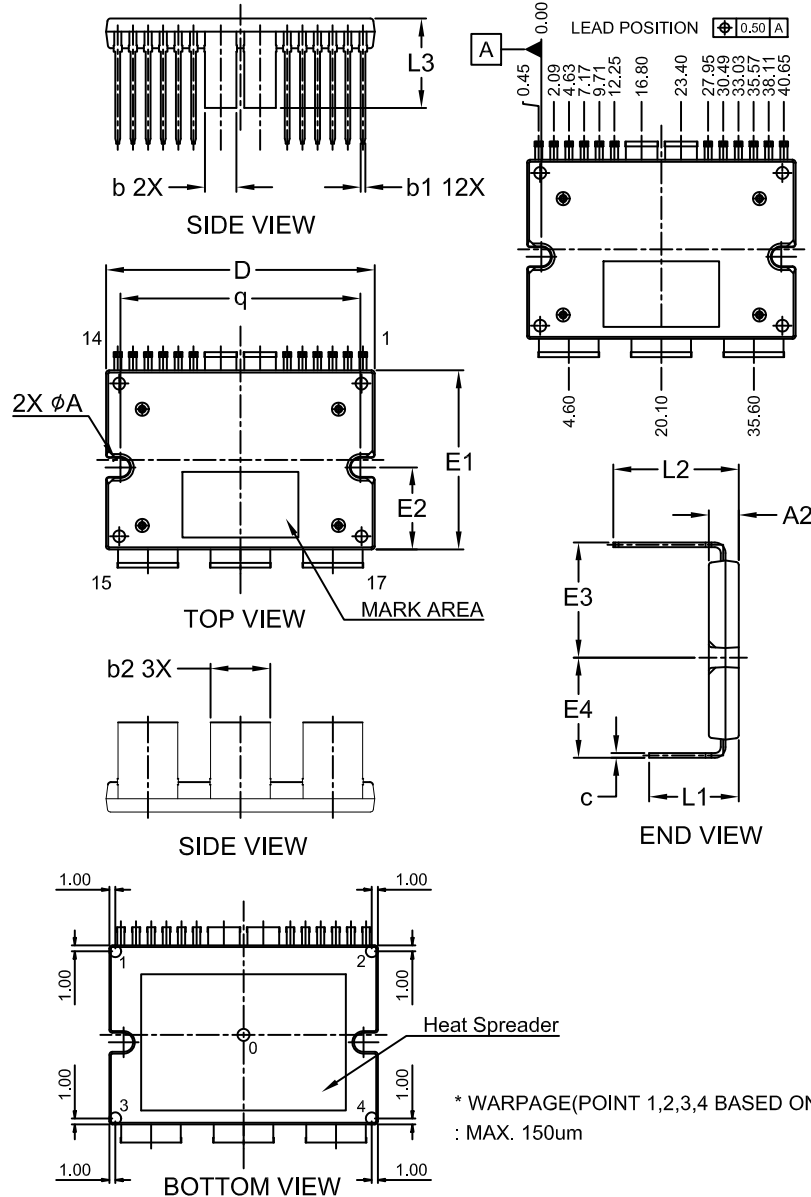


# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



## APM17-MDC CASE MODHH ISSUE C

DATE 08 DEC 2021

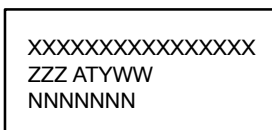


NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A2	4.90	5.00	5.10
b	5.20	5.30	5.40
b1	0.70	0.80	0.90
b2	9.90	10.00	10.10
c	0.75	0.80	0.90
D	44.90	45.00	45.10
E1	29.90	30.00	30.10
E2	13.65	13.75	13.85
E3	19.00	19.30	19.60
E4	16.50	16.80	17.10
L1	14.70	15.00	15.30
L2	20.70	21.00	21.30
L3	14.70	15.00	15.30
q	40.10	40.20	40.30
φA	3.10	3.20	3.30

### GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
 ZZZ = Lot ID  
 AT = Assembly & Test Location  
 Y = Year  
 W = Work Week  
 NNN = Serial Number

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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