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Self Restoring Logic (SRL) Cell Targets Space Application Designs

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Introduction

Circuit designs for space applications must address harsh radiation environments that impact Application Specific Integrated Circuit (ASIC) performance. Single high energy particles can disrupt integrated circuits if they strike sensitive circuit nodes. As feature sizes shrink and clock speeds increase, the impact becomes more significant.   Semiconductor manufacturers have a variety of techniques to reduce or eliminate Single Event Effects (SEE). Some solutions include process modifications that reduce (but cannot eliminate) SEE. Here we will review Radiation Hardened by Design (RHBD) methods to improve immunity to Single Event Upsets: Triple Modular Redundancy (TMR) and Self Restoring Logic (SRL). Both methods share similar traits to provide fault tolerance for Single Event Upsets (SEUs) in ASICs. However, this paper reveals that the SRL design goes well beyond TMR in terms of demonstrated tolerance to SEUs, system performance, transistor count, and power. In short, SRL is a step beyond TMR for RHBD designs that demand fault tolerance, performance, and low power.   Finally at the conclusion of this paper, it is shown that legacy SEU tolerant designs fail to provide SEU tolerance in circuits that operate at high speed; therefore if SEU tolerance is desired, there are only two options: TMR and SRL. SRL is shown to be superior herein.

Triple Modular Redundancy

Triple Modular Redundancy (TMR) is a fault tolerant mitigation technique used to eliminate single event effects in semiconductor devices. A typical TMR implementation for single fault tolerance is shown in Figure 1.
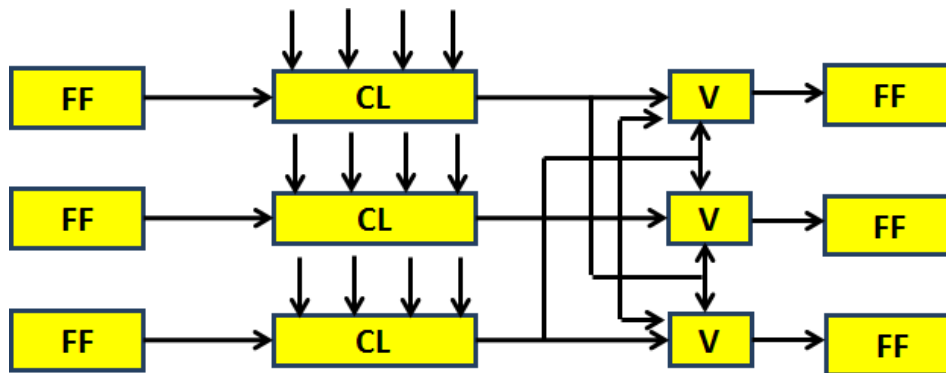

Figure 1: Traditional TMR

Here, CL represents arbitrary combinational logic that performs addition, multiplication and more. Three voters (V) are required to eliminate the possibility that a fault to any one voter would drive an incorrect result for the entire redundant system. Each voter presents a single fault tolerant output. This design requires six flip flops (FF) and three voters which results in a larger die size and increased power consumption. Voters added to the data path and the increased area needed to accommodate triplication often reduces system performance. An additional flaw with this design is the lack of self-recovery within the flip flops which may remain

in an incorrect state as a result of single event effects. Any erroneous data contained in the flip flop is stored until at least the next clock edge latches new data. This allows a fault to remain in the TMR system until synchronously over-written which can lead to TMR failure.

A second design implementation using the TMR methodology is shown in Figure 2. Here voters are placed in the feedback loop within the latch of the flip flop. Combinational logic is not shown for sake of simplicity.
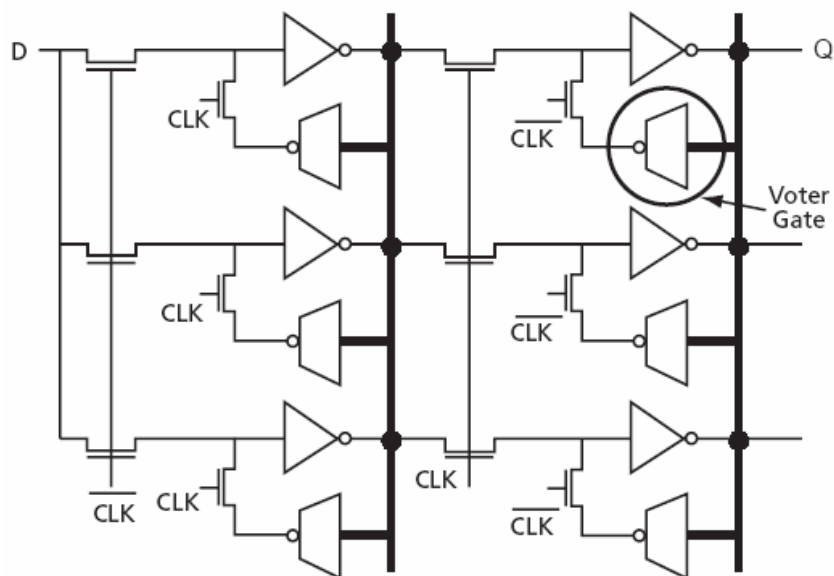

Figure 2: TMR with voters in feedback paths

This is similar to Microsemi's fault tolerant FPGA offerings. The design consists of six latches (3 master, 3 slave) with one voter per latch, three more voters than the solution in Figure 1. Here the voters perform the self-recovery function eliminating the erroneous data flaw described above. While this approach does address self recovery in one form, it is achieved through the addition of circuitry (voters) when compared to classical TMR.

Self-Restoring Logic Cell

The SRL cell was designed to exceed the SEU mitigation goals of the TMR circuit. An asynchronous sequential circuit was created at the transistor level resulting in a fault tolerant flip-flop with superior features including:

- Single fault tolerance
- Three redundant storage elements
- Error correction of stored information and input data
- Self-recovery of internal faults
- Means to prevent fault propagation
- Observable internal nodes such that masked manufacturing faults are avoided
- Minimal performance overhead
- Design tool implementation (ASIC flow)

A typical design using the SRL cell is shown in Figure 3. Transistor level implementation results in a highly integrated cell. The feature set including error correction, data storage, and asynchronous self-recovery cannot be segregated into separate, discrete blocks. This results in a highly efficient solution when compared to traditional or even non-radiation hardened cell designs. Last, the SRL cell is enabled within the ON Semiconductor ASIC design tools providing circuit designers a quick and easy design solution.
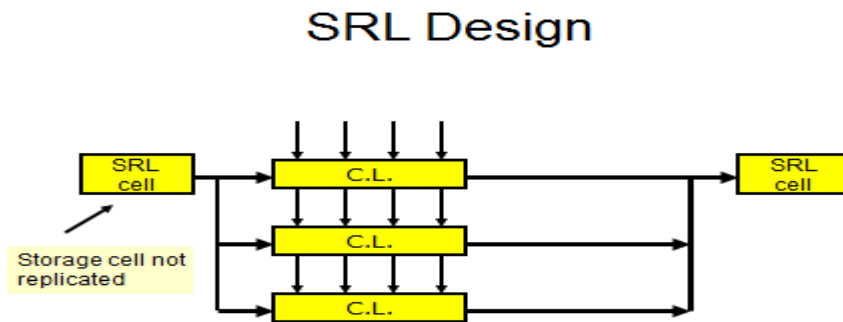

Figure 3: SRL Design Implementation

Design Implementation Comparison (SRL vs. TMR)

Performing a transistor count comparison between two designs can be complex due to the numerous implementations that exist for latches and flip-flops. Here we assume that the TMR designs in figures 1 and 2 are pre-defined modules versus the SRL transistor level solution. As a result, the SRL realizes transistor-usage efficiencies up to 100% over TMR (See Table 1). Fewer transistors generally result in less power consumption, less silicon area and faster circuits.

Design	Number Transistors	% increase over SRL
SRL Figure 3	60	-
TMR Figure 1	108	80%
TMR Figure 2	120	100%

Table 1: Transistor Difference

Radiation Test Comparison (SRL vs. DICE)

The SRL cell is a breakthrough design technology to mitigate SEU at high speed operation. The superiority of SRL was demonstrated using an ON Semiconductor 110nm test chip that included the SRL cell and legacy Dual Interlocked Cell (DICE). Radiation evaluation included Heavy Ion testing at Texas A&M University Cyclotron Institute, Total Ionizing Dose (TID) and Dose Rate testing at Boeing's Radiation Effects Laboratory and Neutron Testing at White-Sands Missile Range Fast-burst Reactor facility. While the focus of this testing is on the 110nm process, the SRL cell can be scaled to smaller technology nodes.

Figure 4 shows the SEU susceptibility of the DICE flip-flop design. Where it barely met the NASA SEU criteria at 25 MHz, the legacy design fails at low LET points when clocked at or above 125 MHz. DICE flip-flops are also very susceptible to shallow angle SEU.
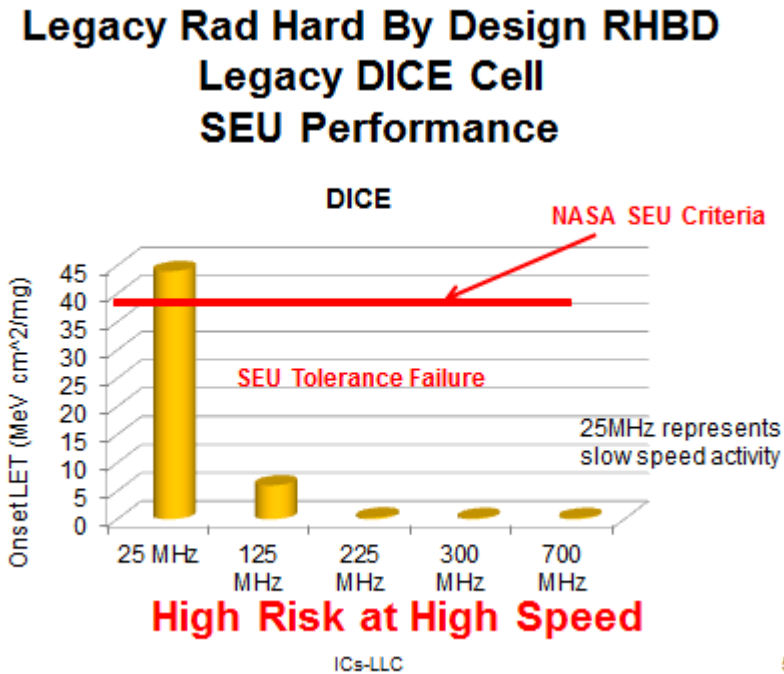
Figure 4: DICE Performance at Various Clock Speeds

The SRL cell exhibited zero upsets up to and including an LET of 106 MeV cm^2/mg through 700 MHz testing (See Figure 5). In addition, the SRL showed no upsets under shallow angle radiation.
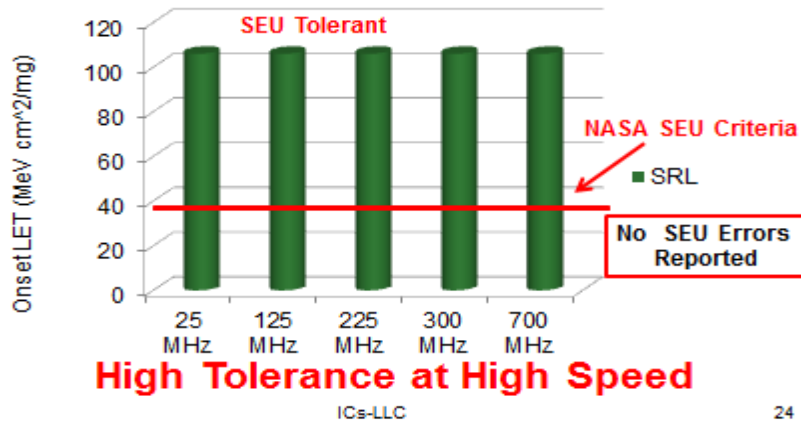
Figure 5: SRL SEU Tolerance

Conclusion

The SRL cell is a novel flip-flop architecture that provides superior SEU protection and better system performance while minimizing silicon area. A fault tolerant flip-flop fully integrated at the transistor level, SRL can protect against solid and transient faults equally. Internal fault detection can isolate manufacturing defects as well as hard and soft faults that occur during device operation. Currently implemented using ON Semiconductor's 110nm process node, the SRL cell is fully enabled within the design tool suite and can be scaled to sub-100nm technologies. Ideal for space electronics, other applications include autonomous vehicles, aerospace electronics and hardware security where errors may be induced into the system to compromise the application's integrity.

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