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# TND301

# Clock Management Design Using Low Skew and Low Jitter Devices

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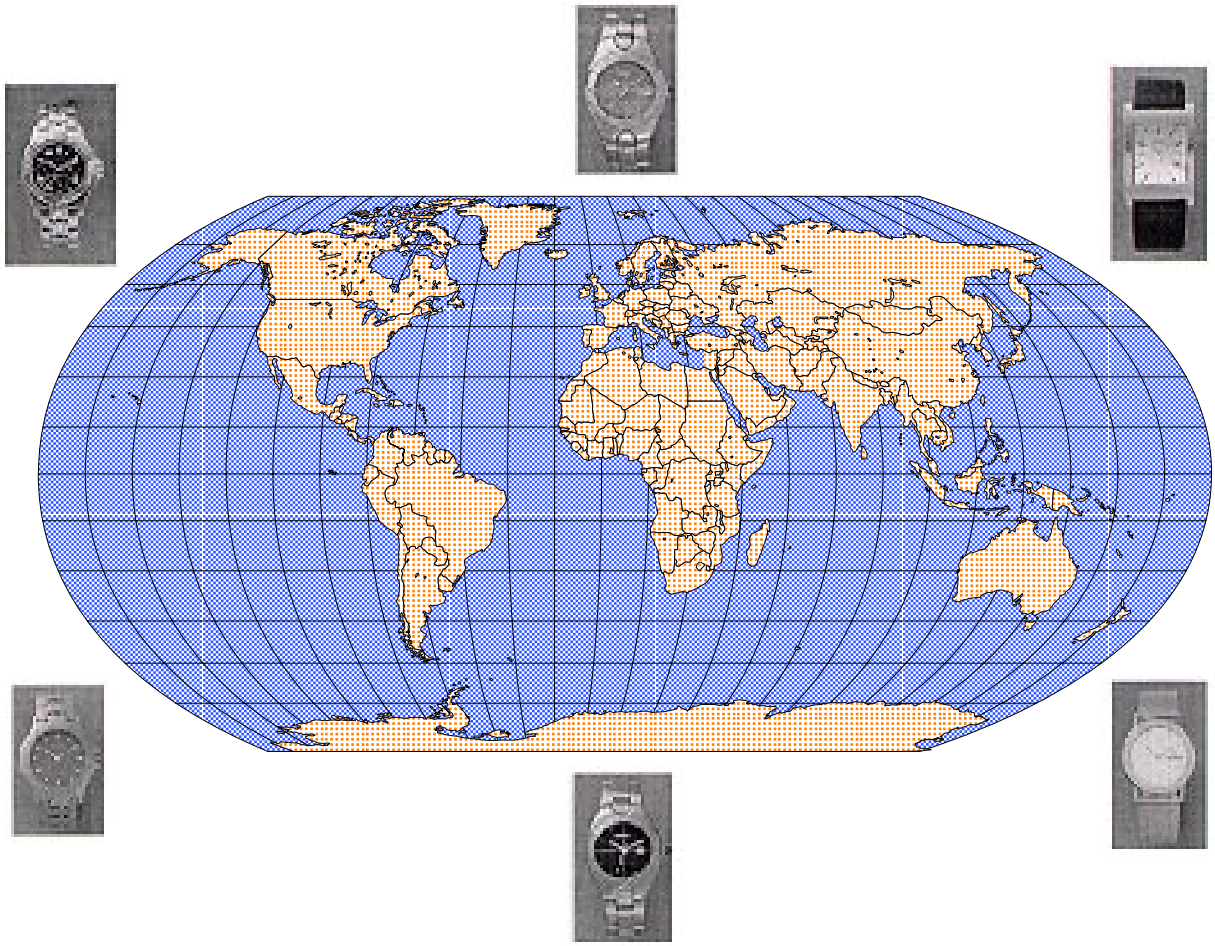
**TECHNICAL NOTE**

### Why Do We Need Clock Management?

Can you imagine the chaos in our world if our clocks or watches were not synchronized to Greenwich Mean Time? How would trains, buses, and airplanes run on schedule? The miniseries *Longitude* was the story of a man who made a major technological breakthrough by inventing an accurate clock that could be carried on sailing ships so navigators could accurately calculate longitude and know where the ship was located at any moment in time. Before this, ships ran aground and many people lost their lives due to navigational errors. Even though there are fixed time zone differences throughout the world, all clocks must agree within fractions of seconds for civilization to work orderly and without confusion. Clock accuracy is one of the most important scientific technologies in our world today.



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June, 2001 – Rev. 0
Publication Order Number:
TND301/D

## Typical Clock Management System

Clock Management of an electronic system (see Figure 1) depends on very accurate time keeping. A well–designed Clock Management scheme begins with a precise Clock Generator which is the standard Master Clock or Mean Time. The Master Clock is passed on to the Clock Distribution circuit which “fans out” multiple clocks throughout the system and activates individual events in the CPUs, ASICs, FPGAs, and Memory. All events are synchronized to the Master Clock and requires accurate devices to generate and distribute the clocks.

Accurate devices are described as those with low jitter and low skew. Jitter is uncertainty in the location of the rising or falling edge of the signal (see Figure 2). Jitter can be random or deterministic. Jitter is called phase noise in the Master Clock and increases as it passes through each device. Noise from power supplies and crosstalk between signals also add to the total jitter. Jitter can be measured as peak–to–peak or RMS in picoseconds.

Skew is a time offset of the clocks as they travel throughout the system (see Figure 3). Skew is defined as duty–cycle skew, within–device skew, or device–to–device skew. Skew is reduced by adjusting the delay of signals within the system. It is similar to propagation delay and is measured in picoseconds.

Large values of jitter and skew on clocks reduce the maximum operating frequency of a system.

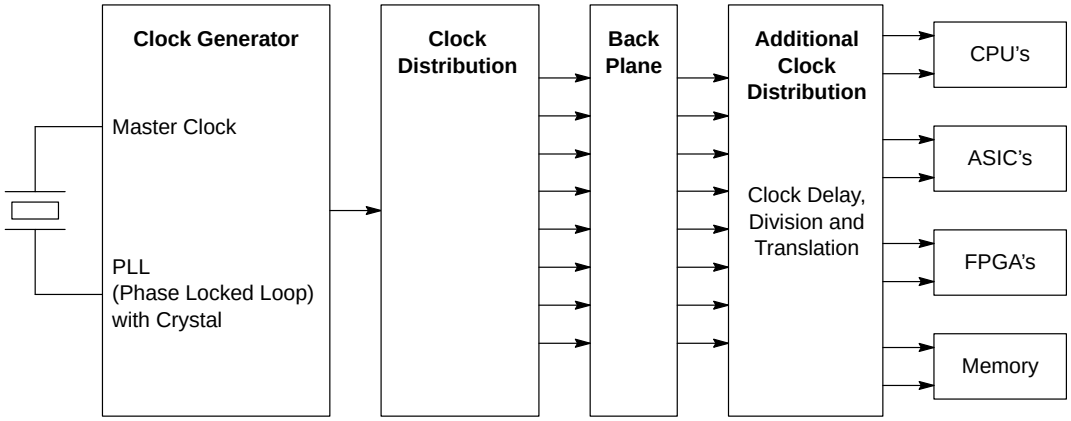
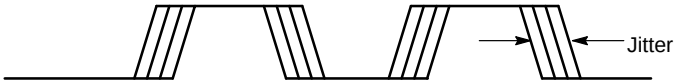
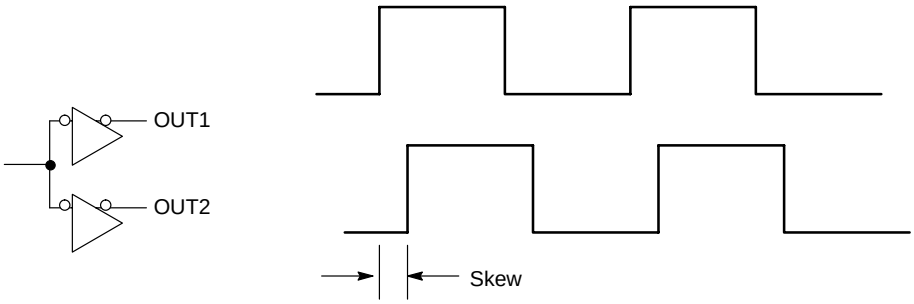



**Figure 1. Typical Clock Management System**




Jitter is the uncertainty caused by many factors including power supply noise, signal crosstalk, and device physics.

**Figure 2. Jitter**




Skew is a fixed difference between outputs caused by many factors including physical layout, device process variations, and unbalanced loading conditions.

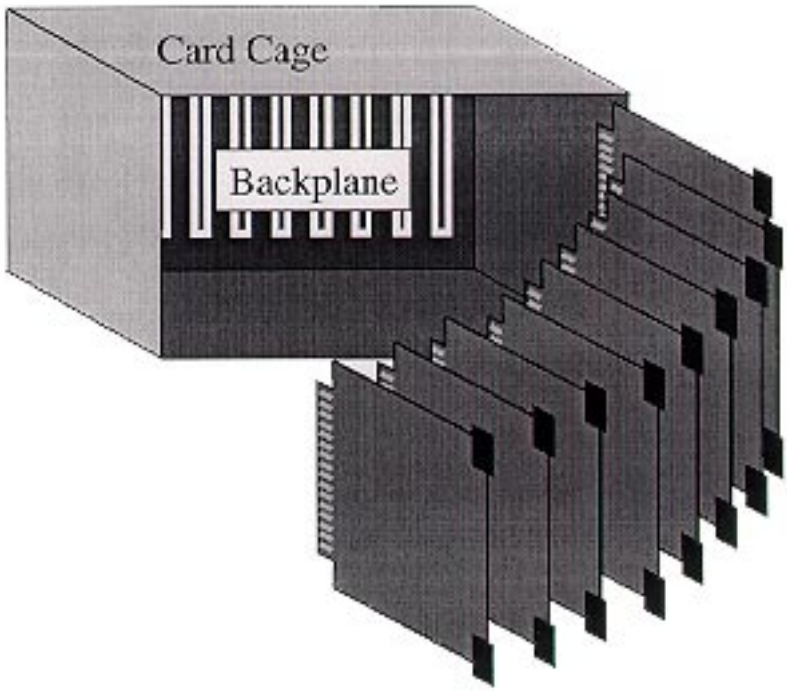
**Figure 3. Skew**

### Clock Management Highways

Clock Management is included in electronic systems that contain backplanes (see Figure 4). Backplanes are the physical highways for clocks. They are multilayer printed circuit boards that are on the back of a card cage and have connectors that each circuit card plugs into. The design of the backplane is very critical to the performance of the Clock Management system. Many factors must be considered for a good backplane design.

The Clock Generator is typically on a circuit card with Clock Distribution circuits. The clocks are distributed throughout the cards on the backplane and each card may then redistribute, delay, divide, and translate these clock signals.

Backplanes are noisy due to the high amount of electronic signal traffic. Standard connectors are also a problem on a backplane since they do not offer a good transition due to impedance mismatch. Most connectors do not offer differential signal capability and do not provide adequate ground pins for elimination of crosstalk. Backplanes tend to slow down signals because they have multiple layers which add capacitance and delay.




Clock Management systems distribute clocks over backplanes in super–and mini–computers, communication equipment like PABX, SONET/SDH systems, ATM, and advance test equipment.

**Figure 4. Example of Backplanes**

## The Building Blocks

### Clock Generator

The Clock Generator uses a Phase Locked Loop (PLL) circuit to generate the Master Clock (see Figure 5). A Crystal Oscillator Circuit generates a low phase noise signal that is received by a phase detector. The phase detector compares the phase of the crystal oscillator with the output of the Divide by N counter. If both phases are the same, the circuit is in LOCK and a small output pulse from the phase detector is averaged by the Loop Filter. The Loop Filter outputs a voltage to the VCO which defines the Master Clock frequency. The Divide by N counter can be programmed to increase or decrease the Master Clock frequency. The Master Clock is equal to the Crystal Oscillator frequency times the value N. This is why a PLL is sometimes called a frequency multiplier. The PLL is a feedback circuit; if the Master Clock begins to drift away, the shift in phase will be discovered by the Phase Detector The Phase Detector will then generate a wider output pulse which will be averaged by the Loop Filter and this new value will push the VCO back in the right direction.

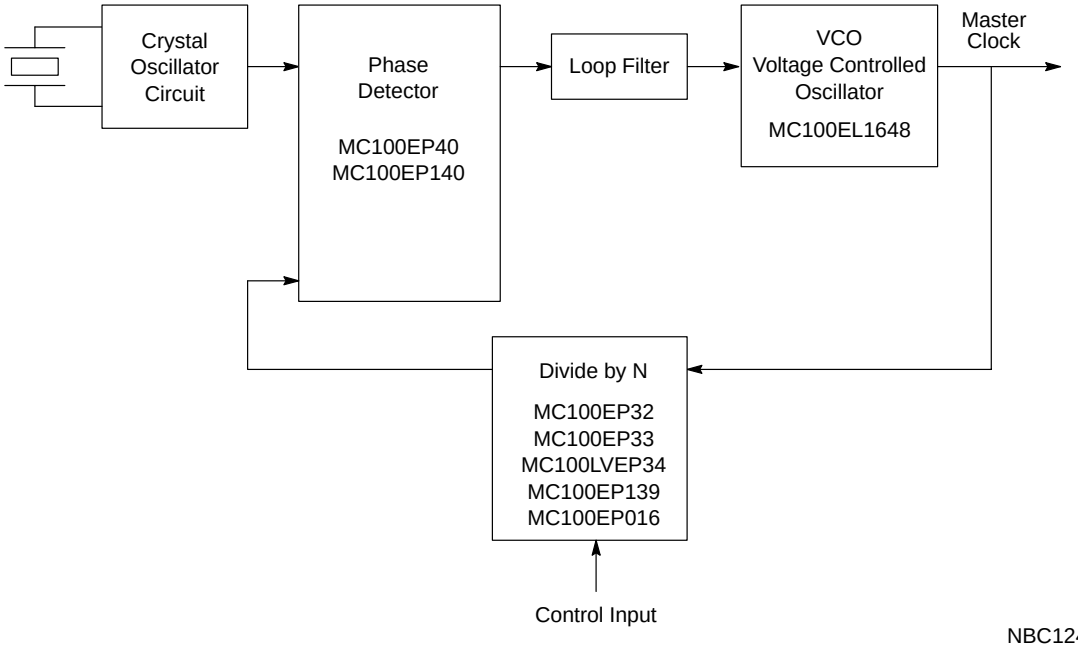



**Figure 5. Clock Generation Using Phase Locked Loop Circuit**

### Clock Distribution

Clock Distribution circuits receive a single differential input and “fan out” multiple outputs with minimum skew (see Figure 6).

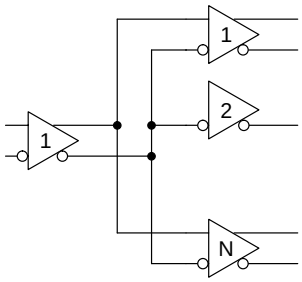



**Figure 6. Clock Distribution Using 1:N Clock Driver Circuit**

| 1:2 | Dual 1:3 | 1:4 | 1:5 | Dual 1:5 | 1:6 | 1:10 | 1:15 |
|---|---|---|---|---|---|---|---|
| MC100EL11 | MC100EL13 | MC100EL15 | MC100EL14 | MC100LVEP210 | MC100E211 | MC100LVEP111 | MC100LVE222 |
| MC100LVEL11 | MC100LVEL13 | | MC100LVEL14 | | | | |
| MC100EP11 | | | MC100EP14 | | | | |
| MC100LVEP11 | | | MC100LVEP14 | | | | |

**Delay Lines**

Delay Lines are used to synchronize clocks that travel different distances within the Clock Management system (see Figure 7). It is difficult in the card cage with a backplane to distribute all clocks to all circuits using the same length line. The position of the cards in the card cage makes this impossible. One way to synchronize the clocks in a large system is to use delay line circuits. The signal comes into the device and is delayed by an amount determined by a programmable input. This programmable input can be a parallel word and/or a single analog voltage input.

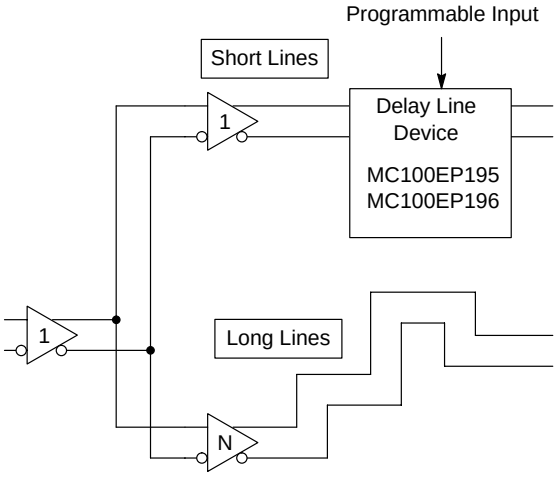



**Figure 7. Example of Clock Delay**

**Clock Dividers**

Clock Dividers are required to reduce the frequency of certain clocks within a system.

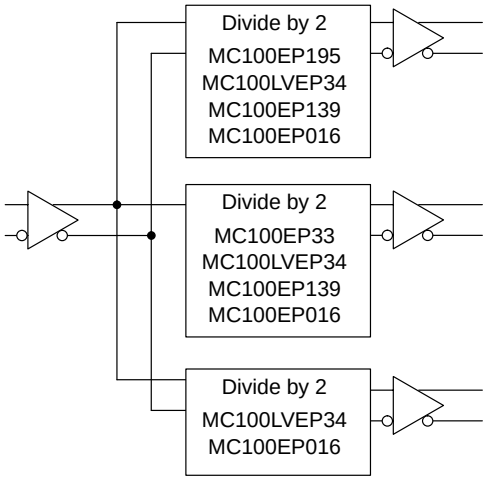



**Figure 8. Example of Clock Division**

### Translators

Translators are required in Clock Management systems to convert voltage levels and amplitudes to other voltage levels and amplitudes to interface with other logic components. These could be microprocessors, FPGAs, ASICs, or Memory all of which could have ECL, CMOS, TTL, LVDS, GTL, or HSTL inputs and outputs.

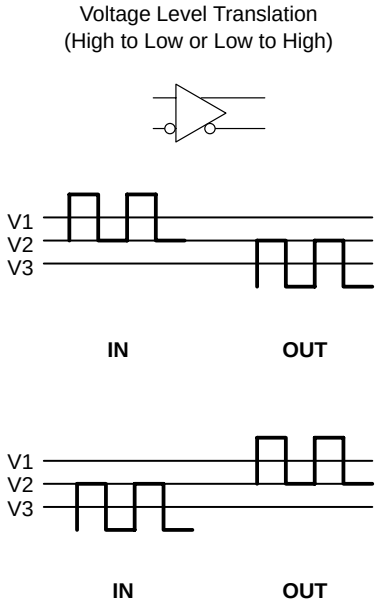



**Figure 9. Voltage Level Translation**

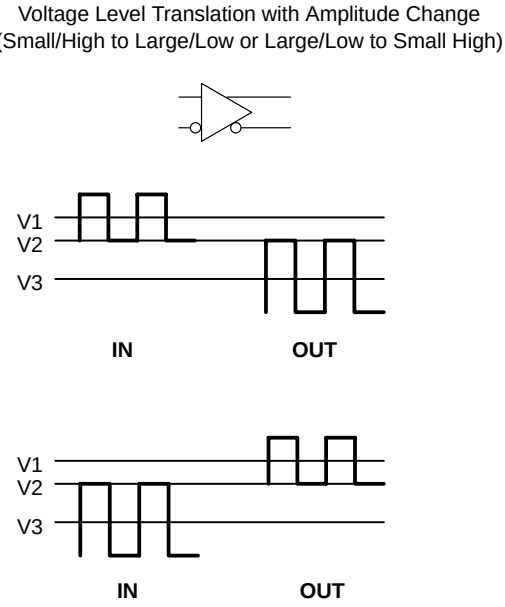



**Figure 10. Voltage Level and Amplitude Translation**

**TRANSLATOR TABLE**

| | PECL/LVPECL | TTL/CMOS | LVDS | NECL |
|---|---|---|---|---|
| **PECL/LVPECL** | MC100EP16<br>MC100LVEP16<br>MC100LVEL92 | MC100EPT21<br>MC100EPT23<br>MC100EPT26 | MC100EP210S | MC100LVEL91 |
| **TTL/CMOS** | MC100EPT20<br>MC100EPT22 | | | MC100EPT24 |
| **LVDS** | MC100LVEP16<br>MC100LVEP17 | | | |
| **NECL** | MC100EP90 | MC100EPT25 | | |

NOTE: For more information, see application note AN1672.

### The Challenges: We Have a Better Solution

Clock Management systems require the clocks to have low jitter and low skew. ECL logic provides less jitter and skew with a higher operating frequency than other technologies. ECL logic technology offers a number of advantages over CMOS, LVDS, and TTL in reducing clock errors caused by jitter and skew. ECL devices have 1 ps jitter and 25 ps skew compared to 15 ps jitter and 100 ps skew for LVDS and CMOS devices. (See Figure 11 and Figure 12). The frequency of ECL logic is 3 Ghz maximum frequency compared to 300 Mhz maximum frequency for LVDS and CMOS logic (see Figure 13). The rise and fall times of clock signals is very critical for edge placement. ECL logic provides rise and fall times of 100 ps compared to rise and fall times of 800 ps for LVDS and CMOS logic (see Figure 14).

ECL logic technologies offer a number of advantages for reducing the noise due to crosstalk and signal mismatch on the backplane over CMOS, LVDS, and TTL technologies. ECL signals are differential signals and can be individually terminated to match the transmission impedance of the backplane ECL signals have adequate current (50 mA) to drive a backplane and can deliver signals with maximum frequencies of 3 Ghz. ECL peak–to–peak output signals of 800 mV provide a good signal–to–noise ratio and excellent EMI characteristics.

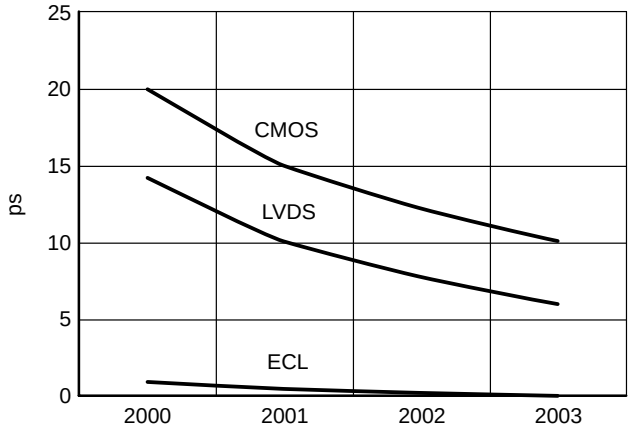



**Figure 11. Standard I/O rms Jitter**

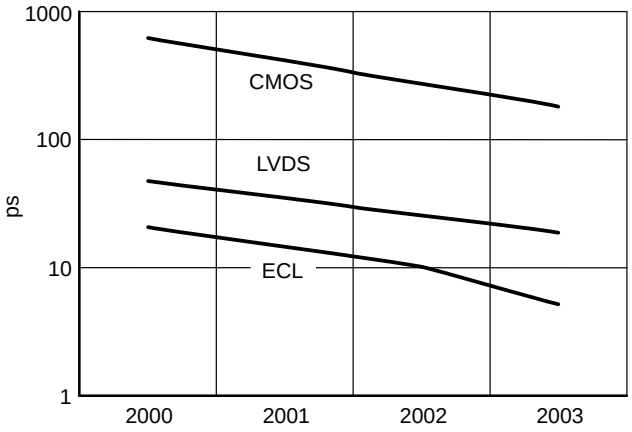



**Figure 12. Standard I/O Skew**

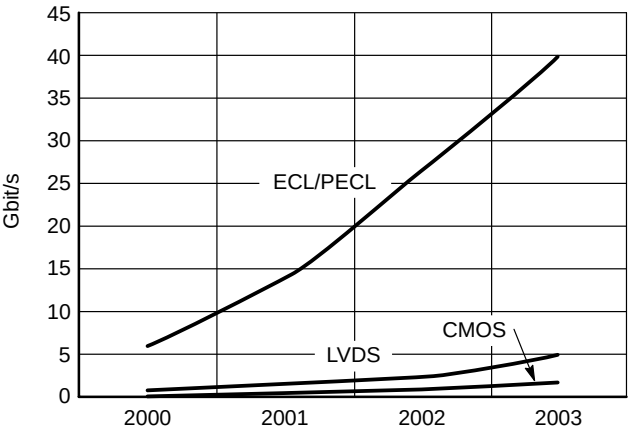



**Figure 13. Standard I/O Fmax**

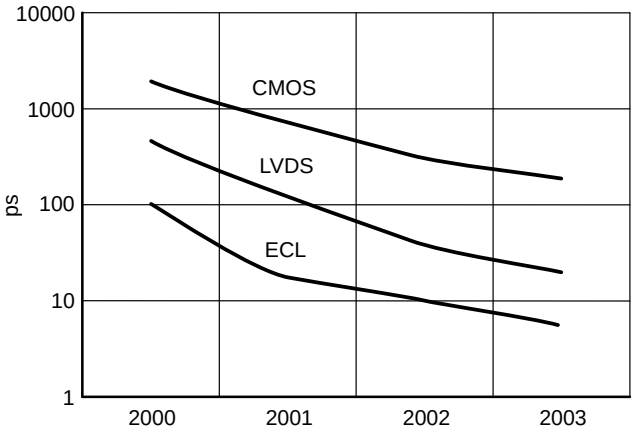



**Figure 14. Standard Rise/Fall Time Comparisons**

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