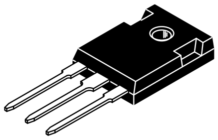
NPN High-Power Transistors

TIP33C

Designed for general−purpose power amplifier and switching applications.

Features

- ESD Ratings: Machine Model, C; > 400 V
  Human Body Model, 3B; > 8000 V
- Epoxy Meets UL 94 V−0 @ 0.125 in
- These Devices is Pb−Free*



TO−247
CASE 340L
STYLE 3

10 AMPERE
NPN SILICON
POWER TRANSISTORS
60 & 100 VOLT, 80 WATTS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector − Emitter Voltage	V_{CEO}	100	Vdc
Collector − Base Voltage	V_{CBO}	100	Vdc
Emitter − Base Voltage	V_{EBO}	5.0	Vdc
Collector Current − Continuous − Peak (Note 1)	I_C	10 15	Adc Apk
Base Current − Continuous	I_B	3.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.64	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

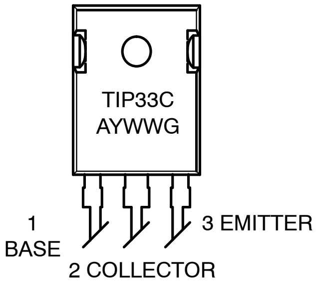
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.56	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	35.7	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

MARKING DIAGRAM



TIP33C = Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
TIP33CG	TO−247 (Pb−Free)	30 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 2) (I_C = 30 mA, I_B = 0)	$V_{CEO(sus)}$	100	– –	Vdc
Collector−Emitter Cutoff Current (V_{CE} = 30 V, I_B = 0) (V_{CE} = 60 V, I_B = 0)	I_{CEO}	–	0.7	mA
Collector−Emitter Cutoff Current (V_{CE} = Rated V_{CEO}, V_{EB} = 0)	I_{CES}	–	0.4	mA
Emitter−Base Cutoff Current (V_{EB} = 5.0 V, I_C = 0)	I_{EBO}	–	1.0	mA
ON CHARACTERISTICS (Note 2)				
DC Current Gain	h_{FE}			–
(I_C = 1.0 A, V_{CE} = 4.0 V)		40	–	
(I_C = 3.0 A, V_{CE} = 4.0 V)		20	100	
Collector−Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 3.0 A, I_B = 0.3 A)		–	1.0	
(I_C = 10 A, I_B = 2.5 A)		–	4.0	
Base−Emitter On Voltage	$V_{BE(on)}$			Vdc
(I_C = 3.0 A, V_{CE} = 4.0 V)		–	1.6	
(I_C = 10 A, V_{CE} = 4.0 V)		–	3.0	
DYNAMIC CHARACTERISTICS				
Small−Signal Current Gain (I_C = 0.5 A, V_{CE} = 10 V, f = 1.0 kHz)	h_{fe}	20	–	–
Current−Gain — Bandwidth Product (I_C = 0.5 A, V_{CE} = 10 V, f = 1.0 MHz)	f_T	3.0	–	MHz

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

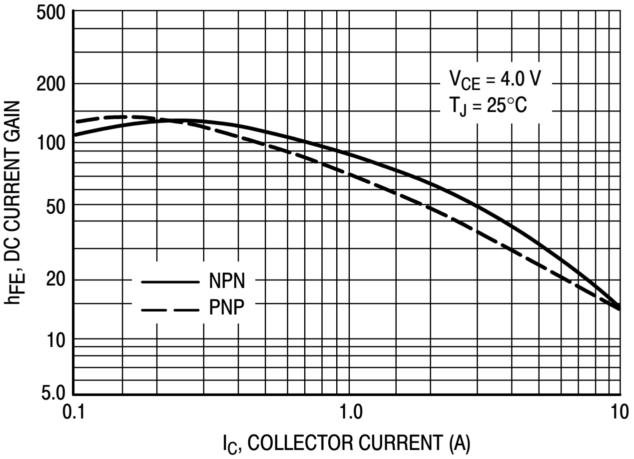


Figure 1. DC Current Gain

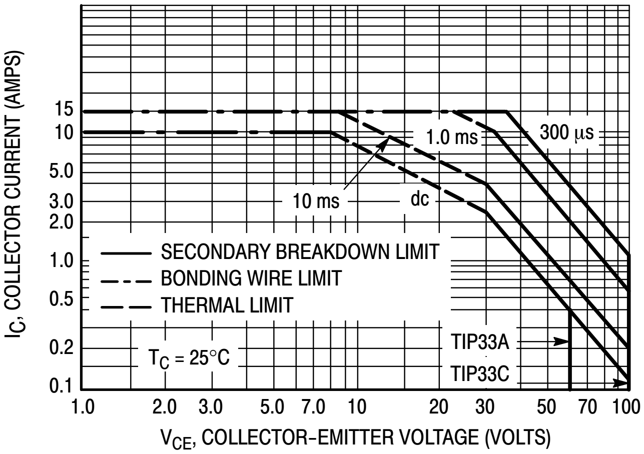


Figure 2. Maximum Rated Forward Bias Safe Operating Area

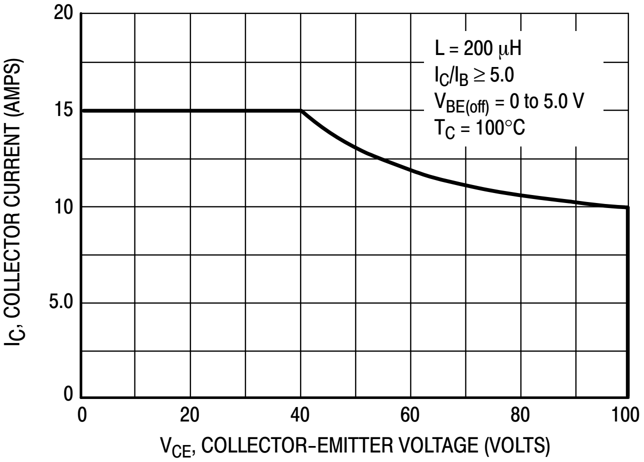


Figure 3. Maximum Rated Forward Bias Safe Operating Area

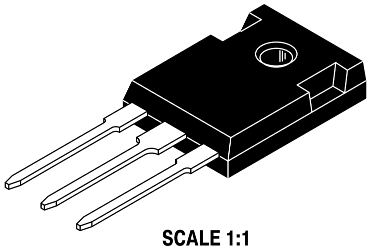
FORWARD BIAS

The Forward Bias Safe Operating Area represents the voltage and current conditions these devices can withstand during forward bias. The data is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10%, and must be derated thermally for $T_C > 25°C$.

REVERSE BIAS

The Reverse Bias Safe Operating Area represents the voltage and current conditions these devices can withstand during reverse biased turn−off. This rating is verified under clamped conditions so the device is never subjected to an avalanche mode.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

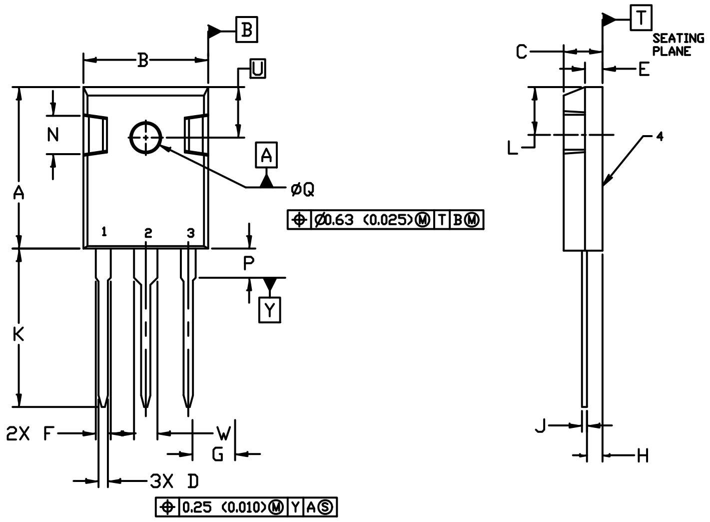


SCALE 1:1

TO−247
CASE 340L
ISSUE G

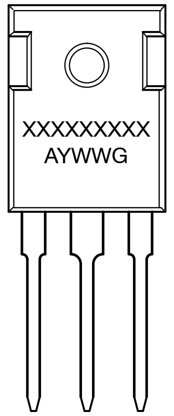
DATE 06 OCT 2021

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER



	MILLIMETERS		INCHES	
DIM	MIN.	MAX.	MIN.	MAX.
A	20.32	21.08	0.800	0.830
B	15.75	16.26	0.620	0.640
C	4.70	5.30	0.185	0.209
D	1.00	1.40	0.040	0.055
E	1.90	2.60	0.075	0.102
F	1.65	2.13	0.065	0.084
G	5.45 BSC		0.215 BSC	
H	1.50	2.49	0.059	0.098
J	0.40	0.80	0.016	0.031
K	19.81	20.83	0.780	0.820
L	5.40	6.20	0.212	0.244
N	4.32	5.49	0.170	0.216
P	----	4.50	----	0.177
Q	3.55	3.65	0.140	0.144
U	6.15 BSC		0.242 BSC	
W	2.87	3.12	0.113	0.123

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
- PIN 1. GATE
  - 2. DRAIN
  - 3. SOURCE
  - 4. DRAIN

STYLE 2:
- PIN 1. ANODE
  - 2. CATHODE (S)
  - 3. ANODE 2
  - 4. CATHODES (S)

STYLE 3:
- PIN 1. BASE
  - 2. COLLECTOR
  - 3. EMITTER
  - 4. COLLECTOR

STYLE 4:
- PIN 1. GATE
  - 2. COLLECTOR
  - 3. EMITTER
  - 4. COLLECTOR

STYLE 5:
- PIN 1. CATHODE
  - 2. ANODE
  - 3. GATE
  - 4. ANODE

STYLE 6:
- PIN 1. MAIN TERMINAL 1
  - 2. MAIN TERMINAL 2
  - 3. GATE
  - 4. MAIN TERMINAL 2

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DESCRIPTION:	**TO−247**	**PAGE 1 OF 1**

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