

MOSFET – Power, Single N-Channel

40 V, 1.4 mΩ, 200 A

NVMFS5C430NL

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS5C430NLWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	40	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	I_D 200	A
		$T_C = 100^\circ\text{C}$	140	
		$T_C = 25^\circ\text{C}$	P_D 110	W
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 100^\circ\text{C}$	53	
		$T_A = 25^\circ\text{C}$	I_D 38	A
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 100^\circ\text{C}$	27	
		$T_A = 25^\circ\text{C}$	P_D 3.8	W
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)	Steady State	$T_A = 100^\circ\text{C}$	1.9	
		$T_A = 25^\circ\text{C}$	I_{DM} 900	A
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	900	A	
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	120	A	
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 15 \text{ A}$)	E_{AS}	493	mJ	
Single Pulse Drain-to-Source Voltage ($t_p = 10 \mu\text{s}$)	V_{DSM}	48	V	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

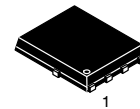
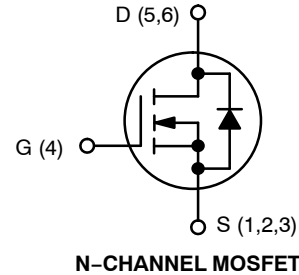
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	1.4	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	40	

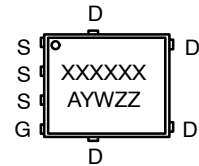
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
40 V	1.4 mΩ @ 10 V	200 A
	2.2 mΩ @ 4.5 V	



DFN5 (SO-8FL) CASE 488AA STYLE 1

MARKING DIAGRAM



XXXXXX = 5C430L (NVMFS5C430NL) or 430LWF (NVMFS5C430NLWF)
 A = Assembly Location
 Y = Year
 W = Work Week
 ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NVMFS5C430NL

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			1.3		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}$	$T_J = 25\ ^\circ\text{C}$		10	μA
			$T_J = 125^\circ\text{C}$		250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-5.6		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 50\text{ A}$		1.7	2.2	m Ω
		$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		1.2	1.4	
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 50\text{ A}$		180		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 20\text{ V}$		4300		pF
Output Capacitance	C_{OSS}			1900		
Reverse Transfer Capacitance	C_{RSS}			72		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 20\text{ V}; I_D = 50\text{ A}$		32		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 20\text{ V}; I_D = 50\text{ A}$		70		
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 20\text{ V}; I_D = 50\text{ A}$		7.0		
Gate-to-Source Charge	Q_{GS}			12		
Gate-to-Drain Charge	Q_{GD}			9.0		
Plateau Voltage	V_{GP}			2.9		V

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 20\text{ V}, I_D = 50\text{ A}, R_G = 1\ \Omega$		15		ns
Rise Time	t_r			140		
Turn-Off Delay Time	$t_{d(OFF)}$			31		
Fall Time	t_f			9		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 50\text{ A}$	$T_J = 25^\circ\text{C}$		0.81	1.2	V
			$T_J = 125^\circ\text{C}$		0.68		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s}, I_S = 50\text{ A}$		61		ns	
Charge Time	t_a			29			
Discharge Time	t_b			32			
Reverse Recovery Charge	Q_{RR}			80			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS



Figure 1. On-Region Characteristics



Figure 2. Transfer Characteristics



Figure 3. On-Resistance vs. Gate-to-Source Voltage



Figure 4. On-Resistance vs. Drain Current and Gate Voltage

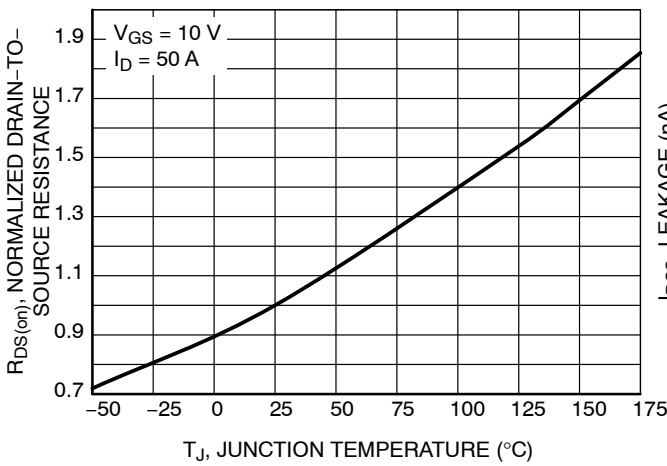


Figure 5. On-Resistance Variation with Temperature

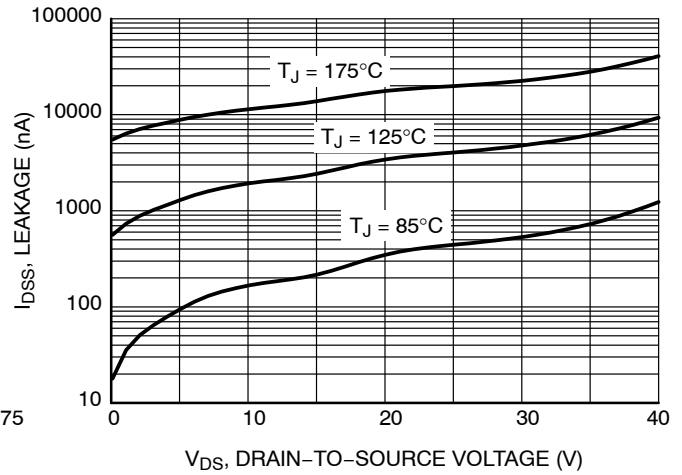


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NVMFS5C430NL

TYPICAL CHARACTERISTICS

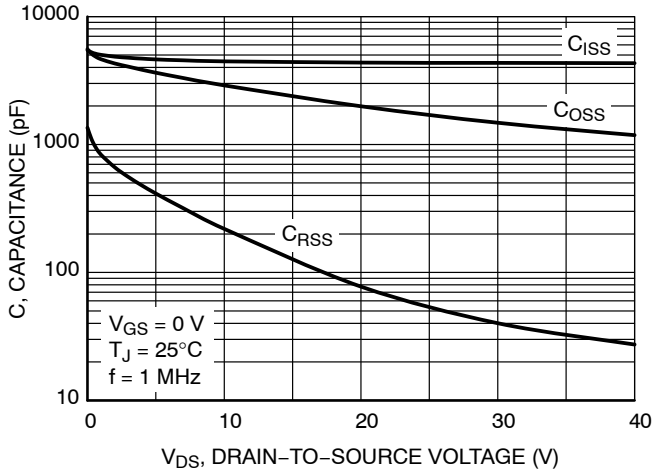


Figure 7. Capacitance Variation



Figure 8. Gate-to-Source Voltage vs. Total Charge

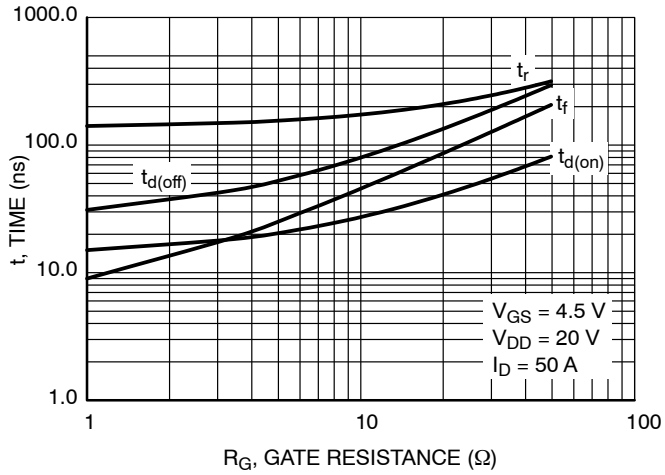


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

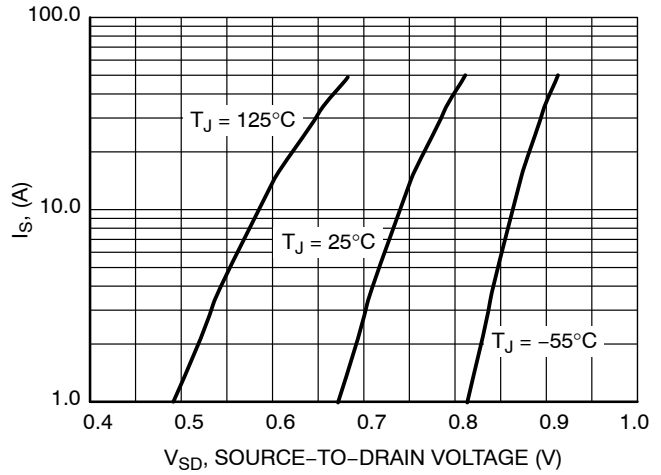


Figure 10. Diode Forward Voltage vs. Current

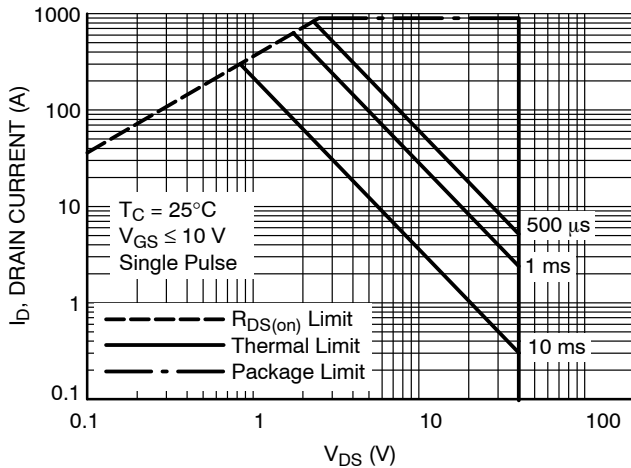


Figure 11. Safe Operating Area

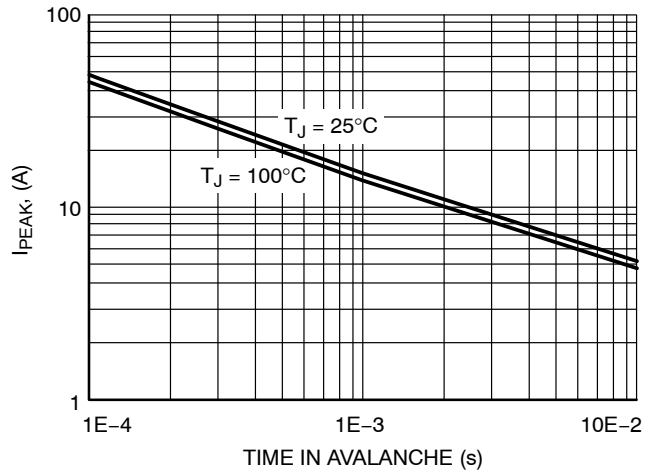


Figure 12. I_{PEAK} vs. Time in Avalanche

NVMFS5C430NL

TYPICAL CHARACTERISTICS

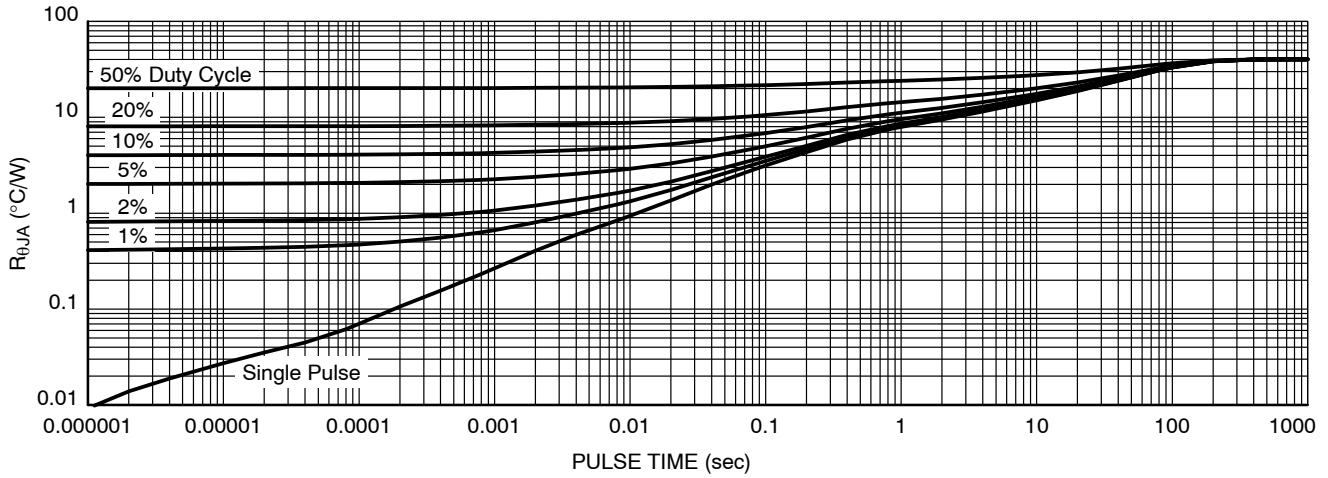


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMFS5C430NLT1G	5C430L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C430NLWFT1G	430LWF	DFN5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel
NVMFS5C430NLT3G	5C430L	DFN5 (Pb-Free)	5000 / Tape & Reel
NVMFS5C430NLWFT3G	430LWF	DFN5 (Pb-Free, Wettable Flanks)	5000 / Tape & Reel
NVMFS5C430NLAFT1G	5C430L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C430NLWFAFT1G	430LWF	DFN5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel
NVMFS5C430NLWFET1G	430LWF	DFN5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



1
SCALE 2:1

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



- STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
- STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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