

NUF2101M

USB Filter with ESD Protection

This device is designed for applications requiring **Line Termination**, **EMI Filtering** and **ESD Protection**. It is intended for use in downstream USB 1.1 ports, Cellular phones, Wireless equipment and computer applications. This device offers an integrated solution in a small package (TSOP-6, Case 318G) reducing PCB space and cost.

Features:

- Provides USB Line Termination, Filtering and ESD Protection
- Single IC Offers Cost Savings by Replacing 4 Resistors, 2 Capacitors, and 5 TVs diodes
- EMI Filtering Prevents Noise from Entering/Leaving the System
- IEC61000-4-2 (Level 4)
 - 8 kV (Contact)
 - 15 kV (Air)
- ESD Ratings: Machine Model = C
 - Human Body Model = 3B
- Pb-Free Package is Available

Benefits:

- TSOP-6 Package Minimizes PCB Space
- Integrated Circuit Increases System Reliability versus Discrete Component Implementation
- TVs Devices Provide ESD Protection That is Better than a Discrete Implementation because the Small IC minimizes Parasitic Inductances

Typical Applications:

- USB Hubs
- Computer Motherboards

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Symbol	Value	Unit
Steady State Power	P_D	225	mW
Maximum Junction Temperature	$T_{J(max)}$	125	$^\circ\text{C}$
Operating Temperature Range	T_J	-55 to +125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +125	$^\circ\text{C}$
Lead Solder Temperature (10 second duration)	T_L	260	$^\circ\text{C}$

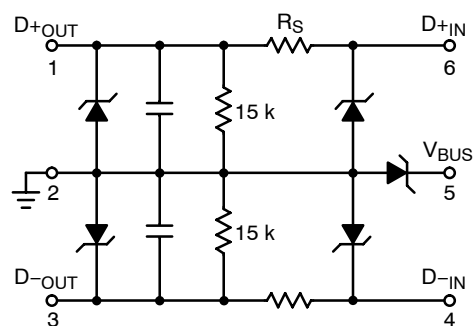
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.



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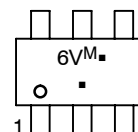
<http://onsemi.com>

SCHEMATIC



TSOP-6
CASE 318G
STYLE 10

MARKING DIAGRAM



6V = Specific Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NUF2101MT1	TSOP-6	3000/Tape & Reel
NUF2101MT1G	TSOP-6 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NUF2101M

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Device	Device Marking	V _{RWM} (Volts)	V _{BR} @ 1 mA (Volts)		Max I _R @ V _{RWM} = 5.25 V V _{BUS} to GND (μA)	Max I _R @ V _{RWM} = 3.3 V V _{BUS} Pin (μA)	Typical Line Capacitance (pF) (Notes 2, 3)	Series Resistor R _S (Ω) (Note 1)			Pulldown Resistor R _{pd} (kΩ)		
			Min	Max				Min	Nom	Max	Min	Nom	Max
NUF2101MT1	6V	5.25	6.0	8.0	1.0	0.1	55	26.3	30	33.7	13	15	17
NUF2101MT1G	6V	5.25	6.0	8.0	1.0	0.1	55	26.3	30	33.7	13	15	17

1. For other R_S values (i.e. R_S = 30 Ω) contact your local ON Semiconductor sales representative.
2. Measured at 25°C, V_R = 0 V, f = 1 MHz, Pins 2, 3, 4 or 5 to GND with Pin 1 also grounded.
3. For other capacitance values contact your local ON Semiconductor sales representative.

NUF2101M

TYPICAL CHARACTERISTICS

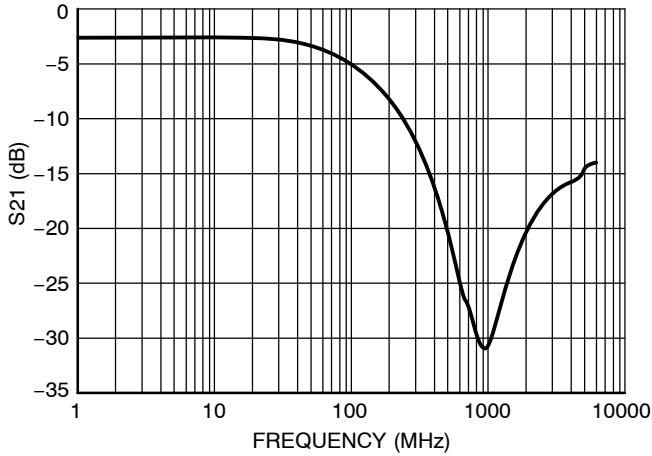


Figure 1. Insertion Loss Characteristics

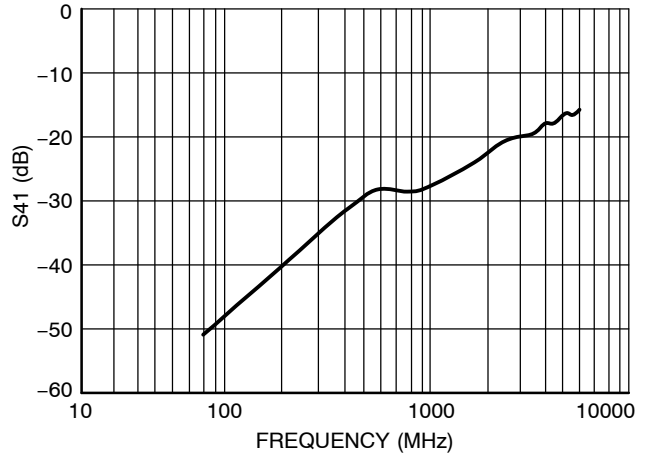


Figure 2. Analog Cross-Talk

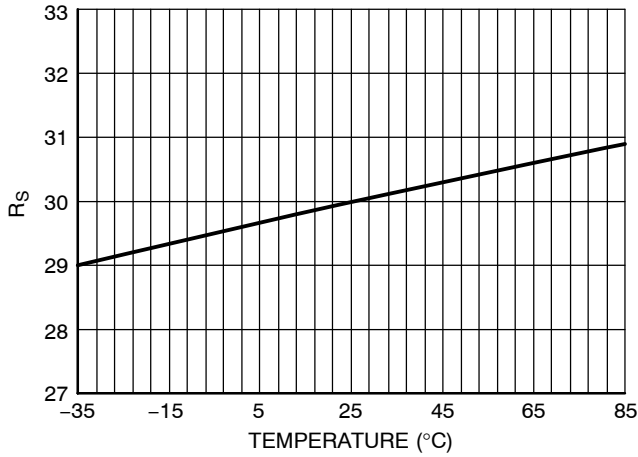


Figure 3. R_S vs. Temperature

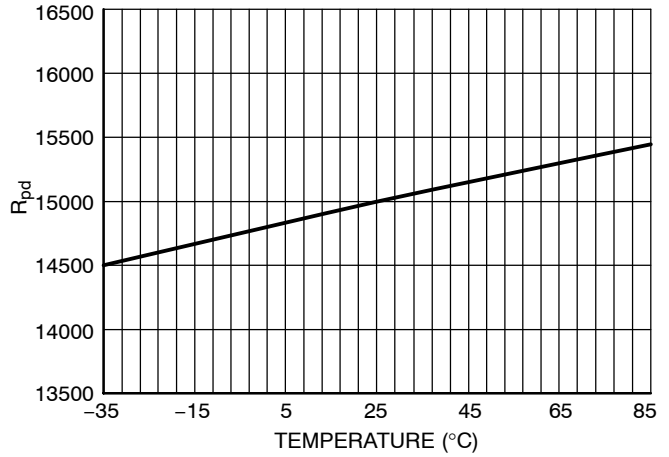


Figure 4. R_{pd} vs. Temperature

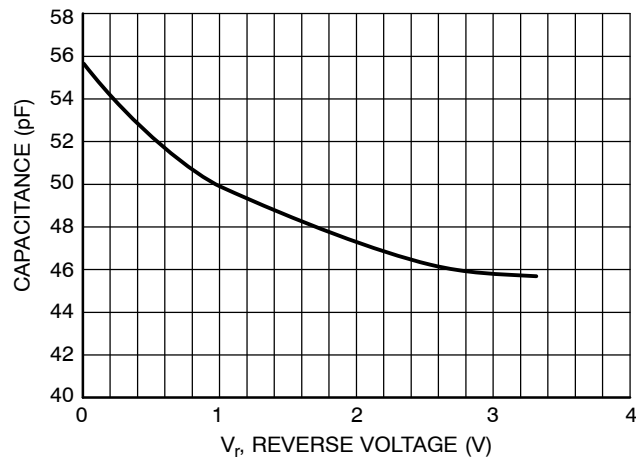
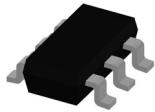


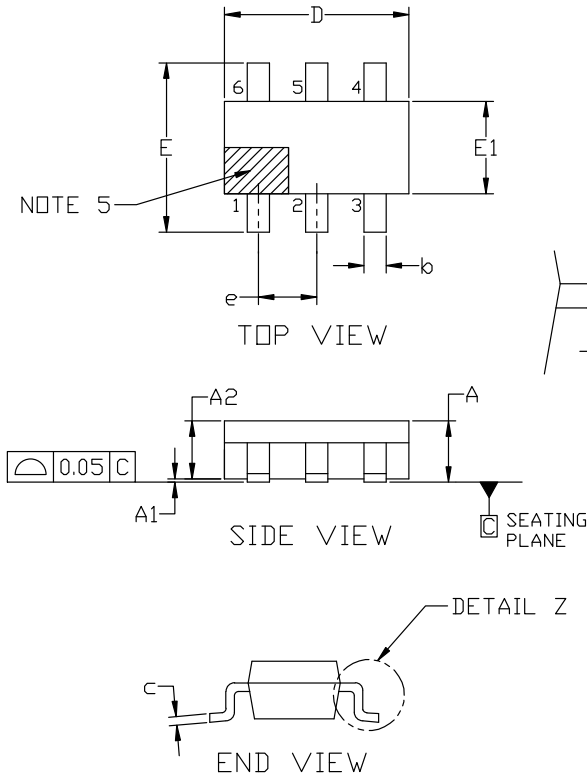
Figure 5. Typical Capacitance

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



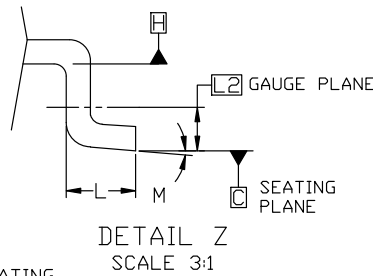
TSOP-6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

DATE 26 FEB 2024

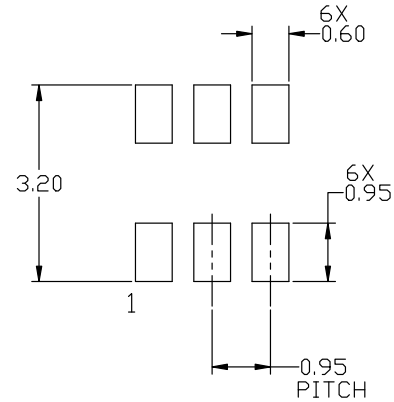


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE



MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

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DESCRIPTION:	TSOP-6 3.00x1.50x0.90, 0.95P	PAGE 1 OF 2

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MECHANICAL CASE OUTLINE

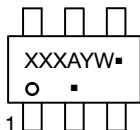
PACKAGE DIMENSIONS



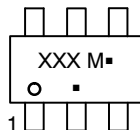
TSOP-6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

DATE 26 FEB 2024

GENERIC MARKING DIAGRAM*



IC



STANDARD

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

- | | | | | | |
|--|--|---|---|---|--|
| <p>STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN</p> | <p>STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2</p> | <p>STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out</p> | <p>STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD</p> | <p>STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2</p> | <p>STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR</p> |
| <p>STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER</p> | <p>STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND</p> | <p>STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE</p> | <p>STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)-
4. D(IN)-
5. VBUS
6. D(IN)+</p> | <p>STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2</p> | <p>STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O</p> |
| <p>STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1</p> | <p>STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN</p> | <p>STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE</p> | <p>STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE</p> | <p>STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR</p> | |

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