

NTTS2P03R2

Power MOSFET -2.48 Amps, -30 Volts P-Channel Enhancement Mode Single Micro8™ Package

Features

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Miniature Micro8 Surface Mount Package
- Diode Exhibits High Speed, Soft Recovery
- Micro8 Mounting Information Provided
- Pb-Free Package is Available

Applications

- Power Management in Portable and Battery-Powered Products, i.e.: Cellular and Cordless Telephones and PCMCIA Cards

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	-30	V
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	V
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	160	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	0.78	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	I_D	-2.48	A
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	I_D	-1.98	A
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	70	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.78	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	I_D	-3.75	A
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	I_D	-3.0	A
Thermal Resistance, Junction-to-Ambient (Note 3)	$R_{\theta JA}$	210	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	0.60	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	I_D	-2.10	A
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	I_D	-1.67	A
Pulsed Drain Current (Note 5)	I_{DM}	-17	A
Thermal Resistance, Junction-to-Ambient (Note 4)	$R_{\theta JA}$	100	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.25	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	I_D	-3.02	A
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	I_D	-2.42	A
Pulsed Drain Current (Note 5)	I_{DM}	-24	A
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Minimum FR-4 or G-10 PCB, Time ≤ 10 Seconds.
2. Mounted onto a 2" square FR-4 Board (1" sq. 2 oz Cu 0.06" thick single sided), Time ≤ 10 Seconds.
3. Minimum FR-4 or G-10 PCB, Steady State.
4. Mounted onto a 2" square FR-4 Board (1" sq. 2 oz Cu 0.06" thick single sided), Steady State.
5. Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.

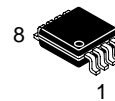
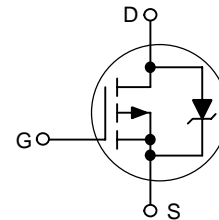


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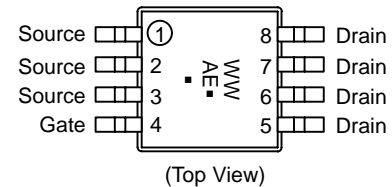
-2.48 AMPERES
-30 VOLTS
85 m Ω @ $V_{GS} = -10$ V

Single P-Channel



Micro8
CASE 846A
STYLE 1

MARKING DIAGRAM & PIN ASSIGNMENT



WW = Work Week
AE = Device Code
■ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTTS2P03R2	Micro8	4000/Tape & Reel
NTTS2P03R2G	Micro8 (Pb-Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Rating	Symbol	Value	Unit
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = -30\text{ Vdc}$, $V_{GS} = -10\text{ Vdc}$, Peak $I_L = -3.0\text{ Apk}$, $L = 65\text{ mH}$, $R_G = 25\ \Omega$)	E_{AS}	292.5	mJ
Maximum Lead Temperature for Soldering Purposes for 10 seconds	T_L	260	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted) (Note 6)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = -250\ \mu\text{Adc}$) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	-30 -	- -30	- -	Vdc mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current ($V_{GS} = 0\text{ Vdc}$, $V_{DS} = -30\text{ Vdc}$, $T_J = 25^\circ\text{C}$) ($V_{GS} = 0\text{ Vdc}$, $V_{DS} = -30\text{ Vdc}$, $T_J = 125^\circ\text{C}$)	I_{DSS}	- -	- -	-1.0 -25	μAdc
Gate-Body Leakage Current ($V_{GS} = -20\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	-	-	-100	nAdc
Gate-Body Leakage Current ($V_{GS} = +20\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	-	-	100	nAdc

ON CHARACTERISTICS

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = -250\ \mu\text{Adc}$) Temperature Coefficient (Negative)	$V_{GS(th)}$	-1.0 -	-1.7 3.6	-3.0 -	Vdc
Static Drain-to-Source On-State Resistance ($V_{GS} = -10\text{ Vdc}$, $I_D = -2.48\text{ Adc}$) ($V_{GS} = -4.5\text{ Vdc}$, $I_D = -1.24\text{ Adc}$)	$R_{DS(on)}$	- -	0.063 0.100	0.085 0.135	Ω
Forward Transconductance ($V_{DS} = -15\text{ Vdc}$, $I_D = -1.24\text{ Adc}$)	g_{FS}	-	3.1	-	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = -24\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $f = 1.0\text{ MHz}$)	C_{iss}	-	500	-	pF
Output Capacitance		C_{oss}	-	160	-	
Reverse Transfer Capacitance		C_{rss}	-	65	-	

SWITCHING CHARACTERISTICS (Notes 7 & 8)

Turn-On Delay Time	$(V_{DD} = -24\text{ Vdc}$, $I_D = -2.48\text{ Adc}$, $V_{GS} = -10\text{ Vdc}$, $R_G = 6.0\ \Omega$)	$t_{d(on)}$	-	10	-	ns
Rise Time		t_r	-	20	-	
Turn-Off Delay Time		$t_{d(off)}$	-	40	-	
Fall Time		t_f	-	35	-	
Turn-On Delay Time	$(V_{DD} = -24\text{ Vdc}$, $I_D = -1.24\text{ Adc}$, $V_{GS} = -4.5\text{ Vdc}$, $R_G = 6.0\ \Omega$)	$t_{d(on)}$	-	16	-	ns
Rise Time		t_r	-	40	-	
Turn-Off Delay Time		$t_{d(off)}$	-	30	-	
Fall Time		t_f	-	30	-	
Total Gate Charge	$(V_{DS} = -24\text{ Vdc}$, $V_{GS} = -4.5\text{ Vdc}$, $I_D = -2.48\text{ Adc}$)	Q_{tot}	-	15	22	nC
Gate-Source Charge		Q_{gs}	-	3.2	-	
Gate-Drain Charge		Q_{gd}	-	4.0	-	

BODY-DRAIN DIODE RATINGS (Note 7)

Diode Forward On-Voltage	$(I_S = -2.48\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$) $(I_S = -2.48\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 125^\circ\text{C}$)	V_{SD}	- -	-0.92 -0.72	-1.3 -	Vdc
Reverse Recovery Time	$(I_S = -1.45\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$, $dI_S/dt = 100\text{ A}/\mu\text{s}$)	t_{rr}	-	38	-	ns
		t_a	-	20	-	
		t_b	-	18	-	
Reverse Recovery Stored Charge		Q_{RR}	-	0.04	-	μC

6. Handling precautions to protect against electrostatic discharge is mandatory.
7. Indicates Pulse Test: Pulse Width = 300 μsec max, Duty Cycle = 2%.
8. Switching characteristics are independent of operating junction temperature.

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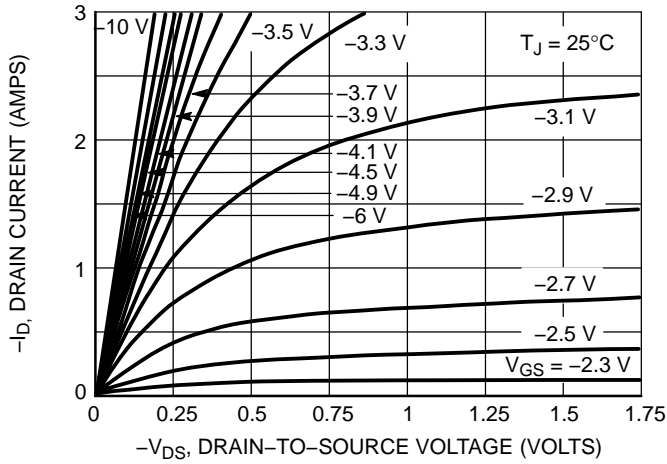


Figure 1. On-Region Characteristics

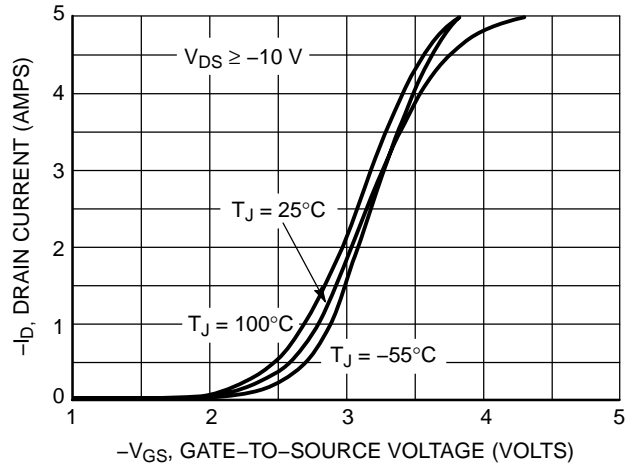


Figure 2. Transfer Characteristics

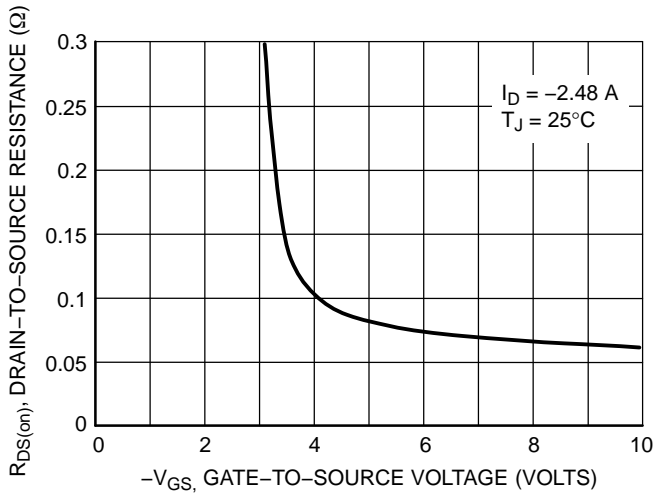


Figure 3. On-Resistance versus Gate-to-Source Voltage

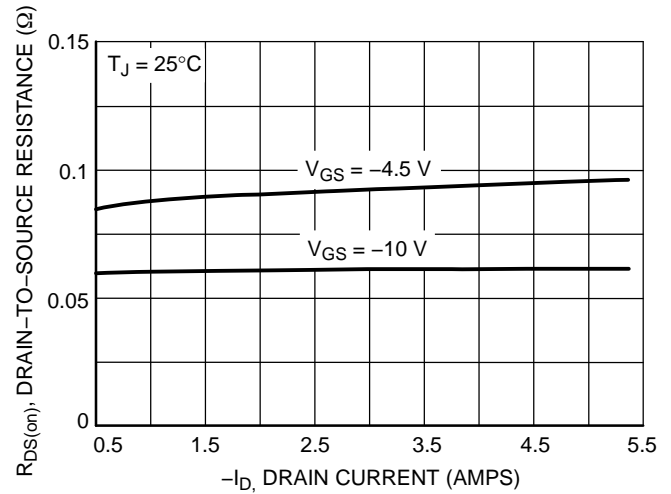


Figure 4. On-Resistance versus Drain Current and Gate Voltage

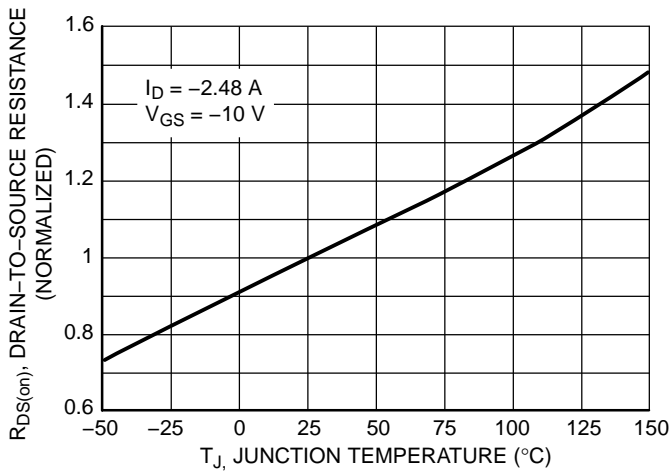


Figure 5. On-Resistance Variation with Temperature

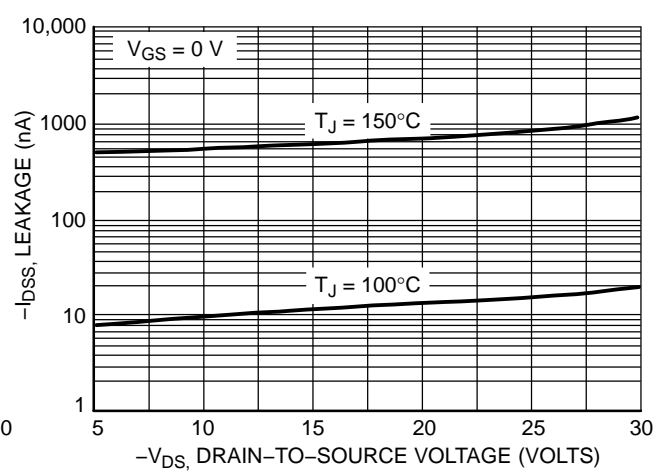


Figure 6. Drain-to-Source Leakage Current versus Voltage

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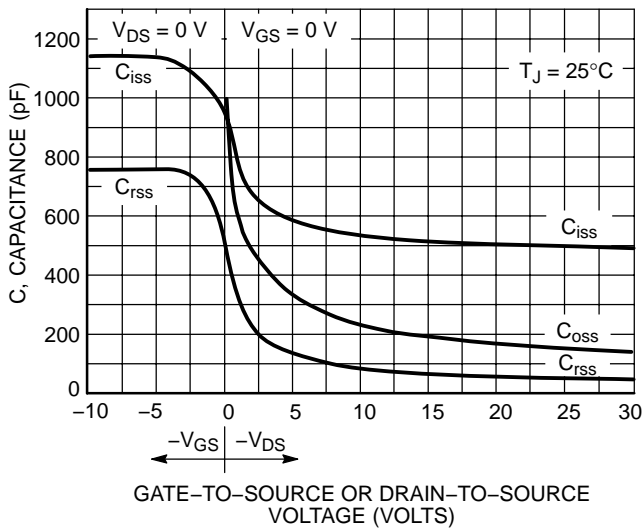


Figure 7. Capacitance Variation

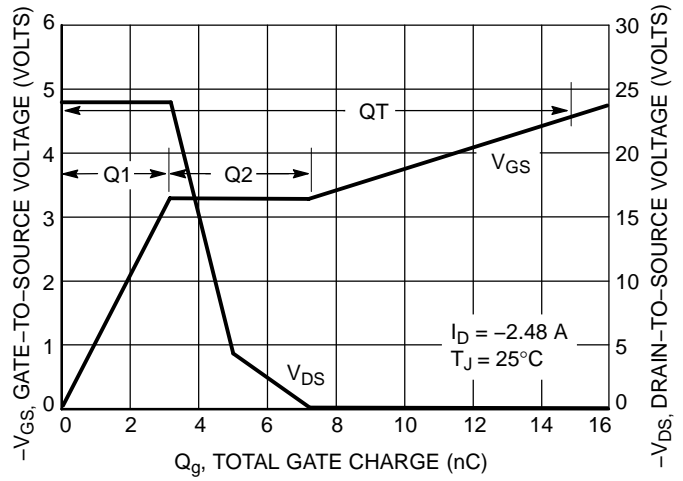


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

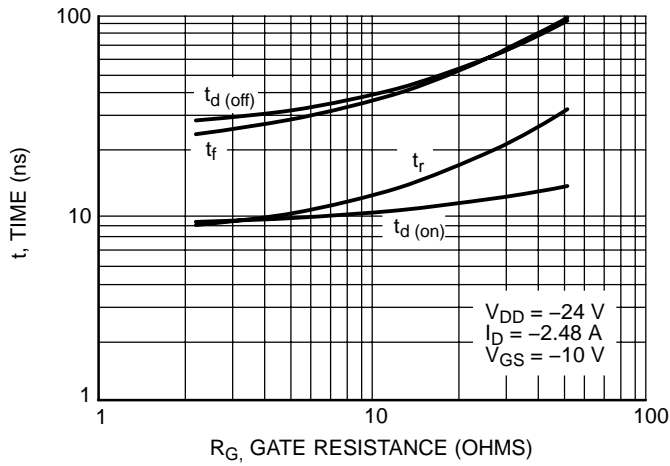


Figure 9. Resistive Switching Time Variation versus Gate Resistance

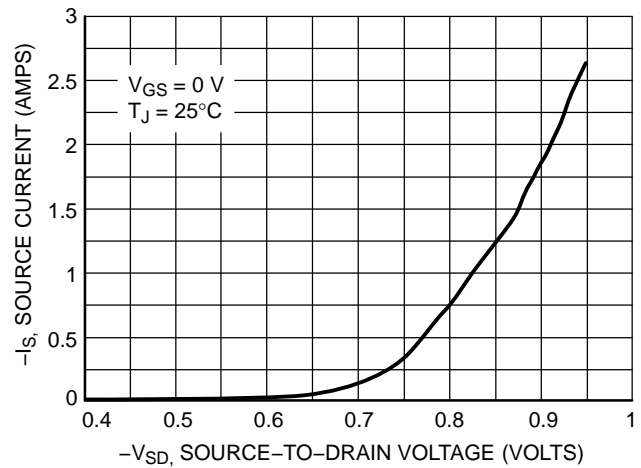


Figure 10. Diode Forward Voltage versus Current

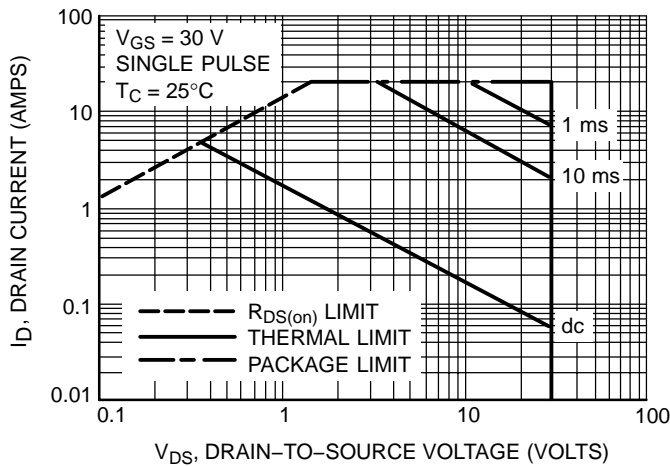


Figure 11. Maximum Rated Forward Biased Safe Operating Area

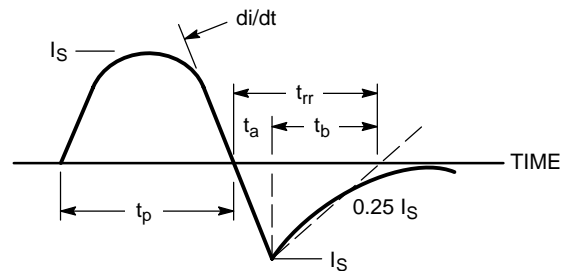


Figure 12. Diode Reverse Recovery Waveform

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TYPICAL ELECTRICAL CHARACTERISTICS

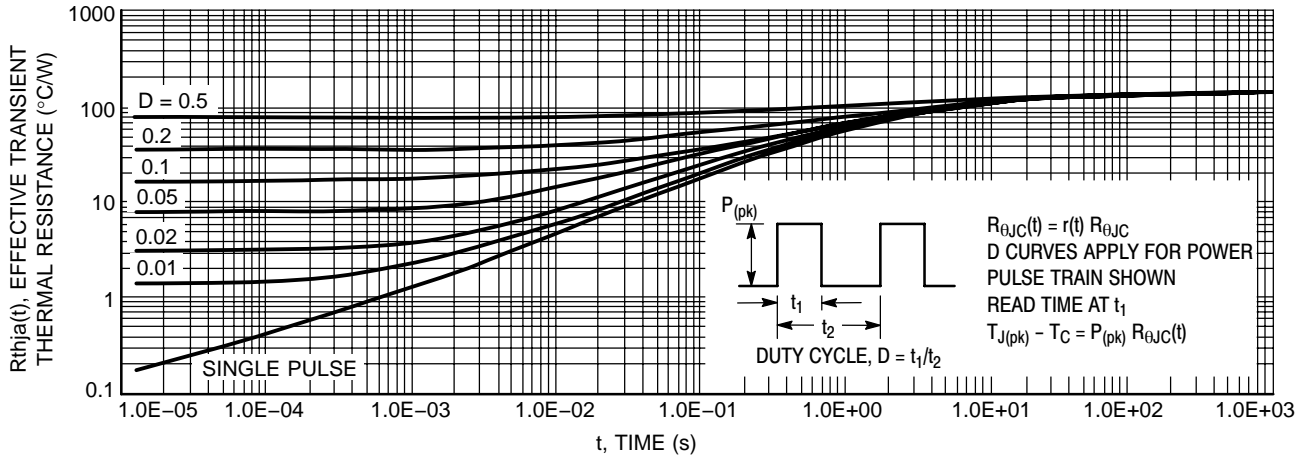


Figure 13. Thermal Response

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

Micro8 CASE 846A-02 ISSUE K

DATE 16 JUL 2020

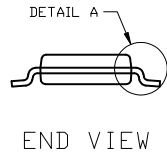


TOP VIEW

NOTE 3



SIDE VIEW



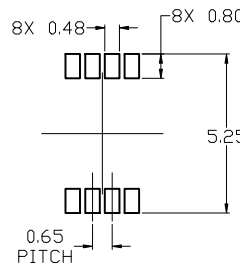
END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS *D* AND *E* DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION *E* DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS *D* AND *E* ARE DETERMINED AT DATUM *F*.
5. DATUMS *A* AND *B* ARE TO BE DETERMINED AT DATUM *F*.
6. *A1* IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

⌀ 0.08 (0.003) M C B S A S

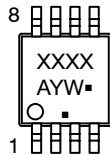
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
<i>b</i>	0.25	0.33	0.40
<i>c</i>	0.13	0.18	0.23
<i>D</i>	2.90	3.00	3.10
<i>E</i>	2.90	3.00	3.10
<i>e</i>	0.65 BSC		
<i>H_E</i>	4.75	4.90	5.05
<i>L</i>	0.40	0.55	0.70



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:

1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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