

NTMD5836NL

Power MOSFET

40 V, Dual N-Channel, SOIC-8

Features

- Asymmetrical N Channels
- Low $R_{DS(on)}$
- Low Capacitance
- Optimized Gate Charge
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

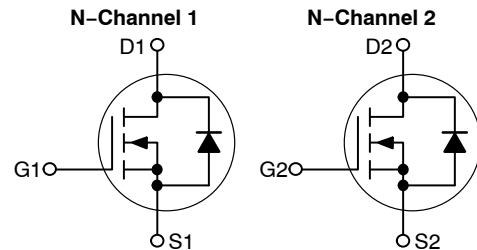
	$V_{(BR)DSS}$	$R_{DS(on)}$ Max	I_D Max (Notes 1 and 2)
Channel 1	40 V	12 m Ω @ 10 V	11 A
		16 m Ω @ 4.5 V	
Channel 2	40 V	20 m Ω @ 10 V	6.5 A
		36.5 m Ω @ 4.5 V	

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
2. Only selected channel is been powered
1W applied on channel 1: $T_J = 1 W * 85^{\circ}C/W + 25^{\circ}C = 110^{\circ}C$

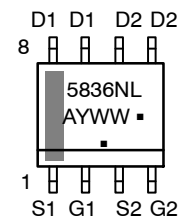


ON Semiconductor®

<http://onsemi.com>



MARKING DIAGRAM* AND PIN ASSIGNMENT



- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTMD5836NLR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

NTMD5836NL

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Symbol	Ch 1	Ch 2	Unit	
Drain-to-Source Voltage		V_{DSS}	40	40	V	
Gate-to-Source Voltage		V_{GS}	± 20	± 20	V	
Continuous Drain Current $R_{\theta JA}$ (Notes 3 and 4)	Steady State	$T_A = 25^\circ\text{C}$	I_D	9.0	5.7	A
		$T_A = 70^\circ\text{C}$		7.2	4.6	
Power Dissipation $R_{\theta JA}$ (Notes 3 and 4)		$T_A = 25^\circ\text{C}$	P_D	1.5	1.5	W
		$T_A = 70^\circ\text{C}$		0.9	0.9	
Continuous Drain Current $R_{\theta JA}$ (Notes 3 and 4)	$t \leq 10\text{s}$	$T_A = 25^\circ\text{C}$	I_D	11	6.5	A
		$T_A = 70^\circ\text{C}$		8.6	4.6	
Power Dissipation $R_{\theta JA}$ (Notes 3 and 4)		$T_A = 25^\circ\text{C}$	P_D	2.1	1.9	W
		$T_A = 70^\circ\text{C}$		1.3	1.2	
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM}	43	26	A	
Operating Junction and Storage Temperature		T_J, T_{STG}	-55 to +150		$^\circ\text{C}$	
Source Current (Body Diode)		I_S	10	7.0	A	
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 40\text{V}$, $V_{GS} = 10\text{V}$, $L = 0.1\text{mH}$)		E_{AS}	76	22	mJ	
		I_{AS}	39	21	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10s)		T_L	260		$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
4. Only selected channel is been powered
1W applied on channel 1: $T_J = 1\text{W} * 85^\circ\text{C}/\text{W} + 25^\circ\text{C} = 110^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Ch 1	Ch 2	Unit
Junction-to-Ambient Steady State (Notes 5 and 7)	$R_{\theta JA}$	85	86	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - $t \leq 10\text{s}$ (Notes 5 and 7)	$R_{\theta JA}$	60	65	
Junction-to-Ambient Steady State (Notes 5 and 8)	$R_{\theta JA}$	59		
Junction-to-Ambient Steady State (Notes 6 and 7)	$R_{\theta JA}$	136	136	

5. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
6. Surface-mounted on FR4 board using 0.155 in sq (100 mm²) pad size
7. Only selected channel is been powered
1W applied on channel 1: $T_J = 1\text{W} * 85^\circ\text{C}/\text{W} + 25^\circ\text{C} = 110^\circ\text{C}$
8. Both channels receive equivalent power dissipation
1 W applied on each channel: $T_J = 2\text{W} * 59^\circ\text{C}/\text{W} + 25^\circ\text{C} = 143^\circ\text{C}$

NTMD5836NL

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Ch	Min	Typ	Max	Unit	
OFF CHARACTERISTICS								
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	Ch 1	40			V	
			Ch 2					
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS} / T_J$		Ch 1		146		mV/ $^\circ\text{C}$	
			Ch 2		25			
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}$	$T_J = 25^\circ\text{C}$				1.0	μA
			Ch 1	Ch 2				
			$T_J = 125^\circ\text{C}$					
			Ch 1	Ch 2				
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	Ch 1			± 100	nA	
			Ch 2					

ON CHARACTERISTICS (Note 9)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	Ch 1	1.0	1.8	3.0	V		
			Ch 2	1.0	1.8	3.0			
Negative Threshold Temperature Coefficient	$V_{GS(TH)} / T_J$		Ch 1		6.0		mV/ $^\circ\text{C}$		
			Ch 2		6.0				
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	Ch 1		9.5	12	m Ω		
			Ch 2		16.2	20			
			Ch 1	Ch 2	$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		13	16	m Ω
					$V_{GS} = 4.5\text{ V}, I_D = 7\text{ A}$		25.0	36.5	
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$	Ch 1		10.5		S		
			Ch 2		6.0				

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 20\text{ V}$	Ch 1		2120		pF
			Ch 2		730		
Output Capacitance	C_{OSS}		Ch 1		315		
			Ch 2		123		
Reverse Transfer Capacitance	C_{RSS}		Ch 1		225		
			Ch 2		84		

9. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

10. Switching characteristics are independent of operating junction temperatures

NTMD5836NL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Ch	Min	Typ	Max	Unit
CHARGES, CAPACITANCES & GATE RESISTANCE							
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10V, V _{DS} = 20V, I _D = 10A	Ch 1		36	50	nC
		V _{GS} = 10 V, V _{DS} = 20 V, I _D = 7 A	Ch 2		16		
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 4.5 V, V _{DS} = 20 V, CH1: I _D = 10 A, CH2: I _D = 7 A	Ch 1		15	23	V
			Ch 2		8.5	11	
Gate-to-Source Charge	Q _{GS}		Ch 1		2.4		
			Ch 2		1.0		
Gate-to-Drain Charge	Q _{GD}		Ch 1		6.9		
			Ch 2		2.8		
Plateau Voltage	V _{GP}		Ch 1		7.2		
			Ch 2		4.0		
Gate Resistance	R _G	Ch 1		3.2			
		Ch 2		3.3			
Gate Resistance	R _G	Ch 1		1.2		Ω	
		Ch 2		2.1			

SWITCHING CHARACTERISTICS (Note 10)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 4.5 V, V _{DD} = 20 V, CH1: I _D = 10 A, CH2: I _D = 7 A, R _G = 2.5 Ω	Ch 1		16		ns
			Ch 2		11.5		
Rise Time	t _r		Ch 1		22		
			Ch 2		14		
Turn-Off Delay Time	t _{d(OFF)}		Ch 1		26		
			Ch 2		15.5		
Fall Time	t _f		Ch 1		8.5		
			Ch 2		3.5		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, CH1: I _D = 10 A, CH2: I _D = 7 A	T _J = 25°C	Ch 1		0.9	1.2	V
				Ch 2		0.85	1.2	
			T _J = 125°C	Ch 1		0.65		
				Ch 2		0.73		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _{SD} /dt = 100 A/μs, CH1: I _D = 10 A, CH2: I _D = 7 A	Ch 1		27		ns	
Charge Time	T _a		Ch 2		17			
			Ch 1		14			
Ch 2			11					
Discharge Time	T _b		Ch 1		13			
			Ch 2		6.0			
Reverse Recovery Charge	Q _{RR}		Ch 1		19		nC	
			Ch 2		9.0			

9. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%

10. Switching characteristics are independent of operating junction temperatures

TYPICAL PERFORMANCE CURVES

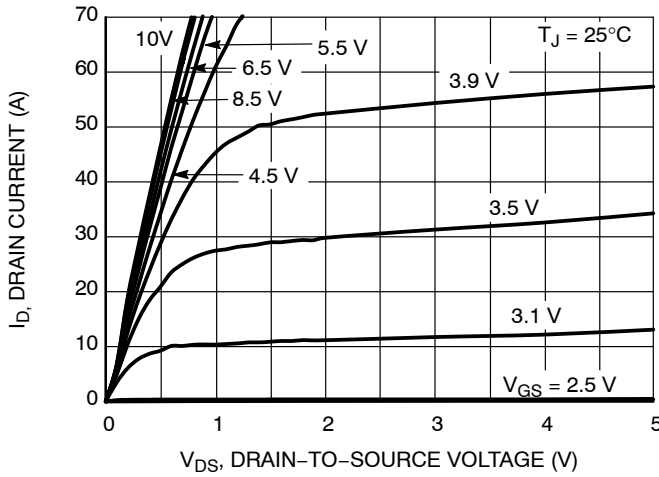


Figure 1. On-Region Characteristics - Channel 1

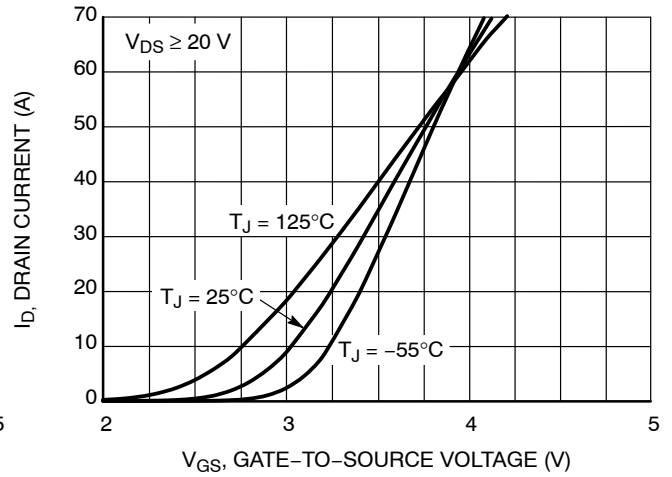


Figure 2. Transfer Characteristics - Channel 1

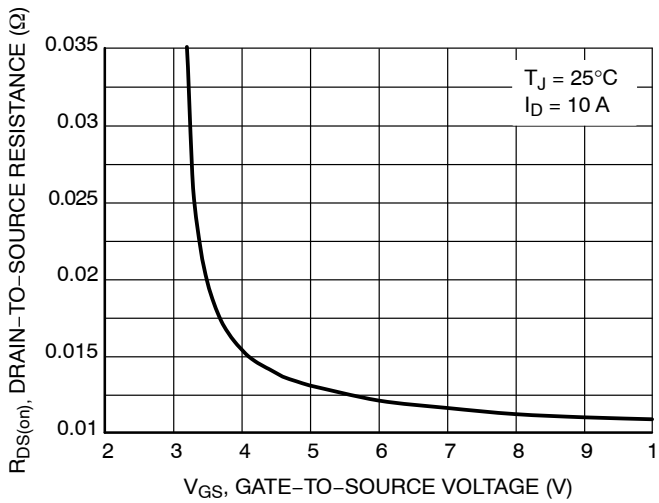


Figure 3. On-Resistance vs. Gate-to-Source Voltage - Channel 1

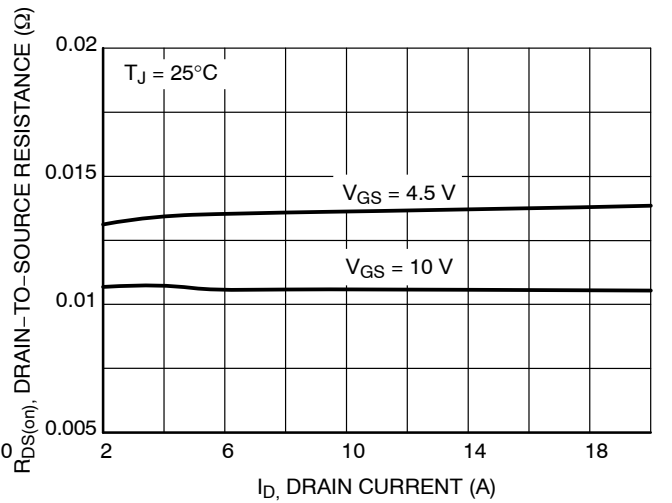


Figure 4. On-Resistance vs. Drain Current and Gate Voltage - Channel 1

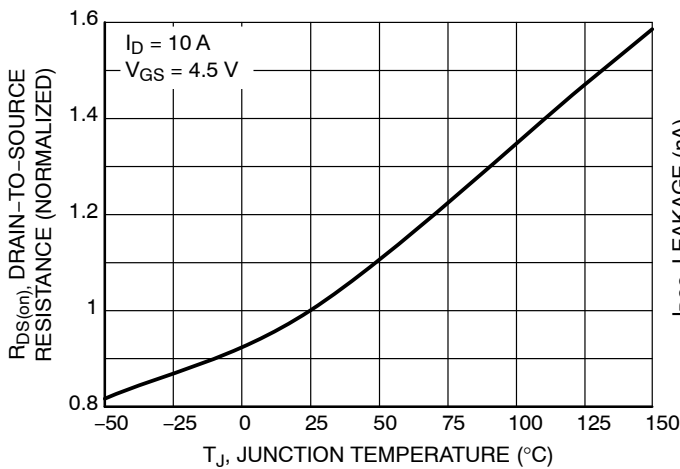


Figure 5. On-Resistance Variation with Temperature - Channel 1

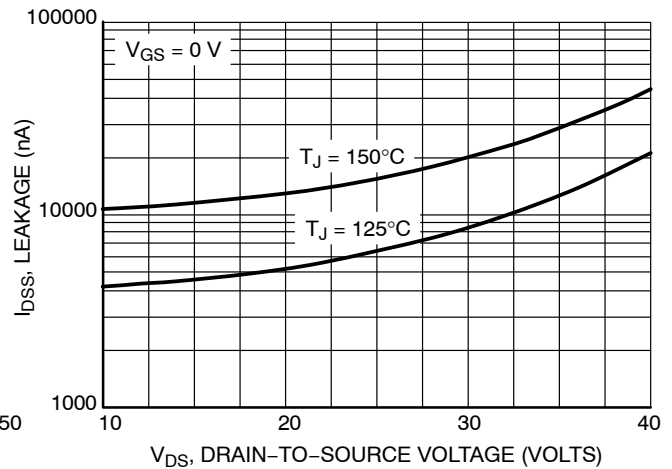


Figure 6. Drain-to-Source Leakage Current vs. Voltage - Channel 1

TYPICAL PERFORMANCE CURVES

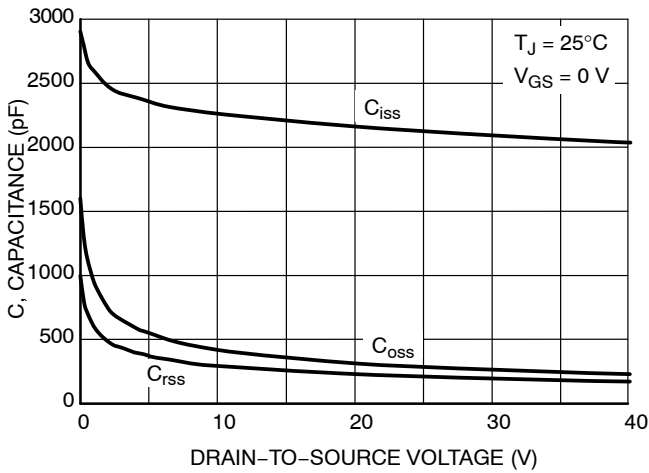


Figure 7. Capacitance Variation - Channel 1

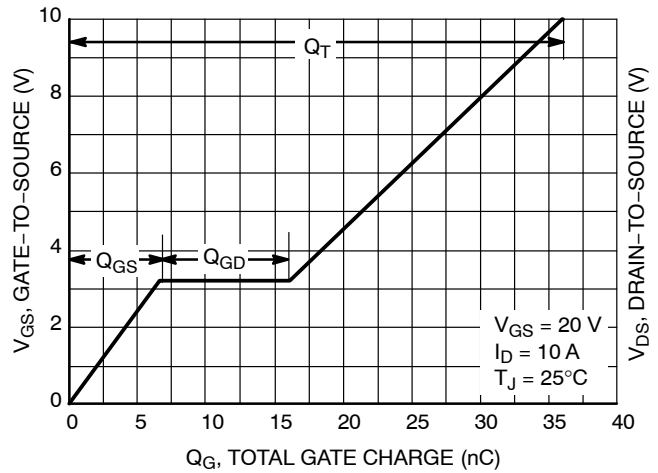


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge - Channel 1

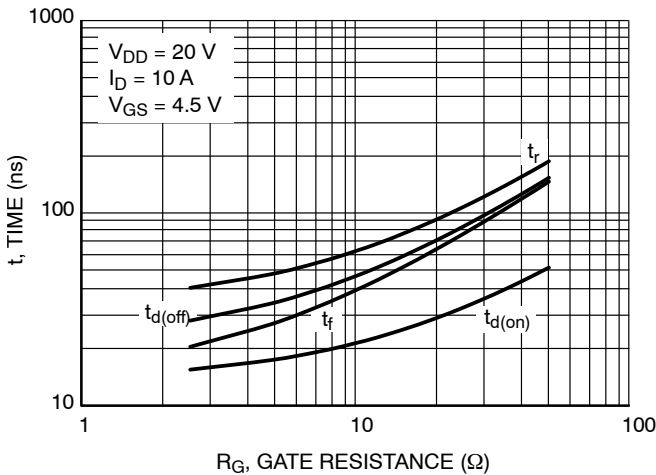


Figure 9. Resistive Switching Time Variation vs. Gate Resistance - Channel 1

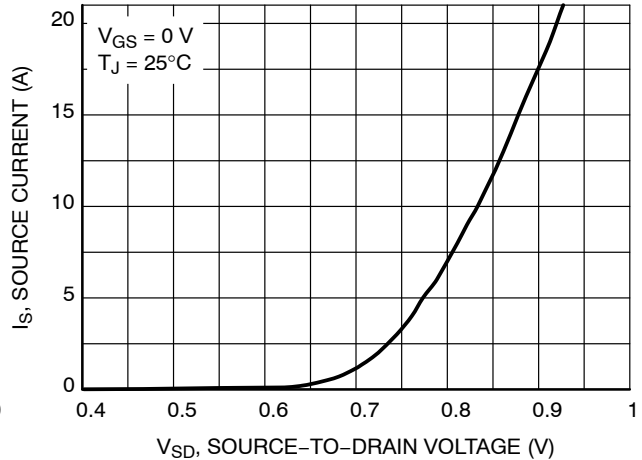


Figure 10. Diode Forward Voltage vs. Current - Channel 1

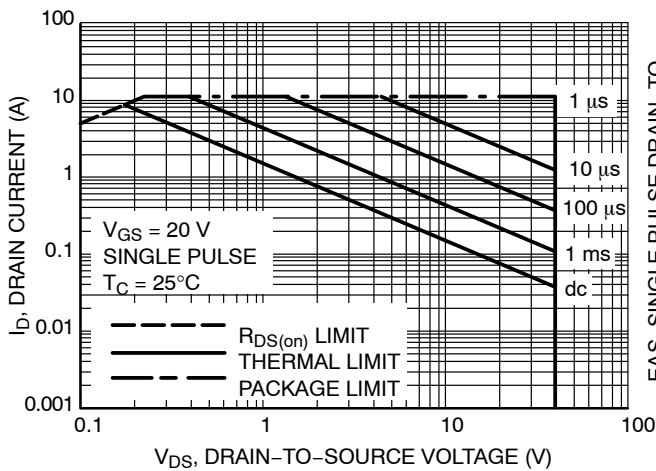


Figure 11. Maximum Rated Forward Biased Safe Operating Area - Channel 1

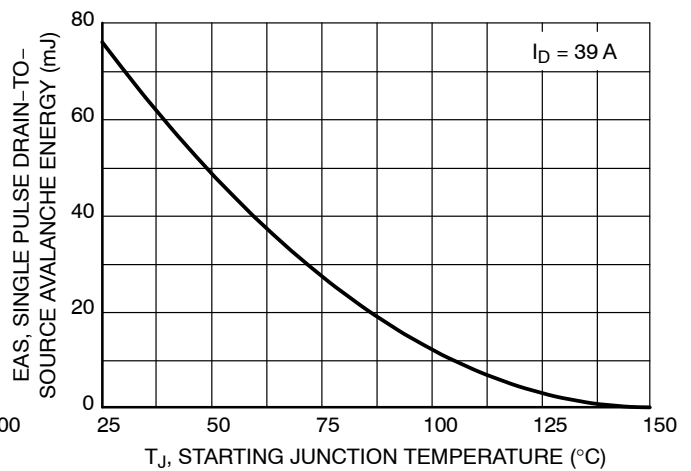


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature - Channel 1

TYPICAL PERFORMANCE CURVES

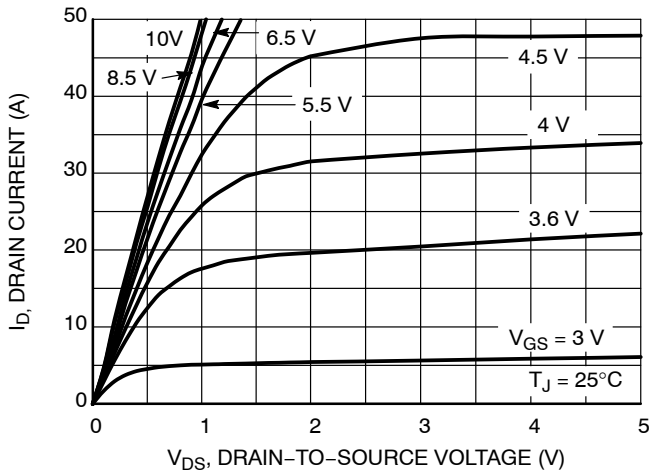


Figure 1. On-Region Characteristics - Channel 2

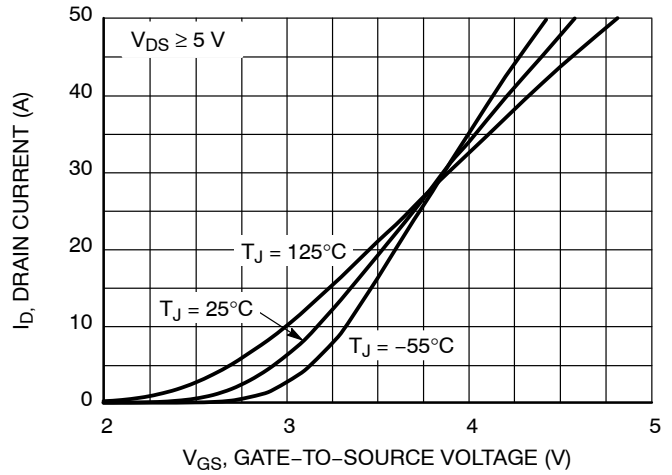


Figure 2. Transfer Characteristics - Channel 2

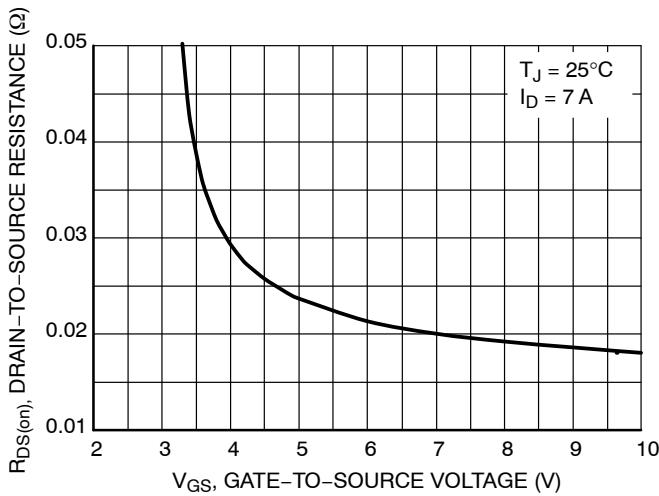


Figure 3. On-Resistance vs. Gate-to-Source Voltage - Channel 2

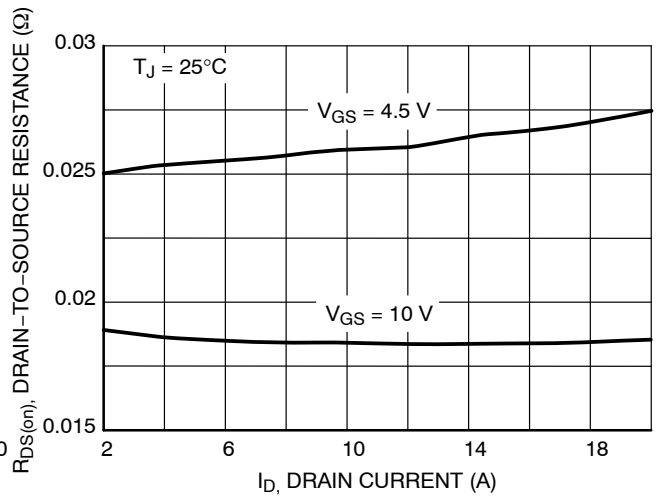


Figure 4. On-Resistance vs. Drain Current and Gate Voltage - Channel 2

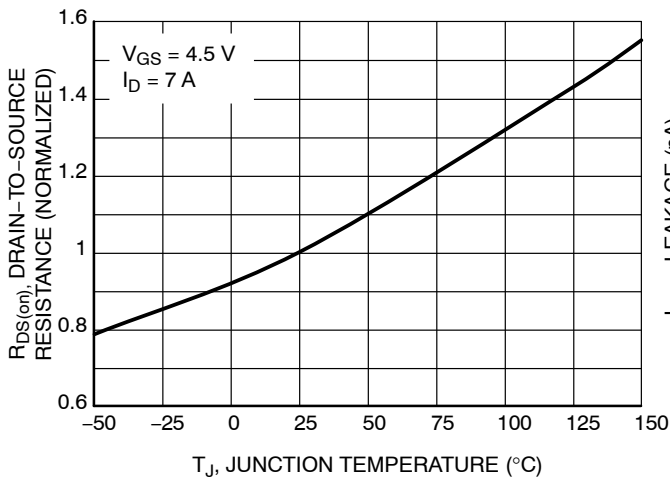


Figure 5. On-Resistance Variation with Temperature - Channel 2

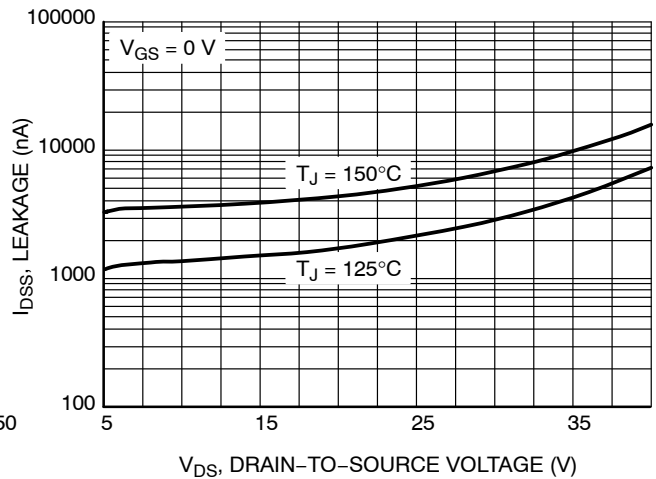


Figure 6. Drain-to-Source Leakage Current vs. Voltage - Channel 2

TYPICAL PERFORMANCE CURVES

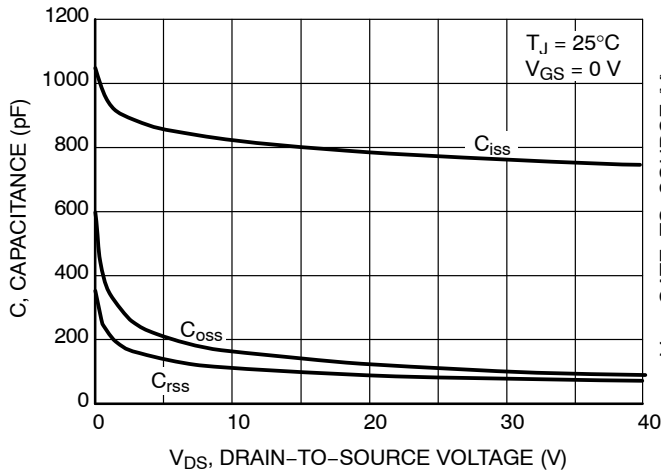


Figure 7. Capacitance Variation - Channel 2

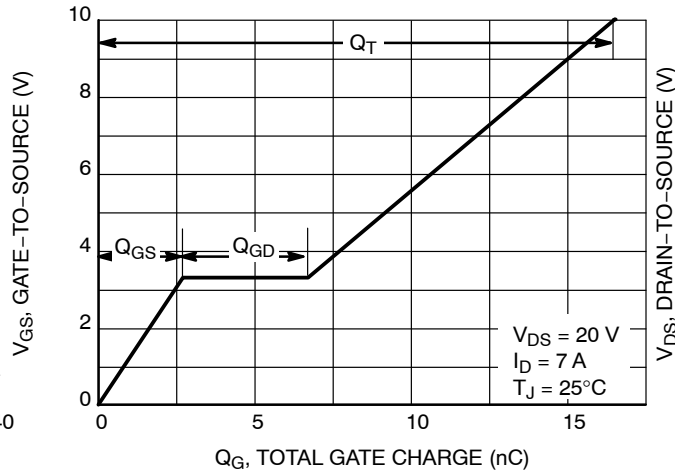


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

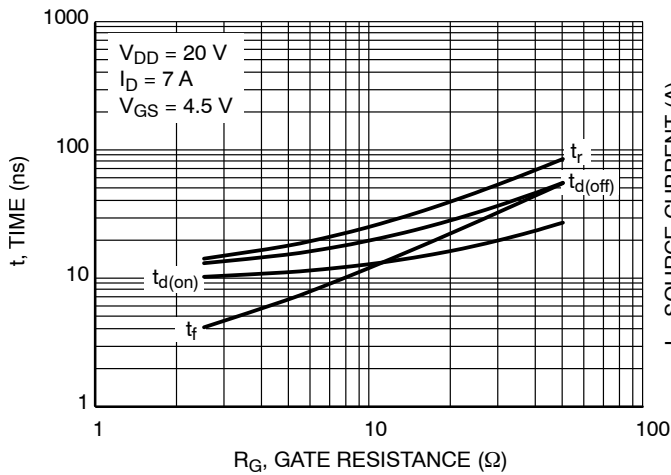


Figure 9. Resistive Switching Time Variation vs. Gate Resistance - Channel 2

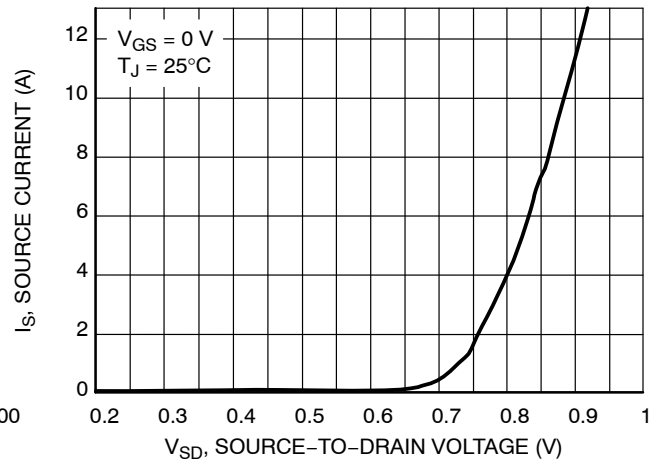


Figure 10. Diode Forward Voltage vs. Current - Channel 2

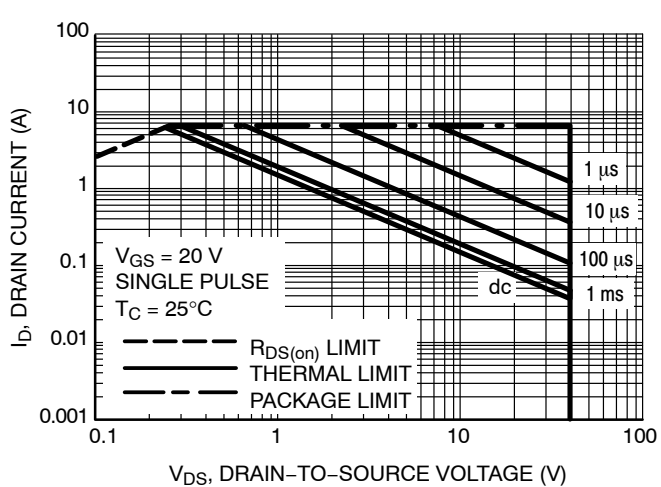


Figure 11. Maximum Rated Forward Biased Safe Operating Area - Channel 2

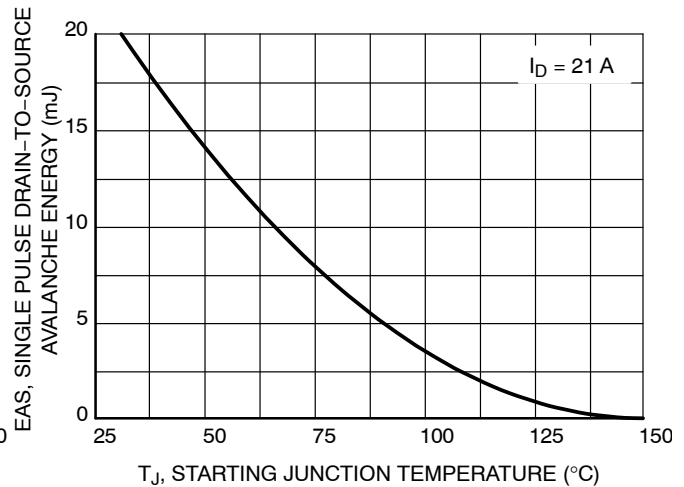


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

NTMD5836NL

TYPICAL PERFORMANCE CURVES

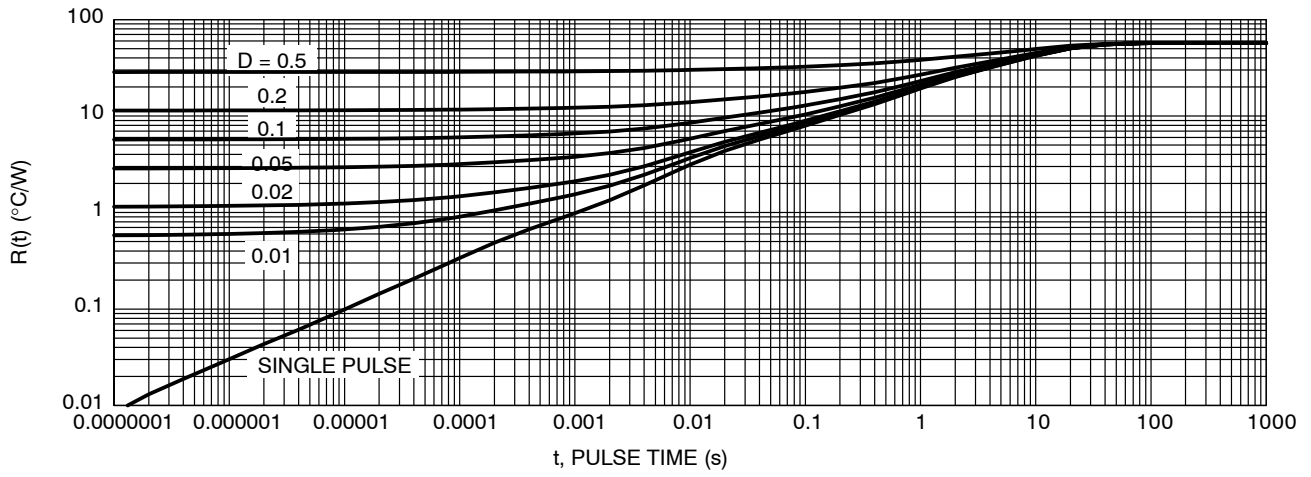


Figure 13. Thermal Response

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

onsemi and ONsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|---|--|--|--|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC_OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 2 OF 2

onsemi and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales