

# NTLUD3A50PZ

## MOSFET – Power, Dual, P-Channel, $\mu$ Cool, UDFN, 2.0x2.0x0.55 mm -20 V, -5.6 A



ON Semiconductor®

<http://onsemi.com>

### Features

- UDFN Package with Exposed Drain Pads for Excellent Thermal Conduction
- Low  $R_{DS(on)}$
- Low Profile UDFN 2.0x2.0x0.55 mm for Board Space Saving
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- High Side Load Switch
- Reverse Current Protection
- Battery Switch
- Optimized for Power Management Applications for Portable Products, such as Cell Phones, PMP, DSC, GPS, and others

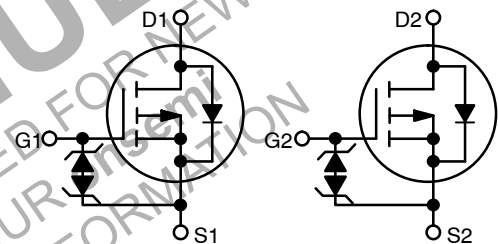
### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Units
Drain-to-Source Voltage	$V_{DSS}$	-20	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 8.0$	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$ -4.4 A
		$T_A = 85^\circ\text{C}$	-3.2
		$t \leq 5$ s	$T_A = 25^\circ\text{C}$
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$ 1.4 W
		$t \leq 5$ s	$T_A = 25^\circ\text{C}$
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$ -2.8 A
		$T_A = 85^\circ\text{C}$	-2.0
Power Dissipation (Note 2)	$T_A = 25^\circ\text{C}$	$P_D$ 0.5	W
Pulsed Drain Current	$t_p = 10$ $\mu\text{s}$	$I_{DM}$ -13	A
Operating Junction and Storage Temperature	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$
ESD (HBM, JESD22-A114) (MM, JESD22-A114)	$V_{ESD}$	1400 200	V
Source Current (Body Diode) (Note 2)	$I_S$	-1.0	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

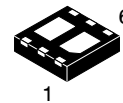
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces) based on both FETs on.

MOSFET		
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
-20 V	50 m $\Omega$ @ -4.5 V	-5.6 A
	70 m $\Omega$ @ -2.5 V	
	115 m $\Omega$ @ -1.8 V	
	175 m $\Omega$ @ -1.5 V	

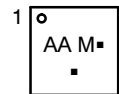


P-Channel MOSFET

### MARKING DIAGRAM



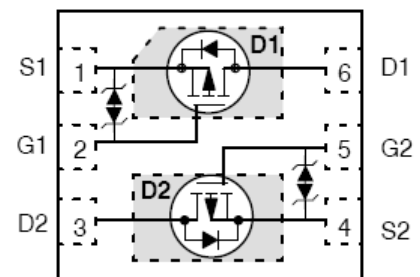
UDFN6  
CASE 517BF  
 $\mu$ COOL™



AA = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### PIN CONNECTIONS



(Top View)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

# NTLUD3A50PZ

2. Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm<sup>2</sup>, 1 oz. Cu based on both FETs on.

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Units
Junction-to-Ambient – Steady State (Note 3)	R <sub>θJA</sub>	91	°C/W
Junction-to-Ambient – t ≤ 5 s (Note 3)	R <sub>θJA</sub>	57	
Junction-to-Ambient – Steady State min Pad (Note 4)	R <sub>θJA</sub>	228	

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>	I <sub>D</sub> = -250 μA, ref to 25°C		-13		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -20 V			-1.0	μA
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±5.0 V			±5.0	μA

### ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250 μA	-0.4		-1.0	V
Negative Threshold Temp. Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			3.0		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -4.0 A		37	50	mΩ
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -3.0 A		46	70	
		V <sub>GS</sub> = -1.8 V, I <sub>D</sub> = -2.0 A		63	115	
		V <sub>GS</sub> = -1.5 V, I <sub>D</sub> = -1.0 A		86	175	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = -5.0 V, I <sub>D</sub> = -3.0 A		16		S

### CHARGES AND CAPACITANCES

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = -15 V		920		pF
Output Capacitance	C <sub>OSS</sub>			85		
Reverse Transfer Capacitance	C <sub>RSS</sub>			80		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -15 V; I <sub>D</sub> = -3.0 A		10.4		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			0.5		
Gate-to-Source Charge	Q <sub>GS</sub>			1.2		
Gate-to-Drain Charge	Q <sub>GD</sub>			3.0		

### SWITCHING CHARACTERISTICS, V<sub>GS</sub> = 4.5 V (Note 6)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = -4.5 V, V <sub>DD</sub> = -15 V, I <sub>D</sub> = -3.0 A, R <sub>G</sub> = 1 Ω		7.0		ns
Rise Time	t <sub>r</sub>			12		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			39		
Fall Time	t <sub>f</sub>			30		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	VSD	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -1.0 A	T <sub>J</sub> = 25°C		-0.67	-1.0	V
			T <sub>J</sub> = 125°C		-0.56		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces) based on both FETs on.
- Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm<sup>2</sup>, 1 oz. Cu based on both FETs on.
- Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperatures.

# NTLUD3A50PZ

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
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### DRAIN-SOURCE DIODE CHARACTERISTICS

Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}$ , $dis/dt = 100\text{ A}/\mu\text{s}$ , $I_S = -1.0\text{ A}$		12.1		ns
Charge Time	$t_a$			6.4		
Discharge Time	$t_b$			5.7		
Reverse Recovery Charge	$Q_{RR}$			4.0		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces) based on both FETs on.
- Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm<sup>2</sup>, 1 oz. Cu based on both FETs on.
- Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Switching characteristics are independent of operating junction temperatures.

DISCONTINUED

THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN  
PLEASE CONTACT YOUR onsemi  
REPRESENTATIVE FOR INFORMATION

# NTLUD3A50PZ

## TYPICAL CHARACTERISTICS

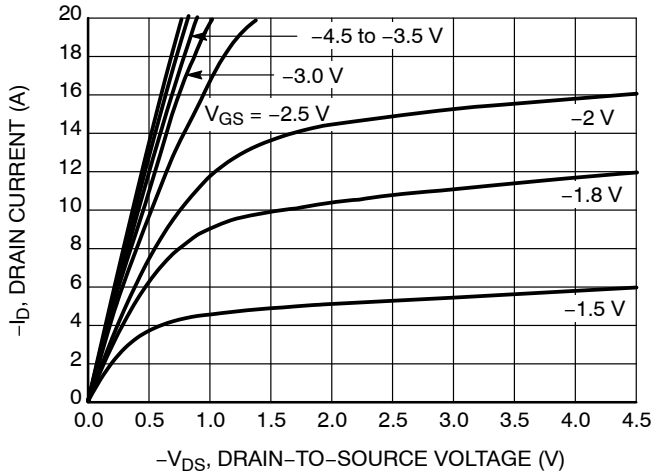


Figure 1. On-Region Characteristics

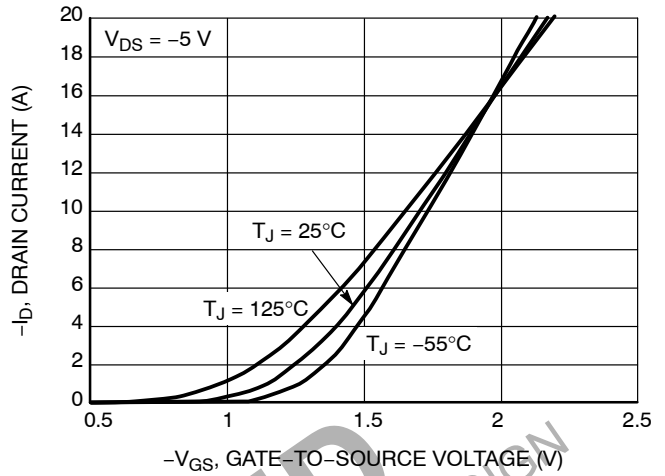


Figure 2. Transfer Characteristics

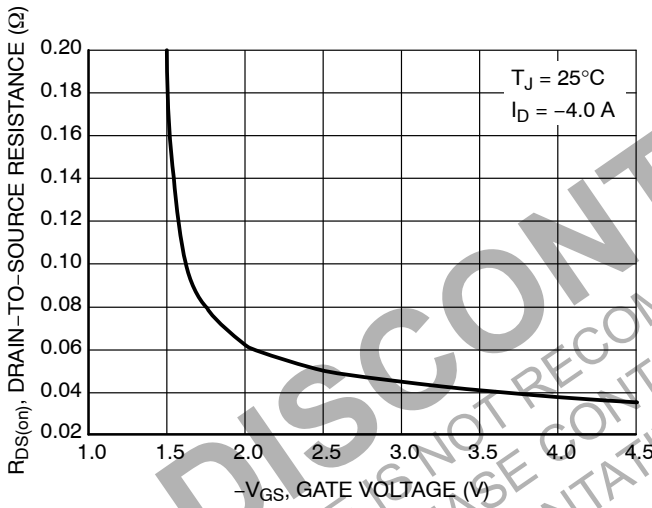


Figure 3. On-Resistance vs. Gate-to-Source Voltage

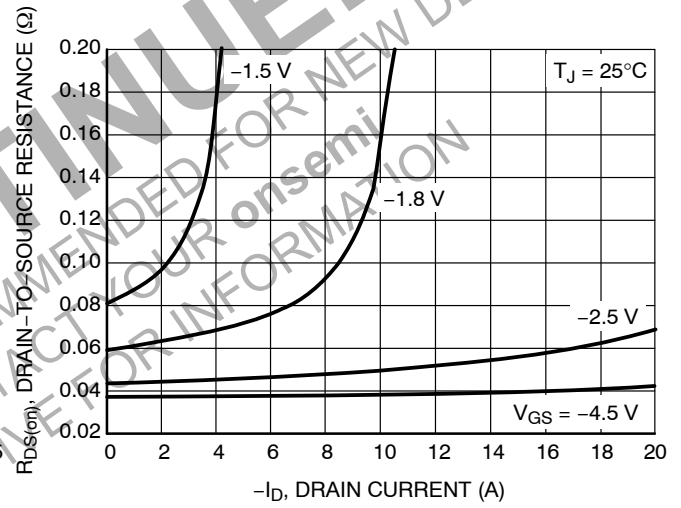


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

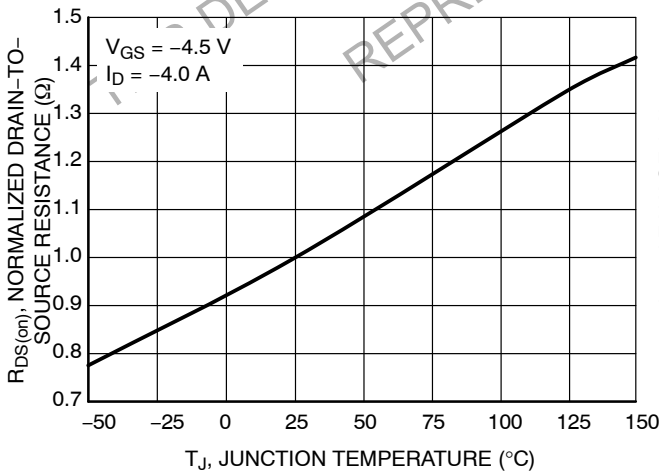


Figure 5. On-Resistance Variation with Temperature

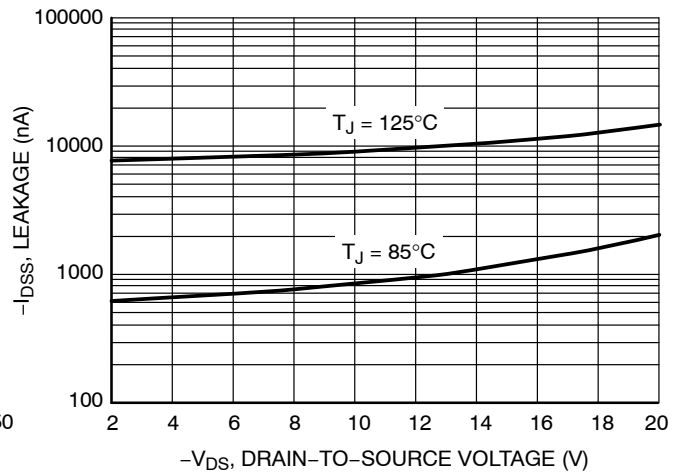


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NTLUD3A50PZ

## TYPICAL CHARACTERISTICS

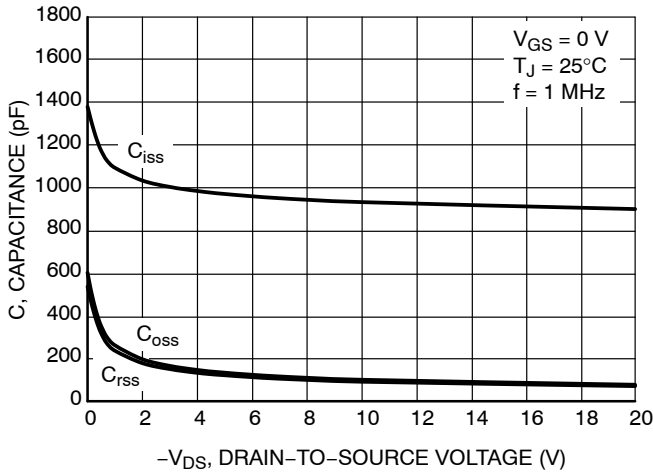


Figure 7. Capacitance Variation

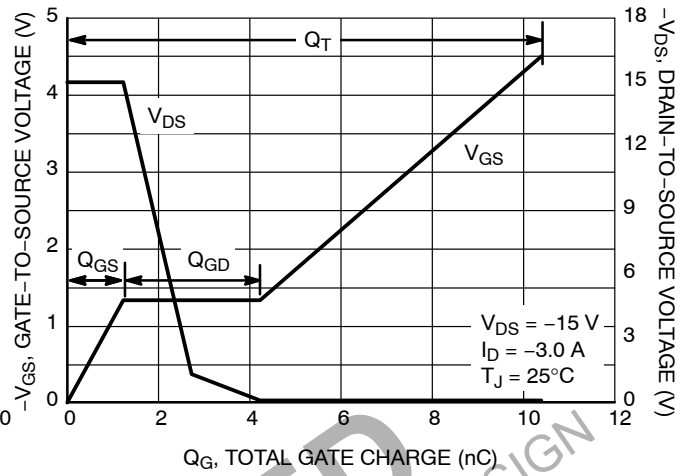


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

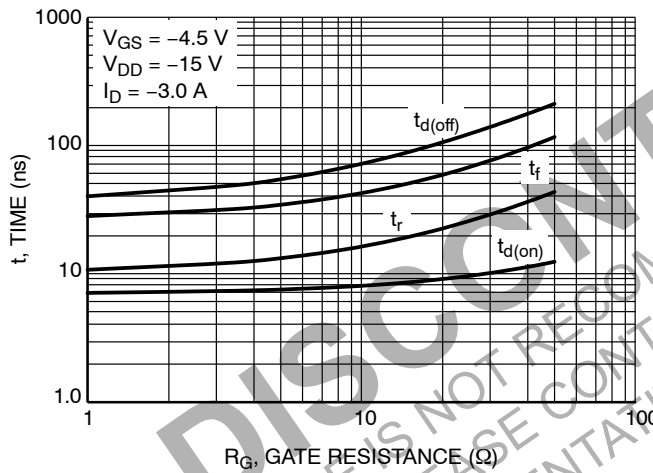


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

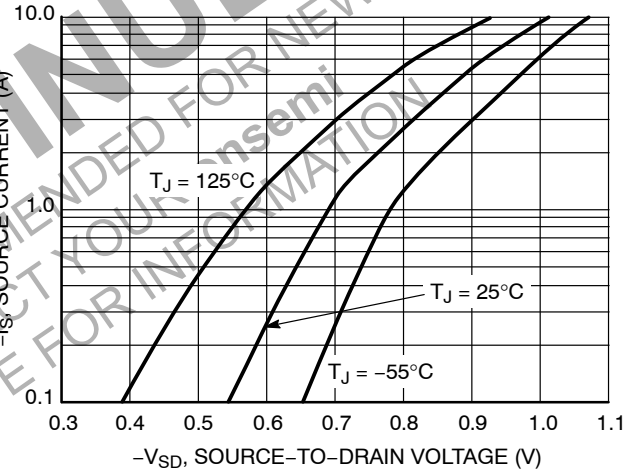


Figure 10. Diode Forward Voltage vs. Current

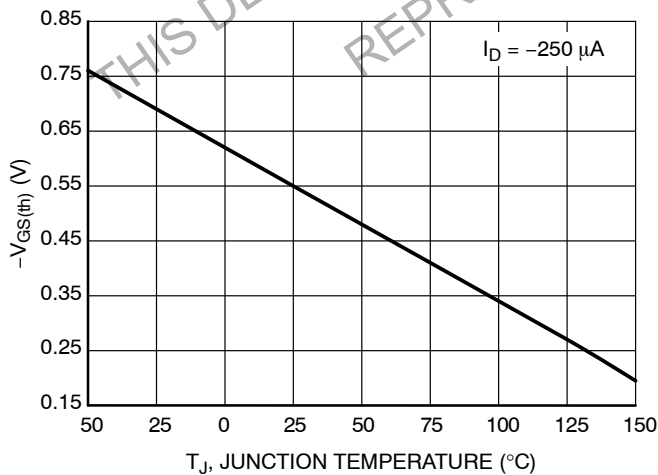


Figure 11. Threshold Voltage

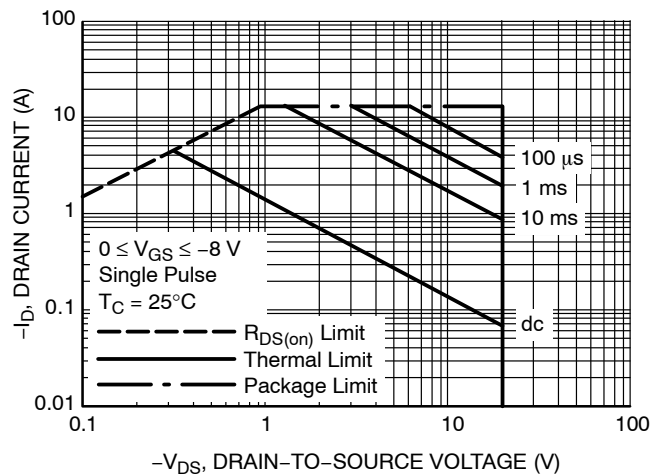


Figure 12. Maximum Rated Forward Biased Safe Operating Area

# NTLUD3A50PZ

## TYPICAL CHARACTERISTICS

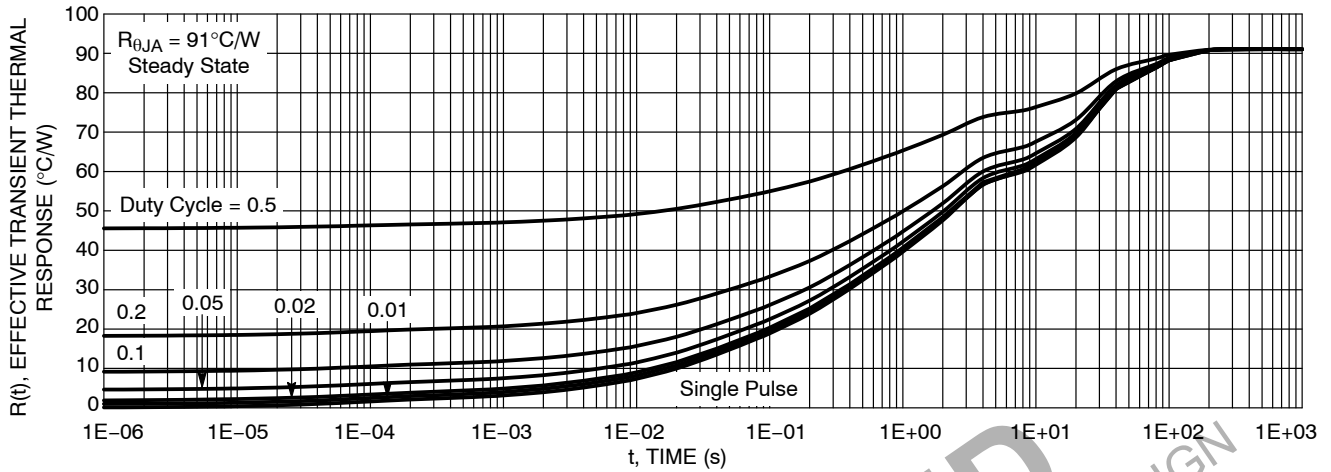


Figure 13. FET Thermal Response

### DEVICE ORDERING INFORMATION

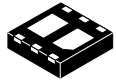
Device	Package	Shipping <sup>†</sup>
NTLUD3A50PZTAG	UDFN6 (Pb-Free)	3000 / Tape & Reel
NTLUD3A50PZTBG	UDFN6 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

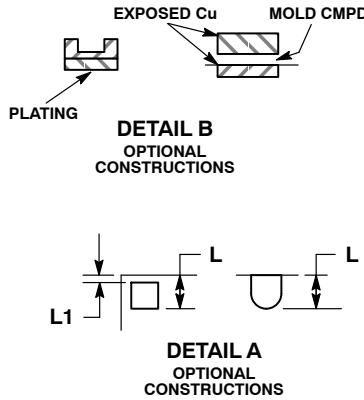
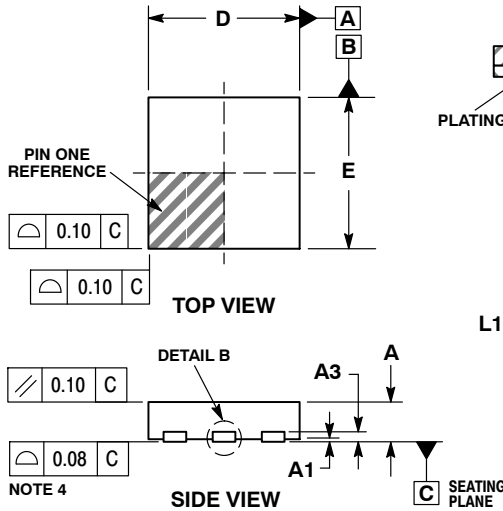
ON Semiconductor®



SCALE 4:1

### UDFN6 2x2, 0.65P CASE 517BF ISSUE B

DATE 20 AUG 2012



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

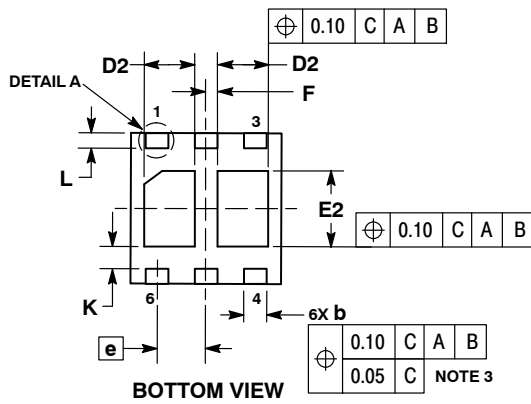
DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.57	0.77
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
F	0.15 BSC	
K	0.25 REF	
L	0.20	0.30
L1	---	0.10

### GENERIC MARKING DIAGRAM\*

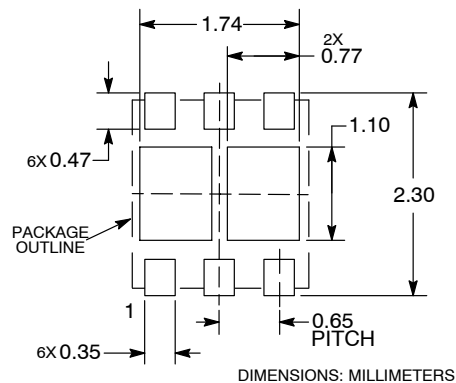


XX = Specific Device Code  
M = Date Code

(Note: Microdot may be in either location)  
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "C" or microdot "•", may or may not be present.



### RECOMMENDED MOUNTING FOOTPRINT



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