

# NTGS3446

## Power MOSFET 20 V, 5.1 A Single N-Channel, TSOP6

### Features

- Ultra Low  $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- $I_{DSS}$  Specified at Elevated Temperature
- Pb-Free Package is Available

### Applications

- Power Management in portable and battery-powered products, i.e. computers, printers, PCMCIA cards, cellular and cordless
- Lithium Ion Battery Applications
- Notebook PC

### MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	20	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 12$	V
Thermal Resistance Junction-to-Ambient (Note 1) Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$R_{\theta JA}$ $P_d$	244 0.5	$^\circ\text{C/W}$ W
Drain Current - Continuous @ $T_A = 25^\circ\text{C}$ - Pulsed Drain Current ( $t_p < 10 \mu\text{s}$ )	$I_D$ $I_{DM}$	2.5 10	A A
Thermal Resistance Junction-to-Ambient (Note 2) Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$R_{\theta JA}$ $P_d$	128 1.0	$^\circ\text{C/W}$ W
Drain Current - Continuous @ $T_A = 25^\circ\text{C}$ - Pulsed Drain Current ( $t_p < 10 \mu\text{s}$ )	$I_D$ $I_{DM}$	3.6 14	A A
Thermal Resistance Junction-to-Ambient (Note 3) Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$R_{\theta JA}$ $P_d$	62.5 2.0	$^\circ\text{C/W}$ W
Drain Current - Continuous @ $T_A = 25^\circ\text{C}$ - Pulsed Drain Current ( $t_p < 10 \mu\text{s}$ )	$I_D$ $I_{DM}$	5.1 20	A A
Source Current (Body Diode)	$I_S$	5.1	A
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$
Maximum Lead Temperature for Soldering Purposes for 10 seconds	$T_L$	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Minimum FR-4 or G-10PCB, operating to steady state.
2. Mounted onto a 2" square FR-4 board (1" sq. 2 oz. cu. 0.06" thick single-sided), operating to steady state.
3. Mounted onto a 2" square FR-4 board (1" sq. 2 oz. cu. 0.06" thick single-sided),  $t < 5.0$  seconds.

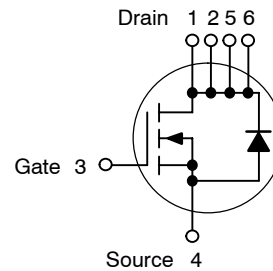


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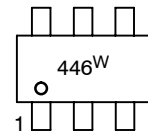
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
20 V	36 m $\Omega$ @ 4.5 V	5.1 A

### N-Channel



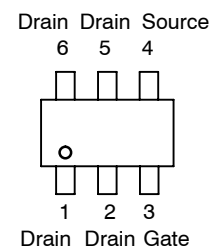
TSOP-6  
CASE 318G  
STYLE 1

### MARKING DIAGRAM



446 = Device Code  
W = Work Week

### PIN ASSIGNMENT



### ORDERING INFORMATION

Device	Package	Shipping†
NTGS3446T1	TSOP-6	3000/Tape & Reel
NTGS3446T1G	TSOP-6 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTGS3446

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 0.25 mAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	20 -	- 22	- -	Vdc mV/°C
Zero Gate Voltage Collector Current (V <sub>DS</sub> = 20 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 20 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 85°C)	I <sub>DSS</sub>	- -	- -	1.0 25	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ±12 Vdc, V <sub>DS</sub> = 0)	I <sub>GSS(f)</sub> I <sub>GSS(r)</sub>	- -	- -	100 -100	nAdc

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage I <sub>D</sub> = 0.25 mA, V <sub>DS</sub> = V <sub>GS</sub> Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	0.6 -	0.85 -2.5	1.2 -	Vdc mV/°C
Static Drain-to-Source On-Resistance (V <sub>GS</sub> = 4.5 Vdc, I <sub>D</sub> = 5.1 Adc) (V <sub>GS</sub> = 2.5 Vdc, I <sub>D</sub> = 4.4 Adc)	R <sub>DS(on)</sub>	- -	36 44	45 55	mΩ
Forward Transconductance (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 5.1 Adc)	g <sub>FS</sub>	-	12	-	mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 10 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>ISS</sub>	-	510	750	pF
Output Capacitance		C <sub>OSS</sub>	-	200	350	
Transfer Capacitance		C <sub>RSS</sub>	-	60	100	

### SWITCHING CHARACTERISTICS (Note 5)

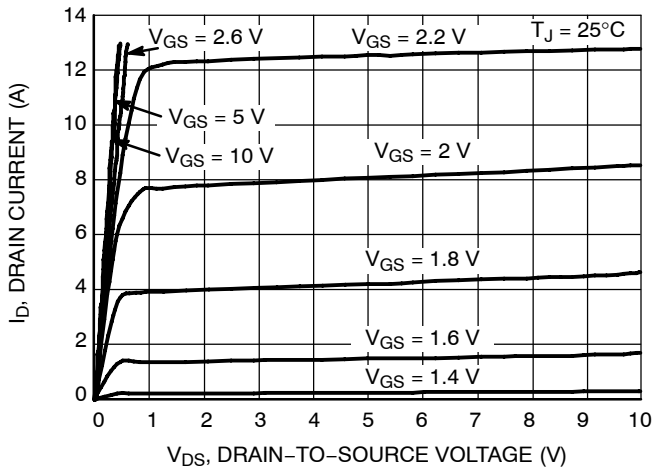
Turn-On Delay Time	(V <sub>DD</sub> = 10 Vdc, I <sub>D</sub> = 1.0 Adc, V <sub>GS</sub> = 4.5 Vdc, R <sub>G</sub> = 6.0 Ω)	t <sub>d(on)</sub>	-	9.0	16	ns
Rise Time		t <sub>r</sub>	-	12	20	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	35	60	
Fall Time		t <sub>f</sub>	-	20	35	
Gate Charge	(V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 5.1 Adc, V <sub>GS</sub> = 4.5 Vdc)	Q <sub>T</sub>	-	8.0	15	nC
		Q <sub>gs</sub>	-	2.0	-	
		Q <sub>gd</sub>	-	2.0	-	

### SOURCE-DRAIN DIODE CHARACTERISTICS

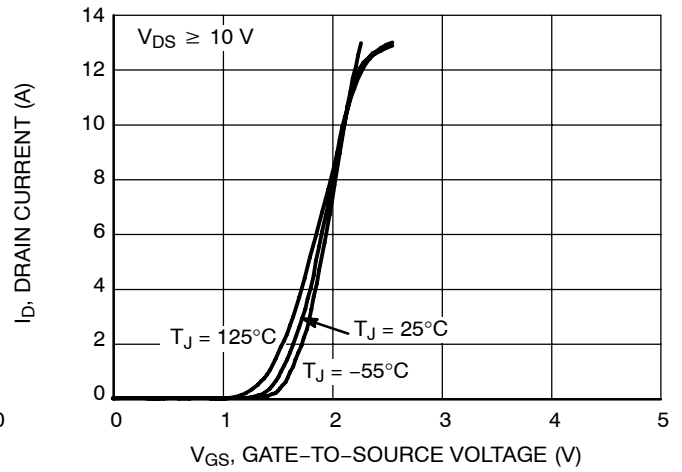
Forward On-Voltage (Note 4)	(I <sub>S</sub> = 1.7 Adc, V <sub>GS</sub> = 0 Vdc) (I <sub>S</sub> = 1.7 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 85°C)	V <sub>SD</sub>	- -	0.74 0.66	1.1 -	Vdc
Reverse Recovery Time		(I <sub>S</sub> = 1.7 Adc, V <sub>GS</sub> = 0 Vdc, di <sub>S</sub> /dt = 100 A/μs)	t <sub>rr</sub>	-	20	-
	t <sub>a</sub>		-	11	-	
	t <sub>b</sub>		-	9.0	-	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	-	0.01	-	μC

- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperature.

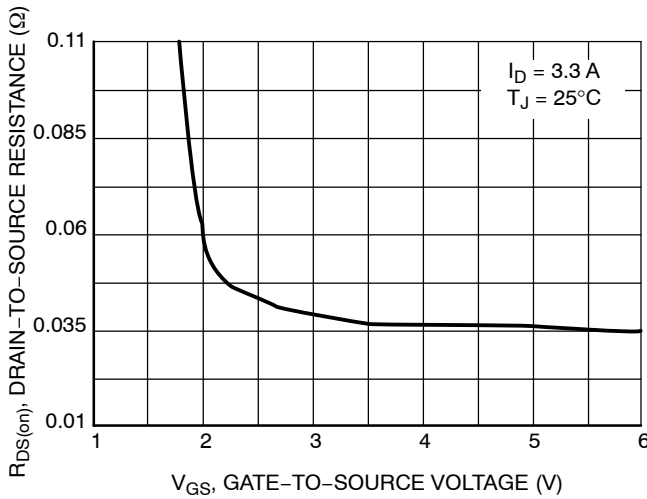
# NTGS3446



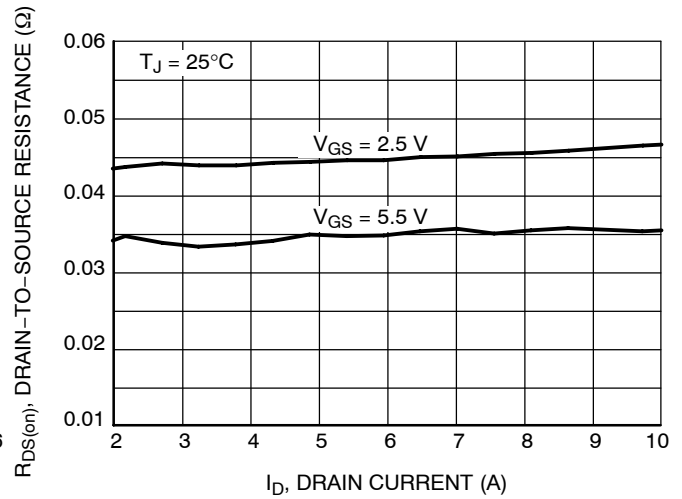
**Figure 1. On-Region Characteristics**



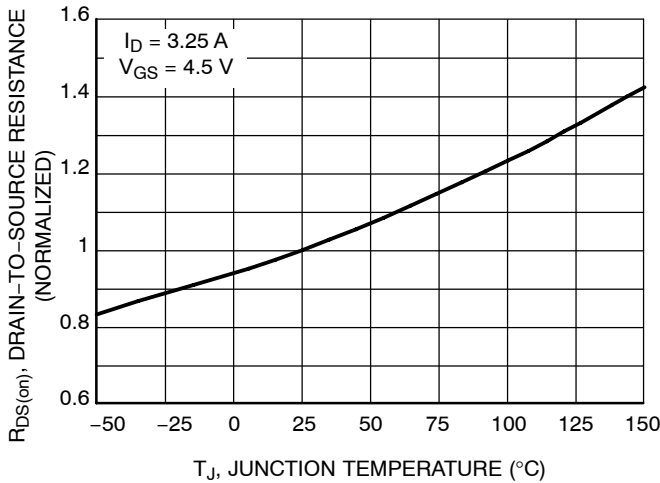
**Figure 2. Transfer Characteristics**



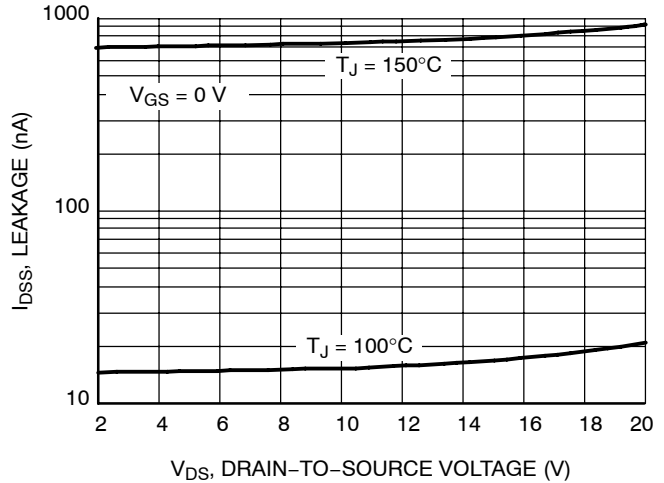
**Figure 3. On-Resistance versus Gate-to-Source Voltage**



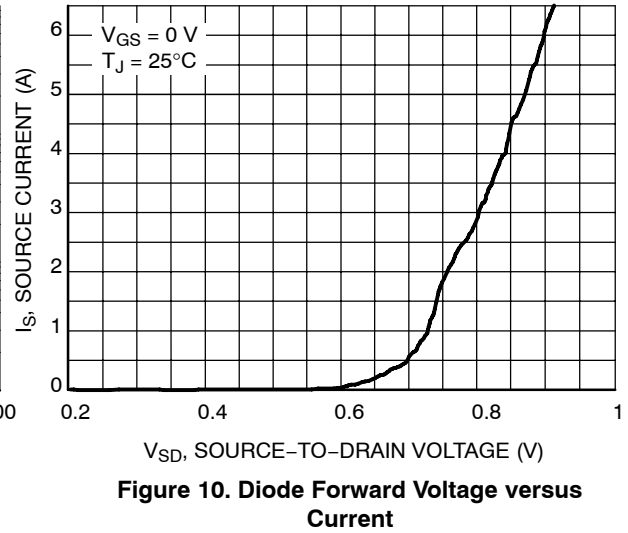
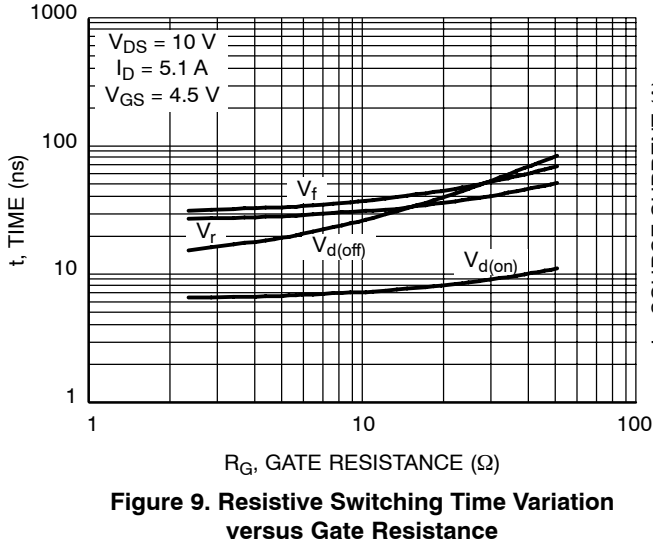
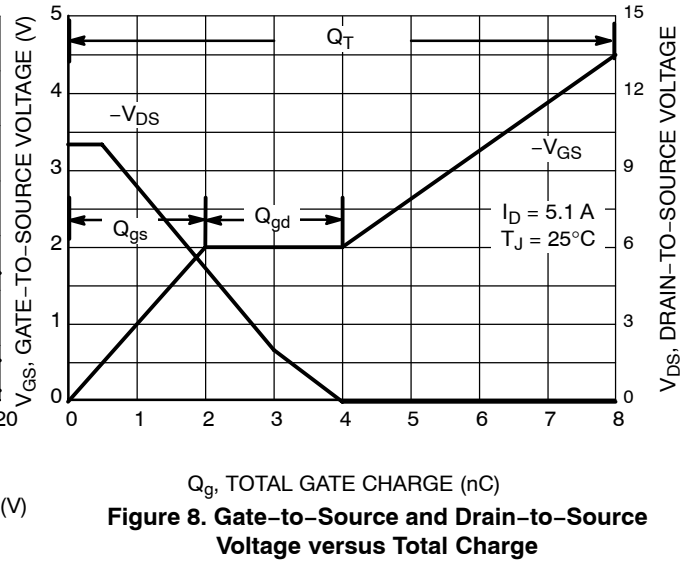
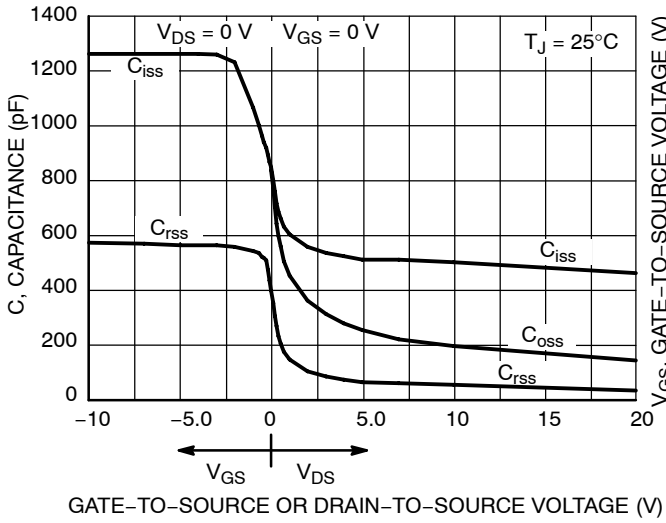
**Figure 4. On-Resistance versus Drain Current and Gate Voltage**



**Figure 5. On-Resistance Variation with Temperature**

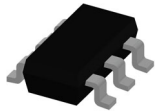


**Figure 6. Drain-to-Source Leakage Current versus Voltage**



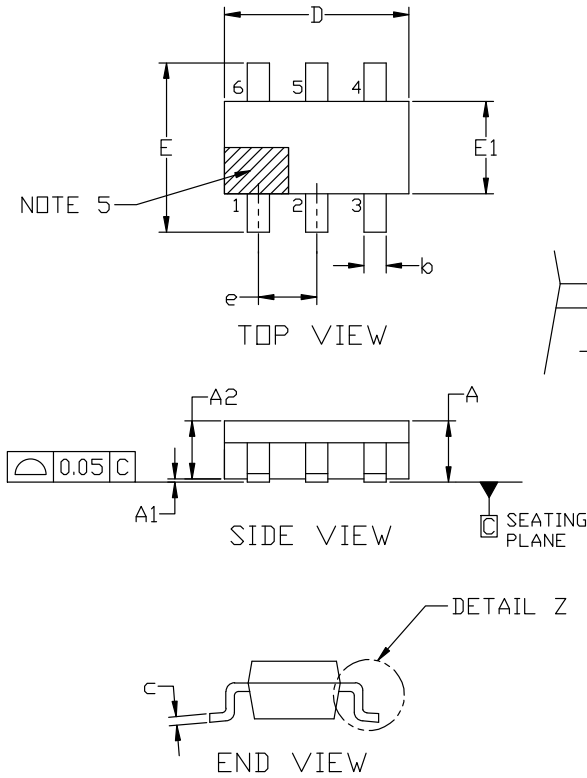
# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS



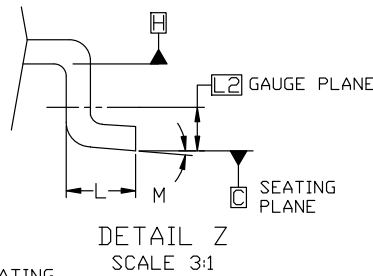
**TSOP-6 3.00x1.50x0.90, 0.95P**  
**CASE 318G**  
**ISSUE W**

DATE 26 FEB 2024

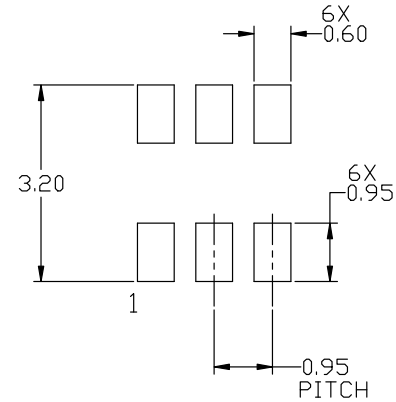


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE



MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

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# MECHANICAL CASE OUTLINE

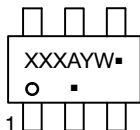
## PACKAGE DIMENSIONS



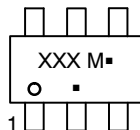
TSOP-6 3.00x1.50x0.90, 0.95P  
CASE 318G  
ISSUE W

DATE 26 FEB 2024

### GENERIC MARKING DIAGRAM\*



IC



STANDARD

XXX = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

- |  |  |   |   |   |  |
|--|--|---|---|---|--|
| <p>STYLE 1:<br/>PIN 1. DRAIN<br/>2. DRAIN<br/>3. GATE<br/>4. SOURCE<br/>5. DRAIN<br/>6. DRAIN</p>              | <p>STYLE 2:<br/>PIN 1. EMITTER 2<br/>2. BASE 1<br/>3. COLLECTOR 1<br/>4. EMITTER 1<br/>5. BASE 2<br/>6. COLLECTOR 2</p>    | <p>STYLE 3:<br/>PIN 1. ENABLE<br/>2. N/C<br/>3. R BOOST<br/>4. Vz<br/>5. V in<br/>6. V out</p>                            | <p>STYLE 4:<br/>PIN 1. N/C<br/>2. V in<br/>3. NOT USED<br/>4. GROUND<br/>5. ENABLE<br/>6. LOAD</p>                | <p>STYLE 5:<br/>PIN 1. EMITTER 2<br/>2. BASE 2<br/>3. COLLECTOR 1<br/>4. EMITTER 1<br/>5. BASE 1<br/>6. COLLECTOR 2</p> | <p>STYLE 6:<br/>PIN 1. COLLECTOR<br/>2. COLLECTOR<br/>3. BASE<br/>4. EMITTER<br/>5. COLLECTOR<br/>6. COLLECTOR</p> |
| <p>STYLE 7:<br/>PIN 1. COLLECTOR<br/>2. COLLECTOR<br/>3. BASE<br/>4. N/C<br/>5. COLLECTOR<br/>6. EMITTER</p>   | <p>STYLE 8:<br/>PIN 1. Vbus<br/>2. D(in)<br/>3. D(in)+<br/>4. D(out)+<br/>5. D(out)<br/>6. GND</p>                         | <p>STYLE 9:<br/>PIN 1. LOW VOLTAGE GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN<br/>5. DRAIN<br/>6. HIGH VOLTAGE GATE</p> | <p>STYLE 10:<br/>PIN 1. D(OUT)+<br/>2. GND<br/>3. D(OUT)-<br/>4. D(IN)-<br/>5. VBUS<br/>6. D(IN)+</p>             | <p>STYLE 11:<br/>PIN 1. SOURCE 1<br/>2. DRAIN 2<br/>3. DRAIN 2<br/>4. SOURCE 2<br/>5. GATE 1<br/>6. DRAIN 1/GATE 2</p>  | <p>STYLE 12:<br/>PIN 1. I/O<br/>2. GROUND<br/>3. I/O<br/>4. I/O<br/>5. VCC<br/>6. I/O</p>                          |
| <p>STYLE 13:<br/>PIN 1. GATE 1<br/>2. SOURCE 2<br/>3. GATE 2<br/>4. DRAIN 2<br/>5. SOURCE 1<br/>6. DRAIN 1</p> | <p>STYLE 14:<br/>PIN 1. ANODE<br/>2. SOURCE<br/>3. GATE<br/>4. CATHODE/DRAIN<br/>5. CATHODE/DRAIN<br/>6. CATHODE/DRAIN</p> | <p>STYLE 15:<br/>PIN 1. ANODE<br/>2. SOURCE<br/>3. GATE<br/>4. DRAIN<br/>5. N/C<br/>6. CATHODE</p>                        | <p>STYLE 16:<br/>PIN 1. ANODE/CATHODE<br/>2. BASE<br/>3. EMITTER<br/>4. COLLECTOR<br/>5. ANODE<br/>6. CATHODE</p> | <p>STYLE 17:<br/>PIN 1. EMITTER<br/>2. BASE<br/>3. ANODE/CATHODE<br/>4. ANODE<br/>5. CATHODE<br/>6. COLLECTOR</p>       |  |

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