

NTGS3433T1

MOSFET – P-Channel, TSOP-6

-3.3 A, -12 V



ON Semiconductor®

<http://onsemi.com>

Features

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Miniature TSOP-6 Surface Mount Package
- Pb-Free Package is Available

Applications

- Power Management in Portable and Battery-Powered Products, i.e.: Cellular and Cordless Telephones, and PCMCIA Cards

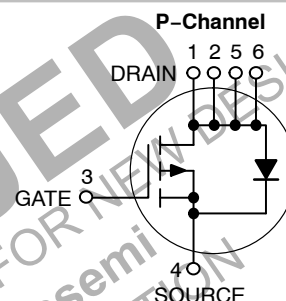
MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	-12	Volts
Gate-to-Source Voltage – Continuous	V_{GS}	± 8.0	Volts
Thermal Resistance Junction-to-Ambient (Note 1)	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_d	2.0	Watts
Drain Current	I_D	-3.3	Amps
– Continuous @ $T_A = 25^\circ\text{C}$	I_{DM}	-20	Amps
– Pulsed Drain Current ($T_p < 10 \mu\text{s}$)	P_d	1.0	Watts
Maximum Operating Power Dissipation	I_D	-2.35	Amps
Maximum Operating Drain Current			
Thermal Resistance Junction-to-Ambient (Note 2)	$R_{\theta JA}$	128	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_d	1.0	Watts
Drain Current	I_D	-2.35	Amps
– Continuous @ $T_A = 25^\circ\text{C}$	I_{DM}	-14	Amps
– Pulsed Drain Current ($T_p < 10 \mu\text{s}$)	P_d	0.5	Watts
Maximum Operating Power Dissipation	I_D	-1.65	Amps
Maximum Operating Drain Current			
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Maximum Lead Temperature for Soldering Purposes for 10 Seconds	T_L	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Mounted onto a 2" square FR-4 board (1 in sq. 2 oz. Cu 0.06" thick single sided), $t < 5.0$ seconds.
2. Mounted onto a 2" square FR-4 board (1 in sq. 2 oz. Cu 0.06" thick single sided), operating to steady state.

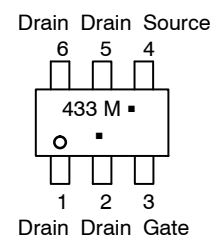
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D Max
-12 V	75 m Ω @ -4.5 V	-3.3 A



MARKING DIAGRAM & PIN ASSIGNMENT



**TSOP-6
CASE 318G
STYLE 1**



433 = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NTGS3433T1	TSOP-6	3000 Tape & Reel
NTGS3433T1G	TSOP-6 (Pb-Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTGS3433T1

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Notes 3 & 4)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = -10 μA)	V _{(BR)DSS}	-12	-	-	Vdc
Zero Gate Voltage Drain Current (V _{GS} = 0 Vdc, V _{DS} = -8 Vdc, T _J = 25°C) (V _{GS} = 0 Vdc, V _{DS} = -8 Vdc, T _J = 70°C)	I _{DSS}	-	-	-1.0 -5.0	μAdc
Gate-Body Leakage Current (V _{GS} = -8.0 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	-	-	-100	nAdc
Gate-Body Leakage Current (V _{GS} = +8.0 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	-	-	100	nAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = -250 μAdc)	V _{GS(th)}	-0.50	-0.70	-1.50	Vdc
Static Drain-Source On-State Resistance (V _{GS} = -4.5 Vdc, I _D = -3.3 Adc) (V _{GS} = -2.5 Vdc, I _D = -2.9 Adc)	R _{DS(on)}	-	0.055 0.075	0.075 0.095	Ω
Forward Transconductance (V _{DS} = -10 Vdc, I _D = -3.3 Adc)	g _{FS}	-	7.0	-	mhos

DYNAMIC CHARACTERISTICS

Total Gate Charge	(V _{DS} = -10 Vdc, V _{GS} = -4.5 Vdc, I _D = -3.3 Adc)	Q _{tot}	7.0	15	nC
Gate-Source Charge		Q _{gs}	2.0	-	
Gate-Drain Charge		Q _{gd}	3.5	-	
Input Capacitance	(V _{DS} = -5.0 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	550	-	pF
Output Capacitance		C _{oss}	450	-	
Reverse Transfer Capacitance		C _{rss}	200	-	

SWITCHING CHARACTERISTICS

Turn-On Delay Time	(V _{DD} = -10 Vdc, I _D = -1.0 Adc, V _{GS} = -4.5 Vdc, R _g = 6.0 Ω)	t _{d(on)}	-	20	30	ns
Rise Time		t _r	-	20	30	
Turn-Off Delay Time		t _{d(off)}	-	110	120	
Fall Time		t _f	-	100	115	
Reverse Recovery Time	(I _S = -1.7 Adc, dI _S /dt = 100 A/μs)	t _{rr}	-	30	-	ns

BODY-DRAIN DIODE RATINGS

Diode Forward On-Voltage	(I _S = -1.7 Adc, V _{GS} = 0 Vdc)	V _{SD}	-	-0.80	-1.5	Vdc
Diode Forward On-Voltage	(I _S = -3.3 Adc, V _{GS} = 0 Vdc)	V _{SD}	-	-0.90	-	Vdc

3. Indicates Pulse Test: P.W. = 300 μsec max, Duty Cycle = 2%.

4. Class 1 ESD rated – Handling precautions to protect against electrostatic discharge are mandatory.

NTGS3433T1

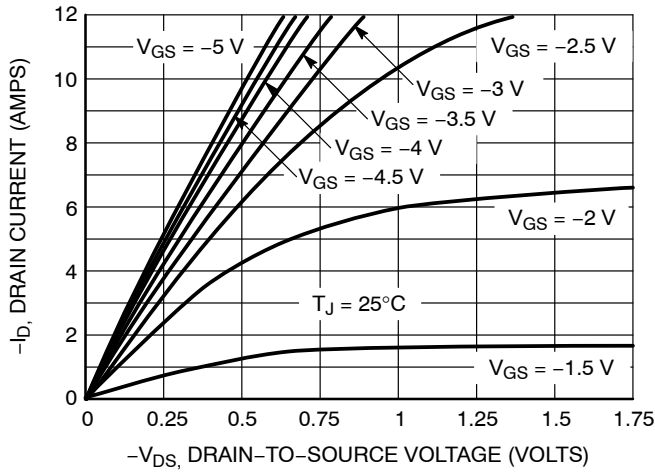


Figure 1. On-Region Characteristics

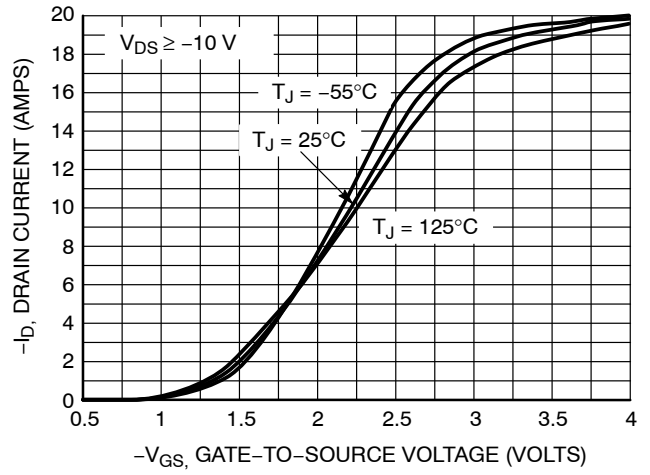


Figure 2. Transfer Characteristics

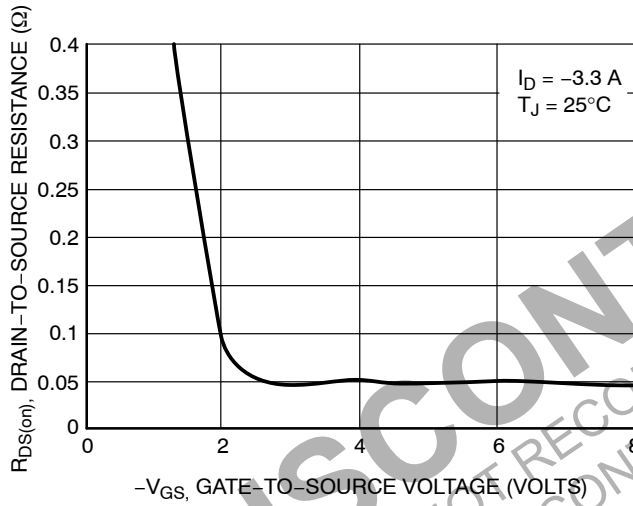


Figure 3. On-Resistance vs. Gate-to-Source Voltage

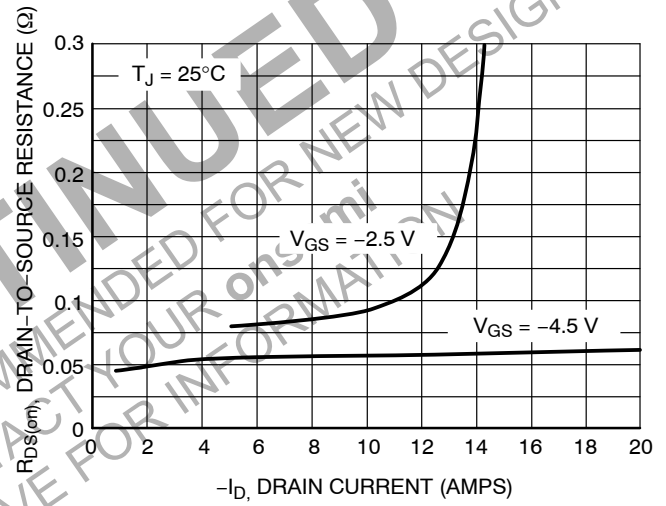


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

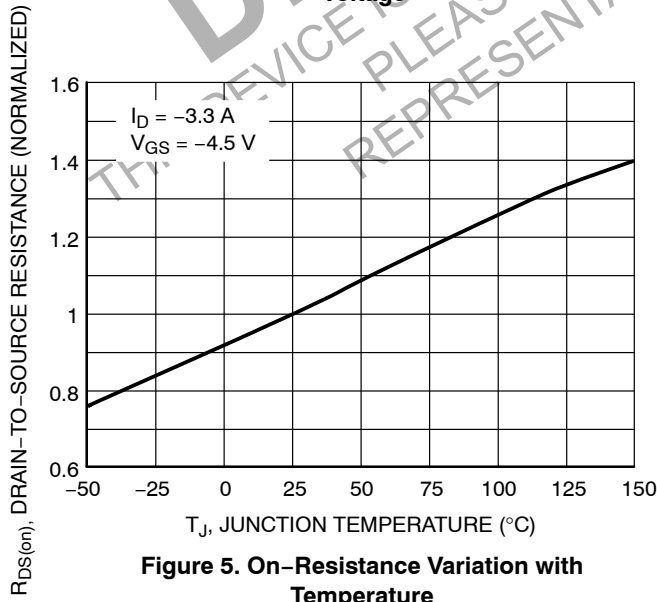


Figure 5. On-Resistance Variation with Temperature

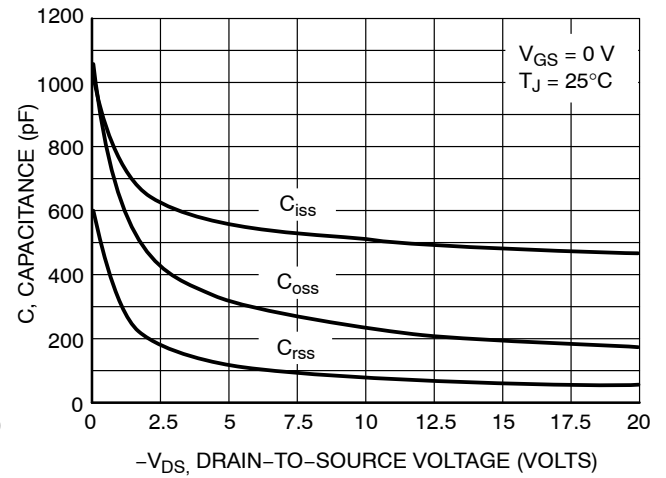


Figure 6. Capacitance Variation

NTGS3433T1

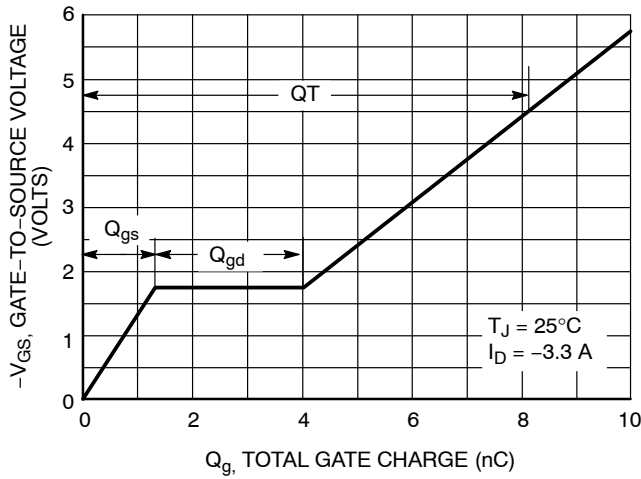


Figure 7. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

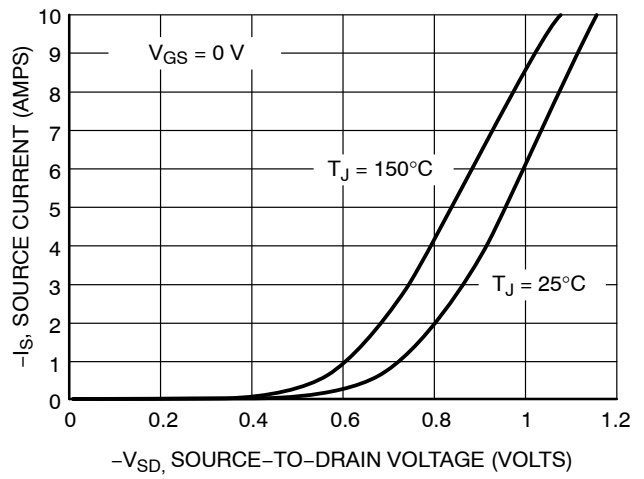


Figure 8. Diode Forward Voltage vs. Current

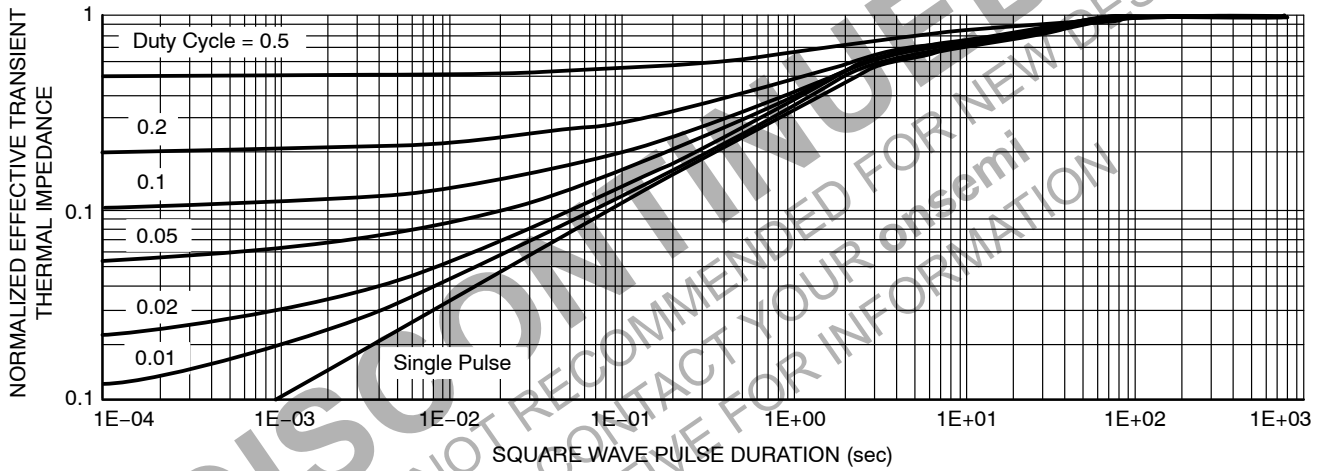


Figure 9. Normalized Thermal Transient Impedance, Junction-to-Ambient

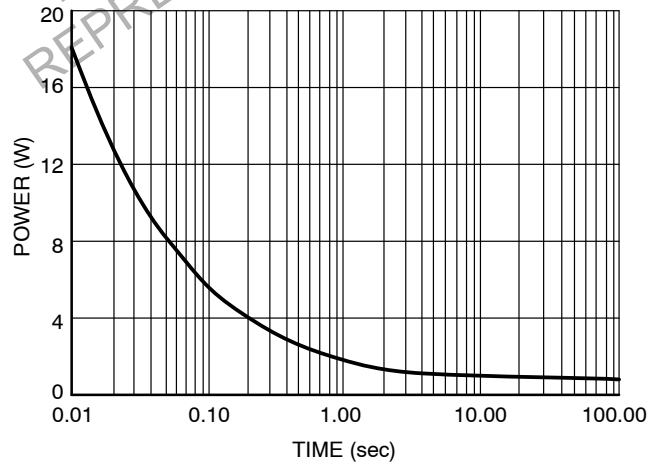
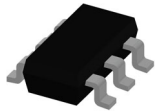


Figure 10. Single Pulse Power

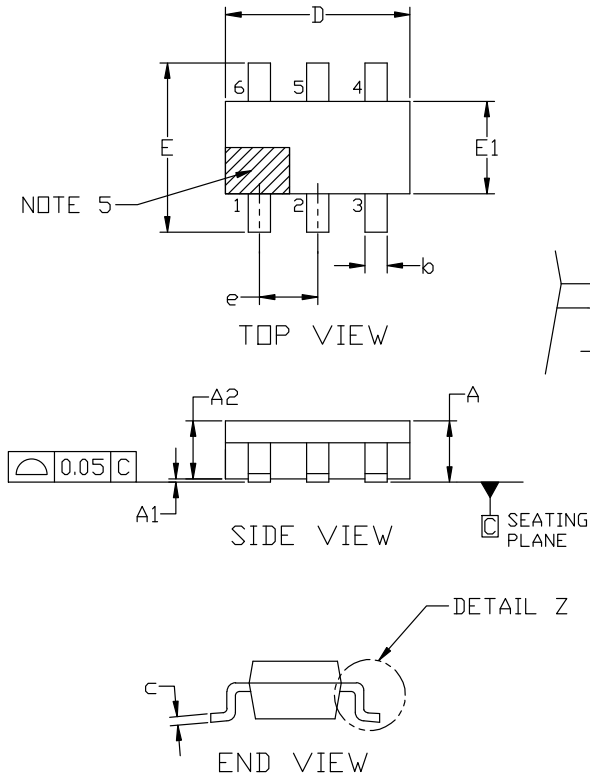


TSOP-6 3.00x1.50x0.90, 0.95P

CASE 318G

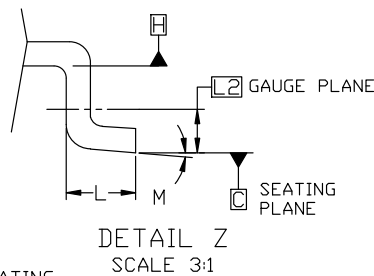
ISSUE W

DATE 26 FEB 2024

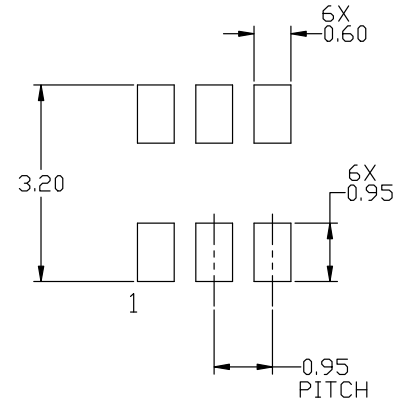


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE



MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

DOCUMENT NUMBER:	98ASB14888C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSOP-6 3.00x1.50x0.90, 0.95P	PAGE 1 OF 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



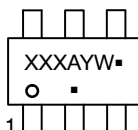
TSOP-6 3.00x1.50x0.90, 0.95P

CASE 318G

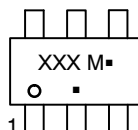
ISSUE W

DATE 26 FEB 2024

GENERIC MARKING DIAGRAM*



IC



STANDARD

XXX = Specific Device Code

A = Assembly Location

Y = Year

W = Work Week

▪ = Pb-Free Package

XXX = Specific Device Code

M = Date Code

▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:

PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:

PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:

PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:

PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:

PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:

PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:

PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:

PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:

PIN 1. D(OUT)+
2. GND
3. D(OUT)-
4. D(IN)-
5. VBUS
6. D(IN)+

STYLE 11:

PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:

PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:

PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 14:

PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:

PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:

PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:

PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

DOCUMENT NUMBER:	98ASB14888C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSOP-6 3.00x1.50x0.90, 0.95P	PAGE 2 OF 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales