

# NTGS1135P

## Power MOSFET

-8 V, -5.8 A, Single P-Channel, TSOP-6

### Features

- Ultra Low  $R_{DS(on)}$
- 1.2 V  $R_{DS(on)}$  Rating
- This is a Pb-Free Device

### Applications

- Load Switch
- Battery Management

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	-8.0	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 6.0$	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	-4.6	A
		$T_A = 85^\circ\text{C}$	-3.3	
	$t \leq 5 \text{ s}$	$T_A = 25^\circ\text{C}$	-5.8	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	0.97	W
	$t \leq 5 \text{ s}$		1.6	
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	$I_{DM}$	-9.2	A
Operating Junction and Storage Temperature	$T_J, T_{STG}$	-55 to 150		$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	-1.0		A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260		$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1 in sq [2 oz] including traces)
2. Surface-mounted on FR4 board using the minimum recommended pad size. (Cu area = 0.0751 in sq)

### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	128	$^\circ\text{C/W}$
Junction-to-Ambient - $t = 5 \text{ s}$ (Note 1)	$R_{\theta JA}$	78	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	188	

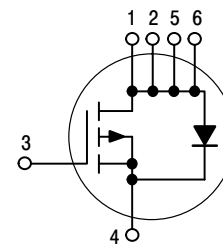


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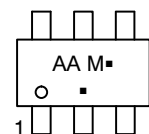
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	$I_D$ MAX
-8 V	31 m $\Omega$ @ -4.5 V	-4.6 A
	38 m $\Omega$ @ -2.5 V	
	57 m $\Omega$ @ -1.8 V	
	300 m $\Omega$ @ -1.2 V	

### P-Channel



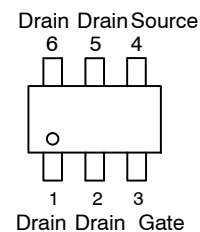
1  
TSOP-6  
CASE 318G  
STYLE 1

### MARKING DIAGRAM



AA = Device Code  
M = Date Code  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

### PIN ASSIGNMENT



### ORDERING INFORMATION

Device	Package	Shipping†
NTGS1135PT1G	TSOP-6 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTGS1135P

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-8.0			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250\ \mu\text{A}$ , Ref to $25^\circ\text{C}$		-8.4		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = -6\text{ V}$			-1.0	$\mu\text{A}$
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 6\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\ \mu\text{A}$	-0.35	-0.57	-0.85	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			2.8		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -4.6\text{ A}$		22	31	m $\Omega$
		$V_{GS} = -2.5\text{ V}, I_D = -2.5\text{ A}$		28	38	
		$V_{GS} = -1.8\text{ V}, I_D = -2.0\text{ A}$		37	57	
		$V_{GS} = -1.5\text{ V}, I_D = -1.0\text{ A}$		47	73	
		$V_{GS} = -1.2\text{ V}, I_D = -0.1\text{ A}$		100	300	
Forward Transconductance	$g_{FS}$	$V_{DS} = -4.0\text{ V}, I_D = -3.0\text{ A}$		1.2		S

### CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = -6.0\text{ V}$		2200		pF
Output Capacitance	$C_{OSS}$			400		
Reverse Transfer Capacitance	$C_{RSS}$			200		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -8.0\text{ V};$ $I_D = -2.5\text{ A}$		21		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.9		
Gate-to-Source Charge	$Q_{GS}$			2.8		
Gate-to-Drain Charge	$Q_{GD}$			3.9		

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -8.0\text{ V},$ $I_D = -2.5\text{ A}, R_G = 6.2\ \Omega$		10		ns
Rise Time	$t_r$			16		
Turn-Off Delay Time	$t_{d(OFF)}$			128		
Fall Time	$t_f$			71		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V},$ $I_S = -1.0\text{ A}$	$T_J = 25^\circ\text{C}$		-0.6	-1.0	V
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = -1.0\text{ A}$			25		ns
Charge Time	$t_a$				11		
Discharge Time	$t_b$				14		
Reverse Recovery Charge	$Q_{RR}$				13		nC

3. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$
4. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

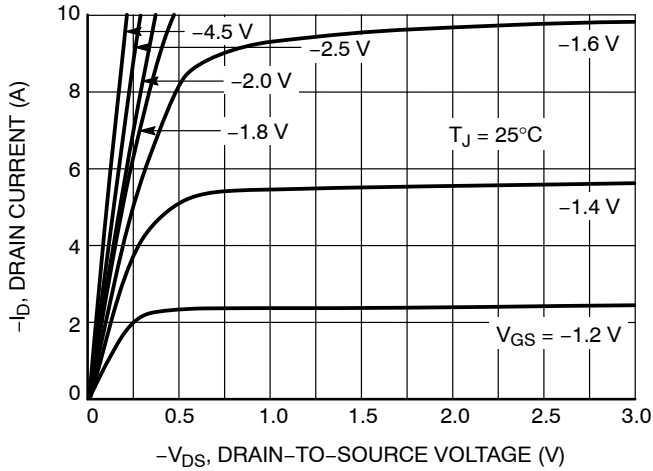


Figure 1. On-Region Characteristics

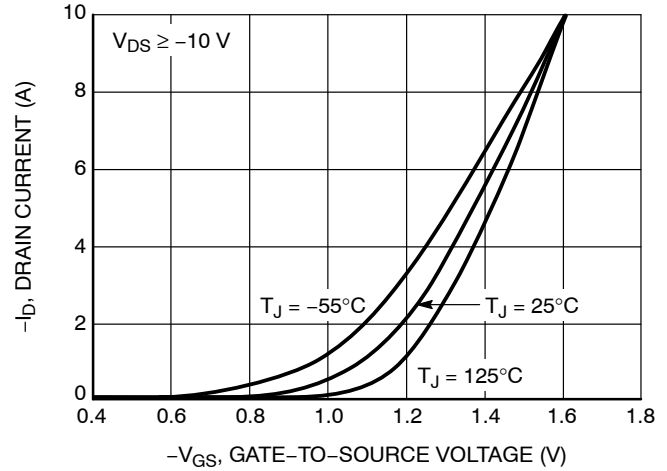


Figure 2. Transfer Characteristics

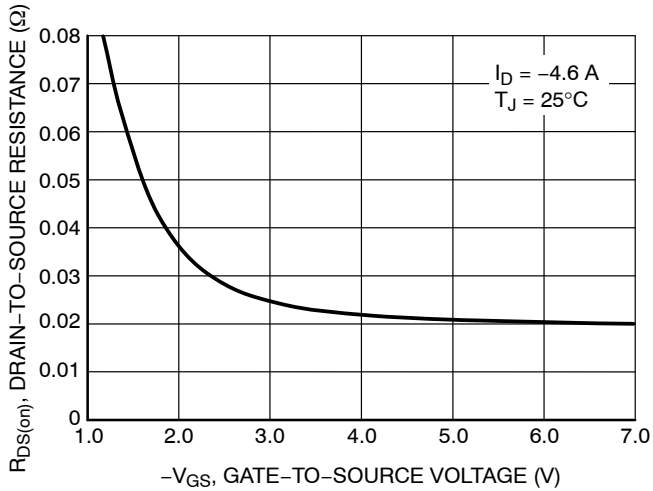


Figure 3. On-Resistance vs. Gate Voltage

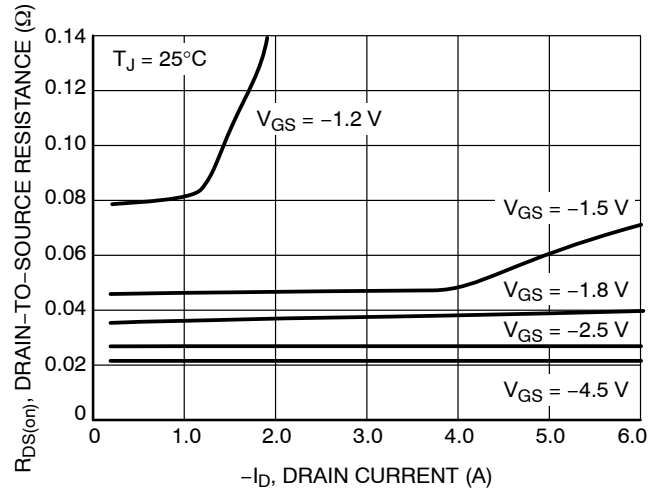


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

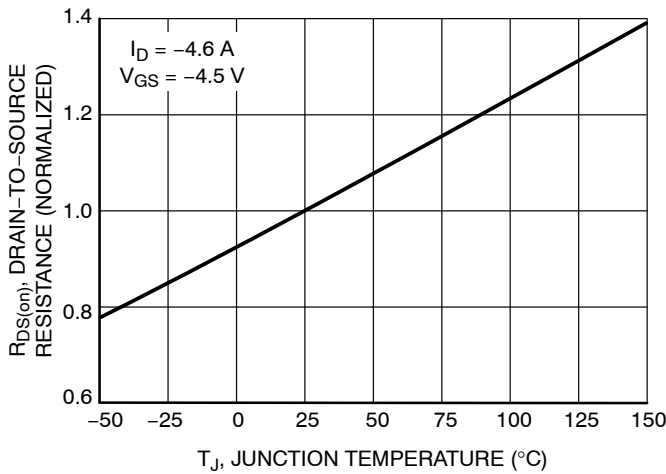


Figure 5. On-Resistance Variation with Temperature

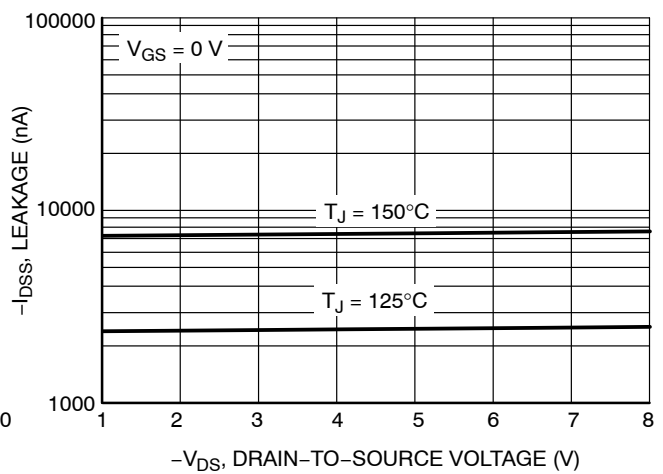


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

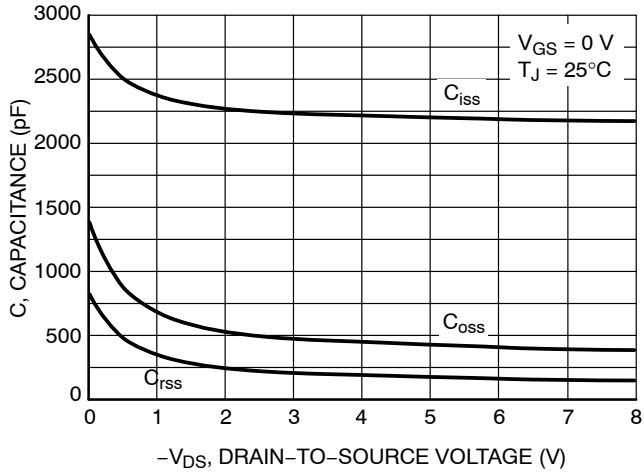


Figure 7. Capacitance Variation

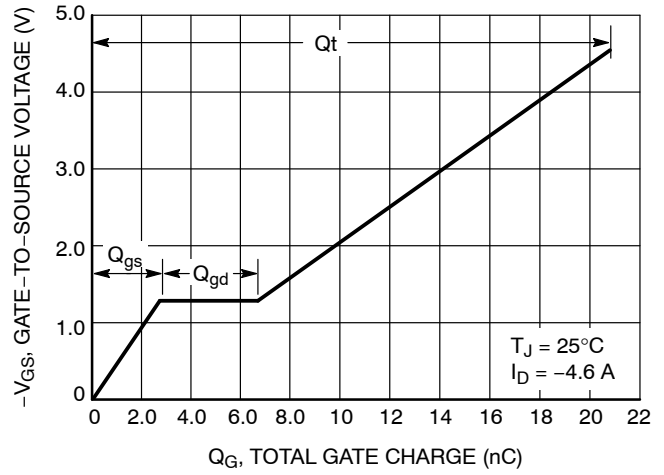


Figure 8. Gate-to-Source Voltage vs. Total Charge

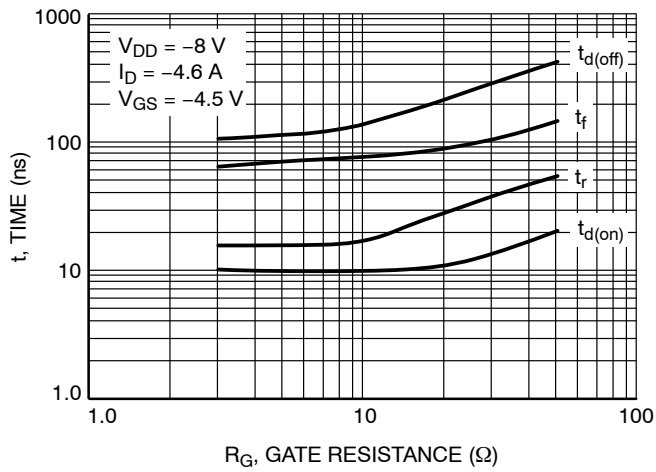


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

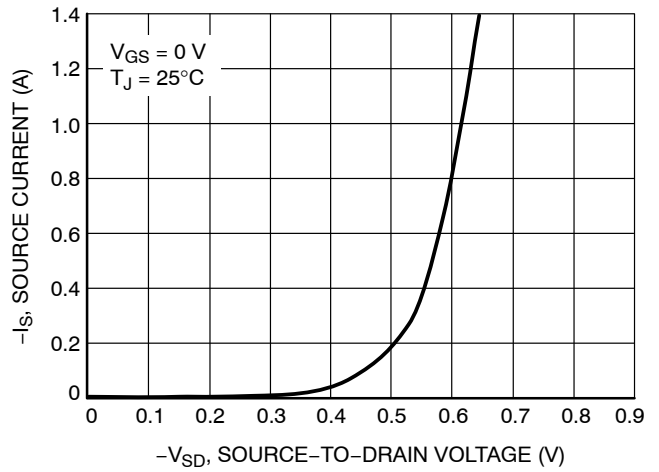
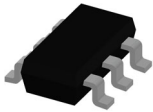


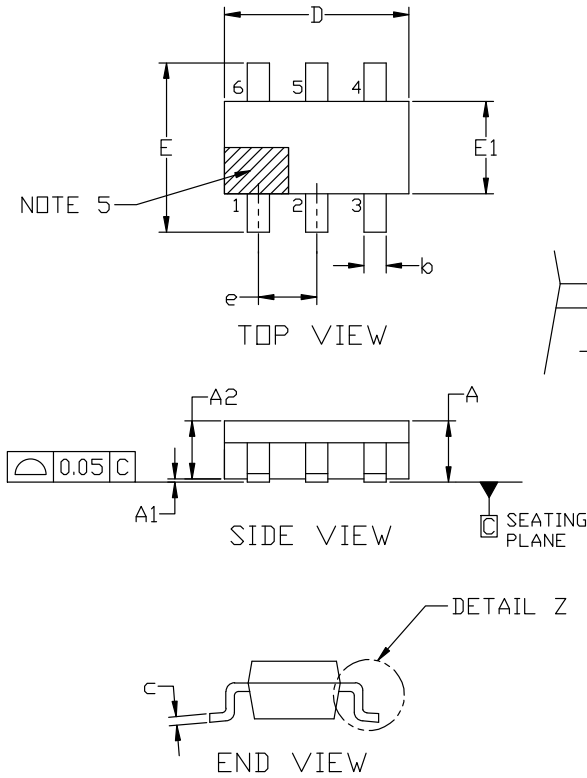
Figure 10. Diode Forward Voltage vs. Current

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**TSOP-6 3.00x1.50x0.90, 0.95P**  
**CASE 318G**  
**ISSUE W**

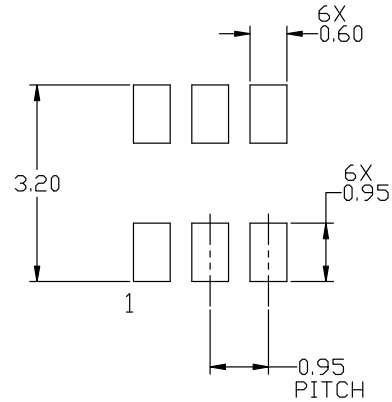
DATE 26 FEB 2024



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



**RECOMMENDED MOUNTING FOOTPRINT**

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

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<b>DESCRIPTION:</b>	<b>TSOP-6 3.00x1.50x0.90, 0.95P</b>	<b>PAGE 1 OF 2</b>

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# MECHANICAL CASE OUTLINE

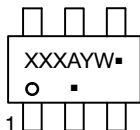
## PACKAGE DIMENSIONS



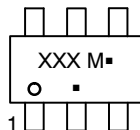
TSOP-6 3.00x1.50x0.90, 0.95P  
CASE 318G  
ISSUE W

DATE 26 FEB 2024

### GENERIC MARKING DIAGRAM\*



IC



STANDARD

XXX = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

- PIN 1. DRAIN
- 2. DRAIN
- 3. GATE
- 4. SOURCE
- 5. DRAIN
- 6. DRAIN

STYLE 2:

- PIN 1. EMITTER 2
- 2. BASE 1
- 3. COLLECTOR 1
- 4. EMITTER 1
- 5. BASE 2
- 6. COLLECTOR 2

STYLE 3:

- PIN 1. ENABLE
- 2. N/C
- 3. R BOOST
- 4. Vz
- 5. V in
- 6. V out

STYLE 4:

- PIN 1. N/C
- 2. V in
- 3. NOT USED
- 4. GROUND
- 5. ENABLE
- 6. LOAD

STYLE 5:

- PIN 1. EMITTER 2
- 2. BASE 2
- 3. COLLECTOR 1
- 4. EMITTER 1
- 5. BASE 1
- 6. COLLECTOR 2

STYLE 6:

- PIN 1. COLLECTOR
- 2. COLLECTOR
- 3. BASE
- 4. EMITTER
- 5. COLLECTOR
- 6. COLLECTOR

STYLE 7:

- PIN 1. COLLECTOR
- 2. COLLECTOR
- 3. BASE
- 4. N/C
- 5. COLLECTOR
- 6. EMITTER

STYLE 8:

- PIN 1. Vbus
- 2. D(in)
- 3. D(in)+
- 4. D(out)+
- 5. D(out)
- 6. GND

STYLE 9:

- PIN 1. LOW VOLTAGE GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN
- 5. DRAIN
- 6. HIGH VOLTAGE GATE

STYLE 10:

- PIN 1. D(OUT)+
- 2. GND
- 3. D(OUT)-
- 4. D(IN)-
- 5. VBUS
- 6. D(IN)+

STYLE 11:

- PIN 1. SOURCE 1
- 2. DRAIN 2
- 3. DRAIN 2
- 4. SOURCE 2
- 5. GATE 1
- 6. DRAIN 1/GATE 2

STYLE 12:

- PIN 1. I/O
- 2. GROUND
- 3. I/O
- 4. I/O
- 5. VCC
- 6. I/O

STYLE 13:

- PIN 1. GATE 1
- 2. SOURCE 2
- 3. GATE 2
- 4. DRAIN 2
- 5. SOURCE 1
- 6. DRAIN 1

STYLE 14:

- PIN 1. ANODE
- 2. SOURCE
- 3. GATE
- 4. CATHODE/DRAIN
- 5. CATHODE/DRAIN
- 6. CATHODE/DRAIN

STYLE 15:

- PIN 1. ANODE
- 2. SOURCE
- 3. GATE
- 4. DRAIN
- 5. N/C
- 6. CATHODE

STYLE 16:

- PIN 1. ANODE/CATHODE
- 2. BASE
- 3. EMITTER
- 4. COLLECTOR
- 5. ANODE
- 6. CATHODE

STYLE 17:

- PIN 1. EMITTER
- 2. BASE
- 3. ANODE/CATHODE
- 4. ANODE
- 5. CATHODE
- 6. COLLECTOR

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