

# MOSFET – Power, N-Channel 100 V, 32 A, 37 mΩ

# NTD6414AN, NVD6414AN

#### **Features**

- Low R<sub>DS(on)</sub>
- High Current Capability
- 100% Avalanche Tested
- NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V <sub>DSS</sub>	100	V
Gate-to-Source Voltage - Continuous			V <sub>GS</sub>	±20	V
Continuous Drain	Steady State			32	Α
Current R <sub>θJC</sub>	State	T <sub>C</sub> = 100°C		22	
Power Dissipation $R_{\theta JC}$	Steady State	T <sub>C</sub> = 25°C	P <sub>D</sub>	100	W
Pulsed Drain Current	t <sub>p</sub>	t <sub>p</sub> = 10 μs		117	Α
Operating and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Source Current (Body Diode)			Is	32	Α
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD}$ = 50 Vdc, $V_{GS}$ = 10 Vdc, $I_{L(pk)}$ = 32 A, L = 0.3 mH, $R_{G}$ = 25 $\Omega$ )			E <sub>AS</sub>	154	mJ
Lead Temperature for Purposes, 1/8" from C		Seconds	TL	260	°C

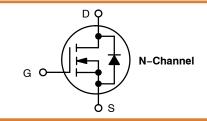
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) Steady State	$R_{\theta JC}$	1.5	°C/W
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	37	

Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [1 oz] including traces).

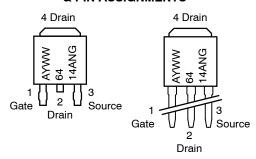
V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> MAX	I <sub>D</sub> MAX (Note 1)
100 V	37 mΩ @ 10 V	32 A







# MARKING DIAGRAM & PIN ASSIGNMENTS



A = Assembly Location\* Y = Year

Y = Year

WW = Work Week

6414AN = Device Code

G = Pb-Free Package

\* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

#### **ORDERING INFORMATION**

See detailed ordering and shipping information on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

## **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise noted)

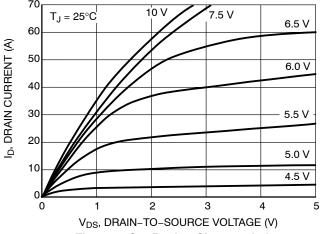
Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	-				•	-	-
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>				107		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	Vcs = 0 V.	T <sub>J</sub> = 25°C			1.0	μΑ
		$V_{GS} = 0 V$ , $V_{DS} = 100 V$	T <sub>J</sub> = 125°C			100	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> =	±20 V			±100	nA
ON CHARACTERISTICS (Note 3)	•		•		•	•	•
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D = 1$	250 μΑ	2.0		4.0	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>				8.3		mV/°C
Drain-to-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> =	= 32 A		30	37	mΩ
Forward Transconductance	gFS	V <sub>GS</sub> = 5.0 V, I <sub>D</sub> = 10 A			18		S
CHARGES, CAPACITANCES AND GA	TE RESISTANO	CE	•			•	•
Input Capacitance	C <sub>ISS</sub>				1450		pF
Output Capacitance	C <sub>OSS</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 25 V			230		
Reverse Transfer Capacitance	C <sub>RSS</sub>				95		
Total Gate Charge	Q <sub>G(TOT)</sub>				40		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>		•		1.7		
Gate-to-Source Charge	$Q_{GS}$	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 80	V, I <sub>D</sub> = 32 A		8.0		
Gate-to-Drain Charge	$Q_{GD}$		•		20		
Plateau Voltage	$V_{GP}$		•		5.9		V
Gate Resistance	$R_{G}$				1.9		Ω
SWITCHING CHARACTERISTICS (Not	e 4)		-				-
Turn-On Delay Time	t <sub>d(on)</sub>				11		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V, V <sub>DD</sub>	= 80 V,		52		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D = 32 \text{ A}, R_G =$	6.1 Ω΄		38		
Fall Time	t <sub>f</sub>		•		48		
DRAIN-SOURCE DIODE CHARACTER	RISTICS					•	•
Forward Diode Voltage	$V_{SD}$	., .,,,	T <sub>J</sub> = 25°C		0.87	1.2	V
		$V_{GS} = 0 \text{ V}, I_S = 32 \text{ A}$	T <sub>J</sub> = 125°C		0.76		
Reverse Recovery Time	t <sub>RR</sub>		•		68		ns
Charge Time	Ta	$V_{GS} = 0 \text{ V, } dI_{S}/dt =$	100 A/μs.		51		
Discharge Time	T <sub>b</sub>	I <sub>S</sub> = 32 A			16		1
Reverse Recovery Charge	Q <sub>RR</sub>		ľ		195		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

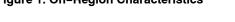
Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

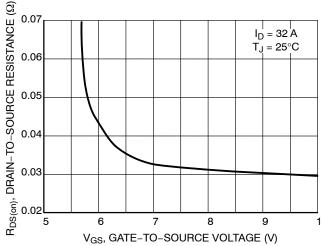
#### **TYPICAL CHARACTERISTICS**



70 V<sub>DS</sub> ≥ 10 V 60 ID, DRAIN CURRENT (A) 50 40 30 20 = 25°C 125°C 10 -55°Ċ 0 2 5 8 V<sub>GS</sub>, GATE-TO-SOURCE VOLTAGE (V) Figure 2. Transfer Characteristics

Figure 1. On-Region Characteristics

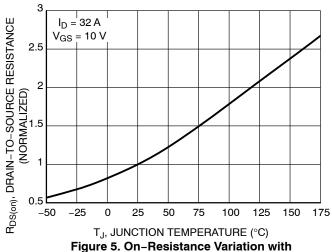




 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})},\,\mathsf{DRAIN-TO-SOURCE}\;\mathsf{RESISTANCE}\;(\Omega)$ 0.10  $V_{GS} = 10^{1} V$ Γ<sub>J</sub> = 175°C 0.08 Т<sub>Ј</sub> = 125°С 0.06 0.04  $T_J = 25^{\circ}C$ 0.02  $T_{.1} = -55^{\circ}C$ 10 15 20 25 30 35 I<sub>D</sub>, DRAIN CURRENT (A)

Figure 3. On-Region versus Gate Voltage

Figure 4. On-Resistance versus Drain Current and Gate Voltage



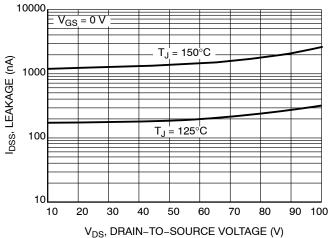
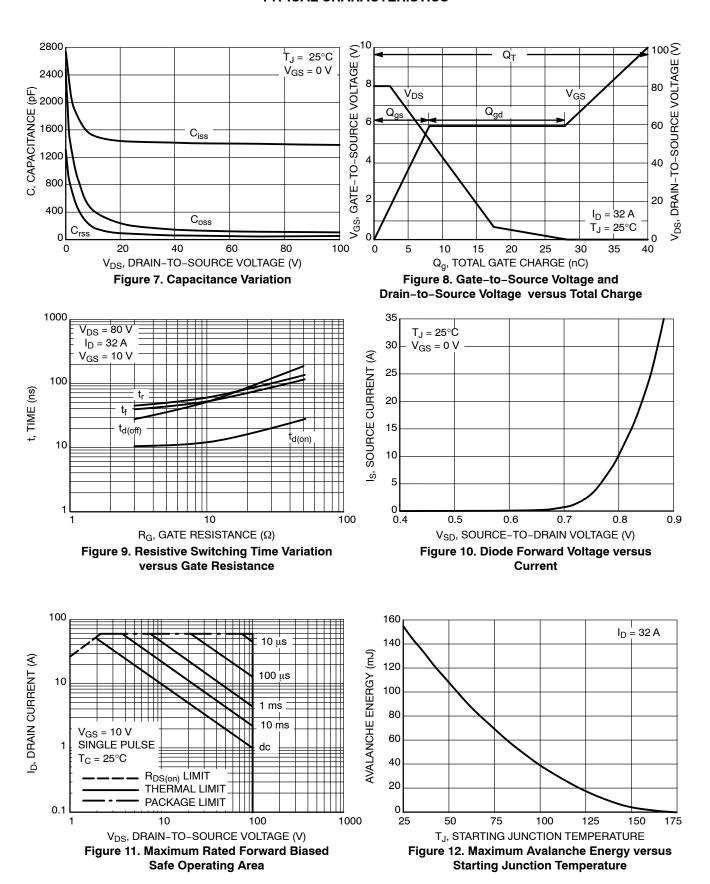


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current versus Voltage

#### **TYPICAL CHARACTERISTICS**



#### **TYPICAL CHARACTERISTICS**

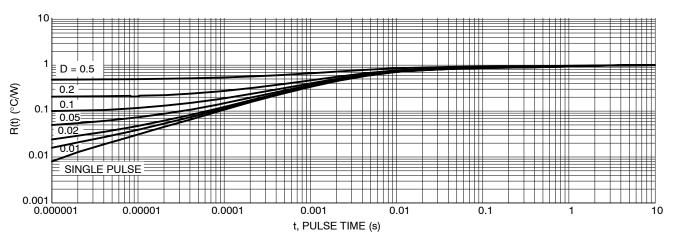


Figure 13. Thermal Response

#### **ORDERING INFORMATION**

Device	Package	Shipping†
NTD6414ANT4G	DPAK (Pb-Free)	2500 / Tape & Reel

#### **DISCONTINUED** (Note 5)

NTD6414AN-1G	IPAK (Pb-Free)	75 Units / Rail
NVD6414ANT4G*	DPAK (Pb-Free)	2500 / Tape & Reel

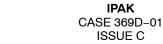
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

<sup>\*</sup>NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

<sup>5.</sup> **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on <a href="https://www.onsemi.com">www.onsemi.com</a>.

# MECHANICAL CASE OUTLINE





STYLE 3: PIN 1. ANODE

2. CATHODE

4. CATHODE

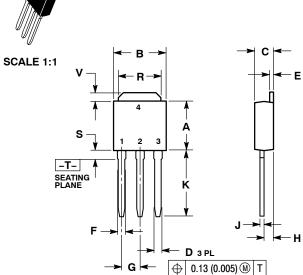
3 ANODE

STYLE 7: PIN 1. GATE 2. COLLECTOR

3. EMITTER

COLLECTOR

**DATE 15 DEC 2010** 



STYLE 2:

PIN 1. GATE

3

STYLE 6: PIN 1. MT1 2. MT2 3. GATE

2. DRAIN

4. DRAIN

MT2

SOURCE

STYLE 1: PIN 1. BASE

3

STYLE 5: PIN 1. GATE

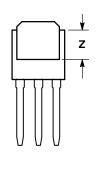
2. ANODE 3. CATHODE

ANODE

2. COLLECTOR

**EMITTER** 

COLLECTOR



#### NOTES:

- DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.245	5.97	6.35
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29 BSC	
Н	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
٧	0.035	0.050	0.89	1.27
Z	0.155		3.93	

#### MARKING DIAGRAMS

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE
Discrete

XXXXX

ALYWW

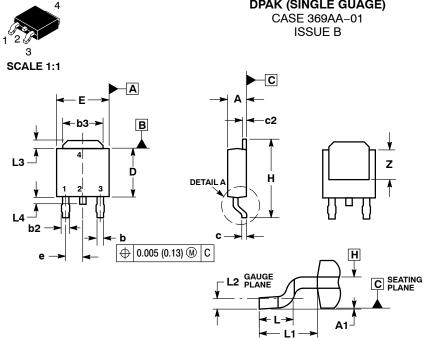
XXXXXXXX

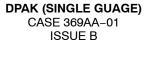
X

xxxxxxxxx = Device Code
A = Assembly Location
IL = Wafer Lot
Y = Year
WW = Work Week

	IPAK (DPAK INSERTION MOUNT)		
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**DETAIL A** ROTATED 90° CW **DATE 03 JUN 2010** 

#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: INCHES.
  3. THERMAL PAD CONTOUR OPTIONAL WITHIN DI-MENSIONS b3, L3 and Z.
  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD
- FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

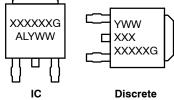
	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
С	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
е	0.090	BSC	2.29	BSC
Н	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108	REF	2.74	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4		0.040		1.01
Z	0.155		3.93	

**GENERIC** 

MARKING DIAGRAM\*

#### STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE STYLE 1: PIN 1. BASE STYLE 2: PIN 1. GATE STYLE 3: PIN 1. ANODE 2. COLLECTOR 3. EMITTER 2. CATHODE 3. ANODE 2. DRAIN 3. SOURCE 4. COLLECTOR 4. DRAIN CATHODE STYLE 5: STYLE 6: STYLE 7: PIN 1. GATE 2. ANODE 3. CATHODE PIN 1. GATE 2. COLLECTOR PIN 1. MT1 2. MT2 3. GATE 3. EMITTER 4. ANODE COLLECTOR

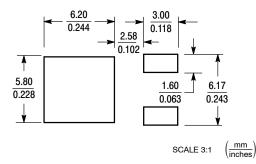
# XXXXXXG



XXXXXX = Device Code Α = Assembly Location L = Wafer Lot ٧ = Year = Work Week WW = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

#### **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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