

# NTB65N02R, NTP65N02R

## Power MOSFET 65 A, 24 V N-Channel TO-220, D<sup>2</sup>PAK

### Features

- Planar HD3e Process for Fast Switching Performance
- Low  $R_{DS(on)}$  to Minimize Conduction Loss
- Low  $C_{iss}$  to Minimize Driver Loss
- Low Gate Charge
- Pb-Free Packages are Available\*

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ Unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DS}$	25	$V_{dc}$
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 20$	$V_{dc}$
Thermal Resistance – Junction-to-Case	$R_{\theta JC}$	2.0	$^\circ\text{C}/\text{W}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	$P_D$	62.5	W
Drain Current –			
Continuous @ $T_C = 25^\circ\text{C}$ , Chip	$I_D$	65	A
Continuous @ $T_C = 25^\circ\text{C}$ , Limited by Package	$I_D$	58	A
Single Pulse ( $t_p = 10 \mu\text{s}$ )	$I_{DM}$	160	A
Thermal Resistance –			
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	67	$^\circ\text{C}/\text{W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	1.86	W
Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	$I_D$	10	A
Thermal Resistance –			
Junction-to-Ambient (Note 2)	$R_{\theta JA}$	120	$^\circ\text{C}/\text{W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	1.04	W
Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	$I_D$	7.6	A
Operating and Storage Temperature Range	$T_J$ and $T_{stg}$	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 50 V_{dc}$ , $V_{GS} = 10 V_{dc}$ , $I_L = 11 A_{pk}$ , $L = 1 \text{ mH}$ , $R_G = 25 \Omega$ )	$E_{AS}$	60	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds	$T_L$	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using 1 in. pad size, (Cu Area 1.127 in<sup>2</sup>).
2. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in<sup>2</sup>).

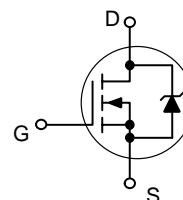
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



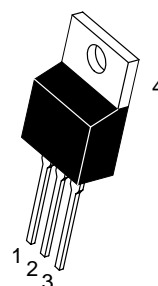
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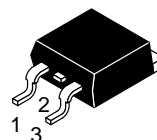
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
24 V	8.4 m $\Omega$ @ 10 V	65 A



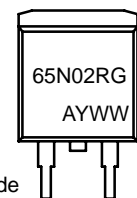
### MARKING DIAGRAMS



TO-220AB  
CASE 221A  
STYLE 5



D<sup>2</sup>PAK  
CASE 418AA  
STYLE 2



65N02R = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb-Free Package

### PIN ASSIGNMENT

PIN	FUNCTION
1	Gate
2	Drain
3	Source
4	Drain

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NTB65N02R, NTP65N02R

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C Unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain-to-Source Breakdown Voltage (Note 3) (V <sub>GS</sub> = 0 V <sub>dc</sub> , I <sub>D</sub> = 250 μA <sub>dc</sub> ) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	24 -	27.5 25.5	- -	V <sub>dc</sub> mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 20 V <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> ) (V <sub>DS</sub> = 20 V <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> , T <sub>J</sub> = 150°C)	I <sub>DSS</sub>	- -	- -	1.5 10	μA <sub>dc</sub>
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 V <sub>dc</sub> , V <sub>DS</sub> = 0 V <sub>dc</sub> )	I <sub>GSS</sub>	-	-	±100	nA <sub>dc</sub>

## ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA <sub>dc</sub> ) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	1.0 -	1.5 4.1	2.0 -	V <sub>dc</sub> mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V <sub>GS</sub> = 4.5 V <sub>dc</sub> , I <sub>D</sub> = 15 A <sub>dc</sub> ) (V <sub>GS</sub> = 10 V <sub>dc</sub> , I <sub>D</sub> = 20 A <sub>dc</sub> ) (V <sub>GS</sub> = 10 V <sub>dc</sub> , I <sub>D</sub> = 30 A <sub>dc</sub> )	R <sub>DS(on)</sub>	- - -	11.2 8.4 8.2	12.5 10.5 -	mΩ
Forward Transconductance (Note 3) (V <sub>DS</sub> = 10 V <sub>dc</sub> , I <sub>D</sub> = 15 A <sub>dc</sub> )	g <sub>FS</sub>	-	27	-	Mhos

## DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 20 V <sub>dc</sub> , V <sub>GS</sub> = 0 V, f = 1 MHz)	C <sub>ISS</sub>	-	948	1330	pF
Output Capacitance		C <sub>OSS</sub>	-	456	640	
Transfer Capacitance		C <sub>rSS</sub>	-	160	225	

## SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V <sub>GS</sub> = 10 V <sub>dc</sub> , V <sub>DD</sub> = 10 V <sub>dc</sub> , I <sub>D</sub> = 30 A <sub>dc</sub> , R <sub>G</sub> = 3 Ω)	t <sub>d(on)</sub>	-	7.0	-	ns
Rise Time		t <sub>r</sub>	-	53	-	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	14	-	
Fall Time		t <sub>f</sub>	-	10	-	
Gate Charge	(V <sub>GS</sub> = 4.5 V <sub>dc</sub> , I <sub>D</sub> = 30 A <sub>dc</sub> , V <sub>DS</sub> = 10 V <sub>dc</sub> ) (Note 3)	Q <sub>T</sub>	-	9.5	-	nC
		Q <sub>1</sub>	-	3.0	-	
		Q <sub>2</sub>	-	4.4	-	

## SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I <sub>S</sub> = 20 A <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> ) (Note 3) (I <sub>S</sub> = 30 A <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> ) (I <sub>S</sub> = 15 A <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> , T <sub>J</sub> = 125°C)	V <sub>SD</sub>	- - -	0.88 1.10 0.80	1.2 - -	V <sub>dc</sub>
Reverse Recovery Time	(I <sub>S</sub> = 30 A <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> , dI <sub>S</sub> /dt = 100 A/μs) (Note 3)	t <sub>rr</sub>	-	29.1	-	ns
		t <sub>a</sub>	-	13.6	-	
		t <sub>b</sub>	-	15.5	-	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	-	0.02	-	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

# NTB65N02R, NTP65N02R

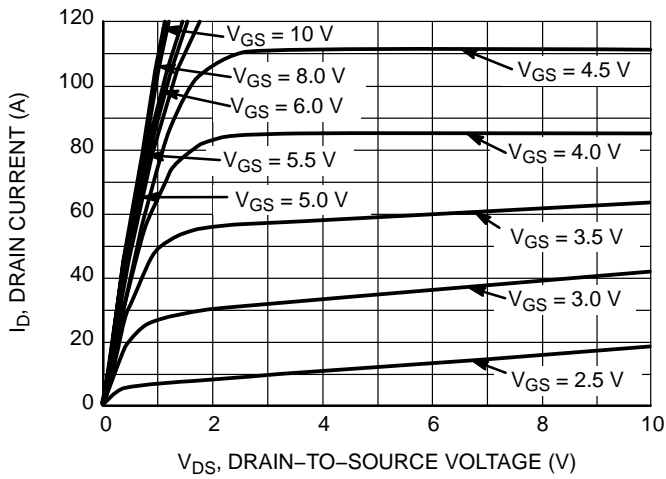


Figure 1. On-Region Characteristics

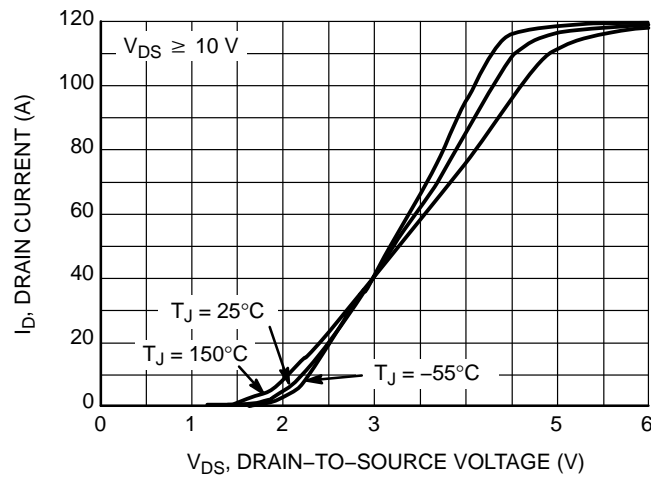


Figure 2. Transfer Characteristics

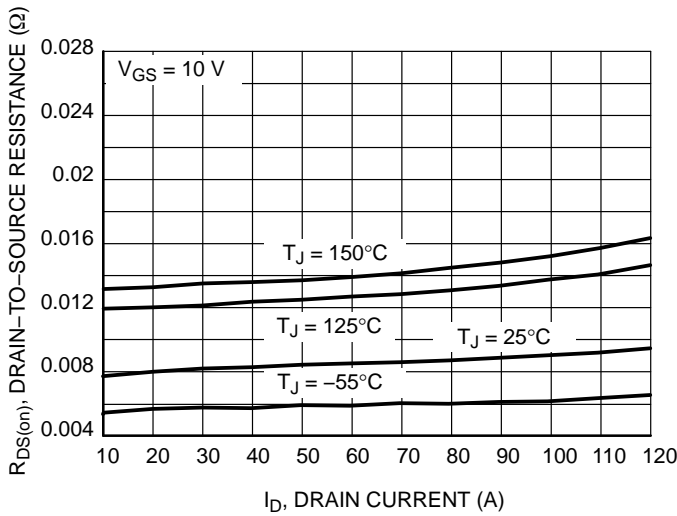


Figure 3. On-Resistance versus Drain Current and Temperature

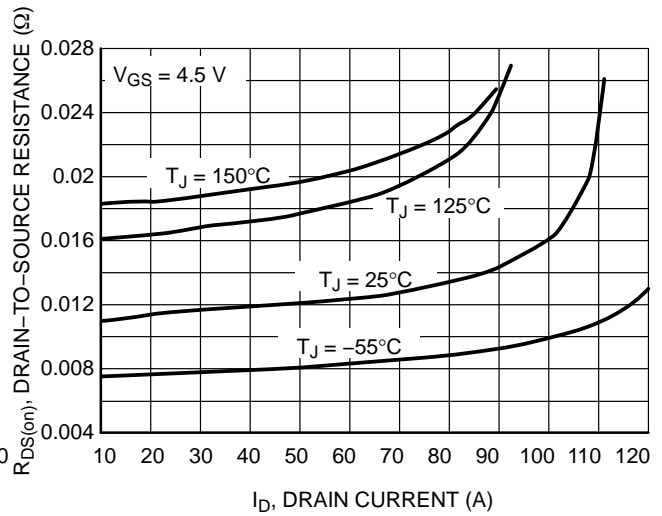


Figure 4. On-Resistance versus Drain Current and Temperature

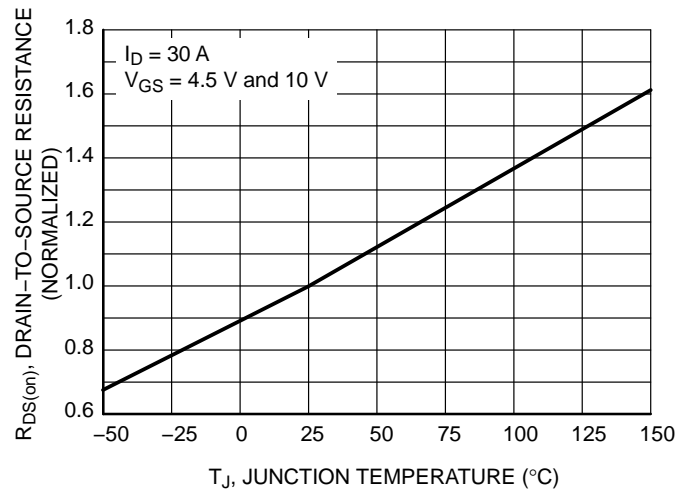


Figure 5. On-Resistance Variation with Temperature

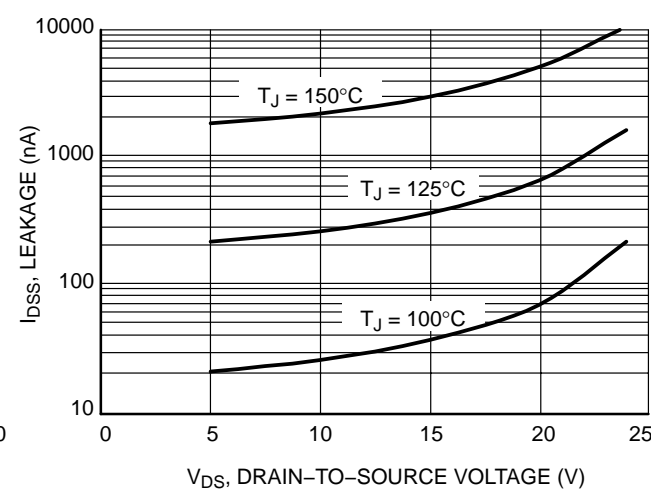


Figure 6. Drain-to-Source Leakage Current versus Voltage

# NTB65N02R, NTP65N02R

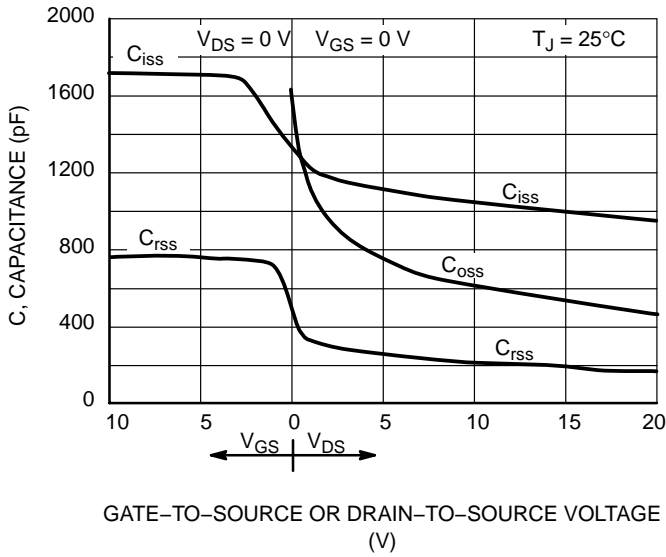


Figure 7. Capacitance Variation

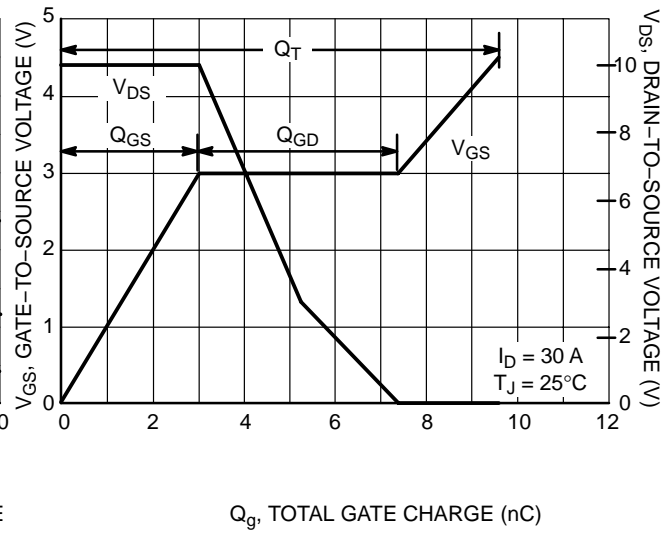


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

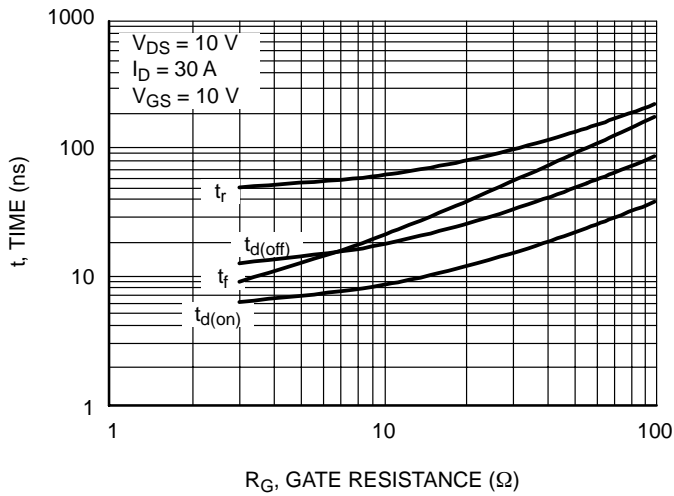


Figure 9. Resistive Switching Time Variation versus Gate Resistance

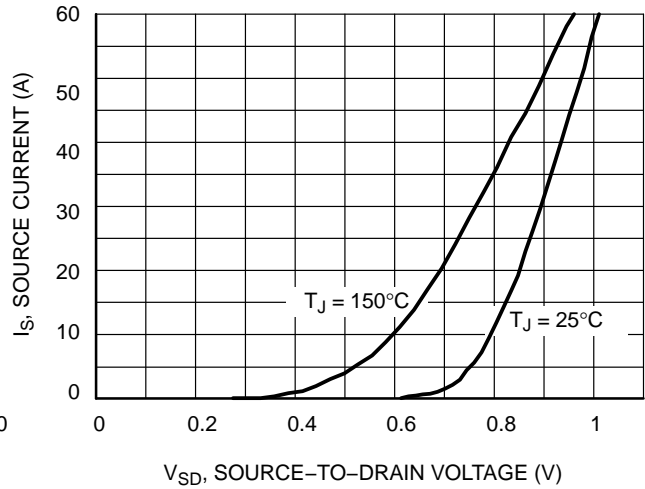


Figure 10. Diode Forward Voltage versus Current

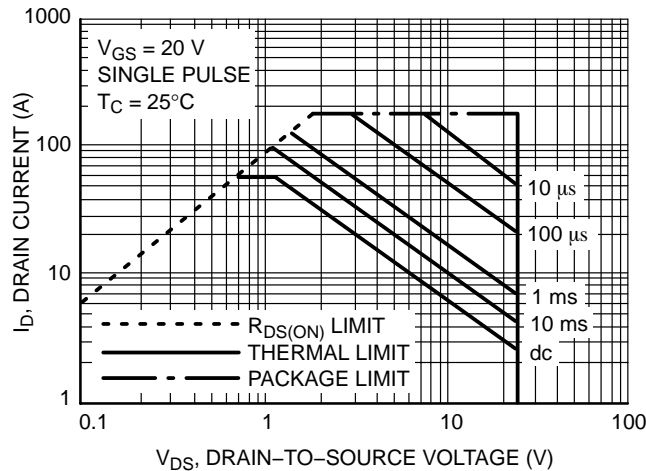
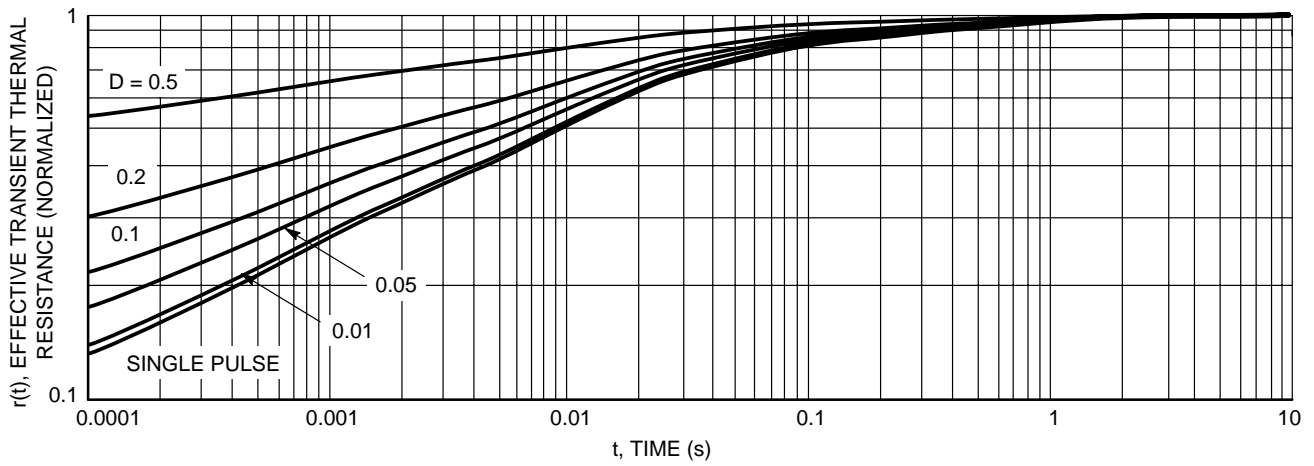


Figure 11. Maximum Rated Forward Biased Safe Operating Area

## NTB65N02R, NTP65N02R



**Figure 12. Thermal Response**

### ORDERING INFORMATION

Device	Package	Shipping†
NTB65N02R	D <sup>2</sup> PAK	50 Units / Rail
NTB65N02RG	D <sup>2</sup> PAK (Pb-Free)	50 Units / Rail
NTB65N02RT4	D <sup>2</sup> PAK	800 / Tape & Reel
NTB65N02RT4G	D <sup>2</sup> PAK (Pb-Free)	800 / Tape & Reel
NTP65N02R	TO-220AB	50 Units / Rail
NTP65N02RG	TO-220AB (Pb-Free)	50 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

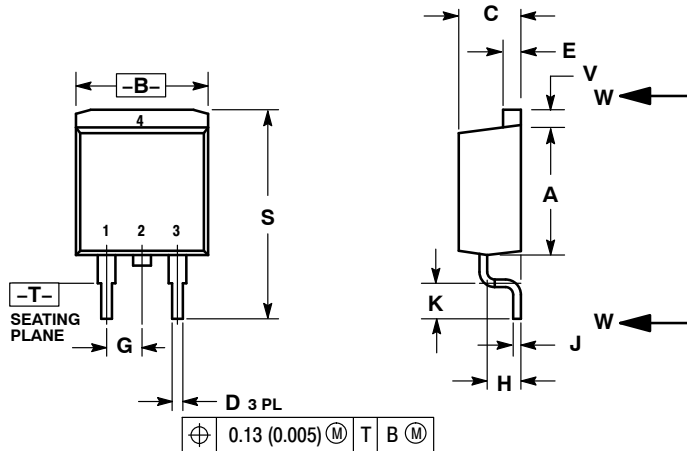
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**D<sup>2</sup>PAK 3**  
CASE 418B-04  
ISSUE L

DATE 17 FEB 2015

SCALE 1:1

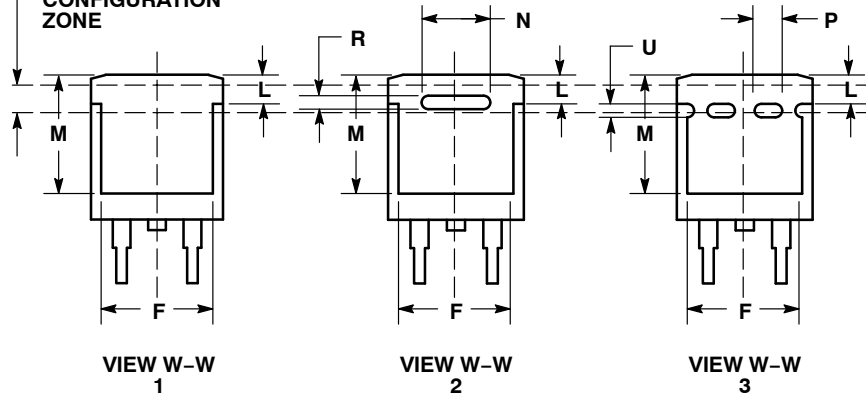


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197	REF	5.00	REF
P	0.079	REF	2.00	REF
R	0.039	REF	0.99	REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

**VARIABLE CONFIGURATION ZONE**



- |  |   |   |  |   |  |
|--|---|---|--|---|--|
| <b>STYLE 1:</b><br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 2:</b><br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN | <b>STYLE 3:</b><br>PIN 1. ANODE<br>2. CATHODE<br>3. ANODE<br>4. CATHODE | <b>STYLE 4:</b><br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 5:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE<br>4. ANODE | <b>STYLE 6:</b><br>PIN 1. NO CONNECT<br>2. CATHODE<br>3. ANODE<br>4. CATHODE |
|--|---|---|--|---|--|

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**D<sup>2</sup>PAK 3**  
CASE 418B-04  
ISSUE L

DATE 17 FEB 2015

**GENERIC  
MARKING DIAGRAM\***



- xx = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package
- AKA = Polarity Indicator

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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