

NSTB1005DXV5T1G

Dual Common Base-Collector Bias Resistor Transistors

NPN and PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. The NSTB1005DXV5T1 contains two complementary BRT devices are housed in the SOT-553 package which is ideal for low power surface mount applications where board space is at a premium.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7 inch Tape and Reel
- This is a Pb-Free Device

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted, common for Q_1 and Q_2 , – minus sign for Q_1 (PNP) omitted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

THERMAL CHARACTERISTICS

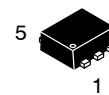
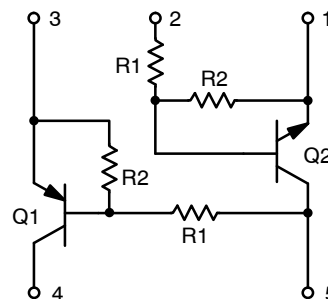
Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 1) Derate above 25°C (Note 1)	P_D	357 2.9	mW mW/ $^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient (Note 1)	$R_{\theta JA}$	350	$^\circ\text{C}/\text{W}$
Characteristic (Both Junctions Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 1) Derate above 25°C (Note 1)	P_D	500 4.0	mW mW/ $^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient (Note 1)	$R_{\theta JA}$	250	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

1. FR-4 @ Minimum Pad



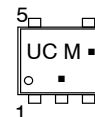
ON Semiconductor®

<http://onsemi.com>



SOT-553
CASE 463B

MARKING DIAGRAM



UC = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NSTB1005DXV5T1G	SOT-553 (Pb-Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NSTB1005DXV5T1G

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Q1 TRANSISTOR: PNP – OFF CHARACTERISTICS					
Collector–Base Cutoff Current (V _{CB} = 50 V, I _E = 0)	I _{CBO}	–	–	100	nAdc
Collector–Emitter Cutoff Current (V _{CE} = 50 V, I _B = 0)	I _{CEO}	–	–	500	nAdc
Emitter–Base Cutoff Current (V _{EB} = 6.0 V, I _C = 0)	I _{EBO}	–	–	0.1	mAdc
Collector–Base Breakdown Voltage (I _C = 10 μA, I _E = 0)	V _{(BR)CBO}	50	–	–	Vdc
Collector–Emitter Breakdown Voltage (I _C = 2.0 mA, I _B = 0)	V _{(BR)CEO}	50	–	–	Vdc

ON CHARACTERISTICS

DC Current Gain	h _{FE}	80	140	–	
Collector–Emitter Saturation Voltage (I _C = 10 mA, I _E = 0.3 mA)	V _{CE(sat)}	–	–	0.25	Vdc
Output Voltage (on) (V _{CC} = 5.0 V, V _B = 3.5 V, R _L = 1.0 kΩ)	V _{OL}	–	–	0.2	Vdc
Output Voltage (off) (V _{CC} = 5.0 V, V _B = 0.5 V, R _L = 1.0 kΩ)	V _{OH}	4.9	–	–	Vdc
Input Resistor	R1	32.9	47	61.1	kΩ
Resistor Ratio	R ₁ /R ₂	0.8	1.0	1.2	

Q2 TRANSISTOR: NPN – OFF CHARACTERISTICS

Collector–Base Cutoff Current (V _{CB} = 50 V, I _E = 0)	I _{CBO}	–	–	100	nAdc
Collector–Emitter Cutoff Current (V _{CB} = 50 V, I _B = 0)	I _{CEO}	–	–	500	nAdc
Emitter–Base Cutoff Current (V _{EB} = 6.0, I _C = 0)	I _{EBO}	–	–	0.1	mAdc

ON CHARACTERISTICS

Collector–Base Breakdown Voltage (I _C = 10 μA, I _E = 0)	V _{(BR)CBO}	50	–	–	Vdc
Collector–Emitter Breakdown Voltage (I _C = 2.0 mA, I _B = 0)	V _{(BR)CEO}	50	–	–	Vdc
DC Current Gain (V _{CE} = 10 V, I _C = 5.0 mA)	h _{FE}	80	140	–	
Collector–Emitter Saturation Voltage (I _C = 10 mA, I _B = 0.3 mA)	V _{CE(SAT)}	–	–	0.25	Vdc
Output Voltage (on) (V _{CC} = 5.0 V, V _B = 2.5 V, R _L = 1.0 kΩ)	V _{OL}	–	–	0.2	Vdc
Output Voltage (off) (V _{CC} = 5.0 V, V _B = 0.5 V, R _L = 1.0 kΩ)	V _{OH}	4.9	–	–	Vdc
Input Resistor	R1	33	47	61	kΩ
Resistor Ratio	R1/R2	0.8	1.0	1.2	

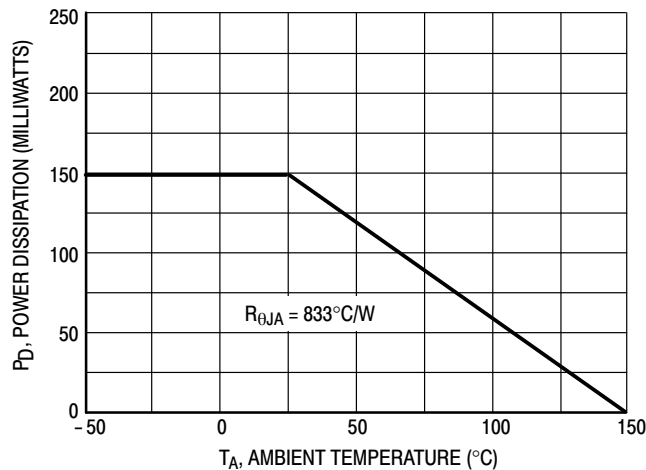


Figure 1. Derating Curve

NSTB1005DXV5T1G

TYPICAL ELECTRICAL CHARACTERISTICS – PNP TRANSISTOR

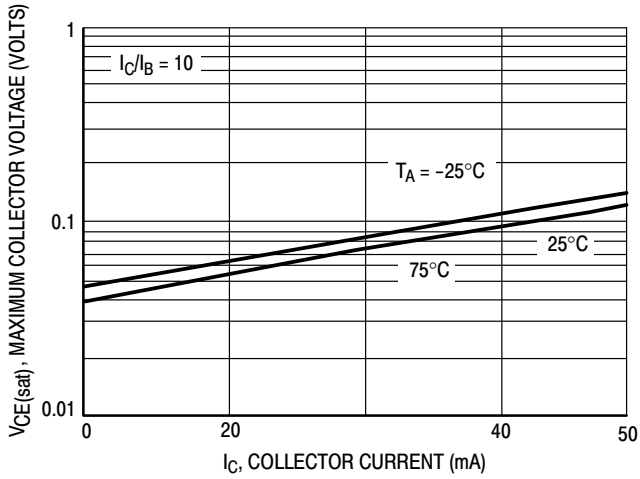


Figure 2. $V_{CE(sat)}$ versus I_C

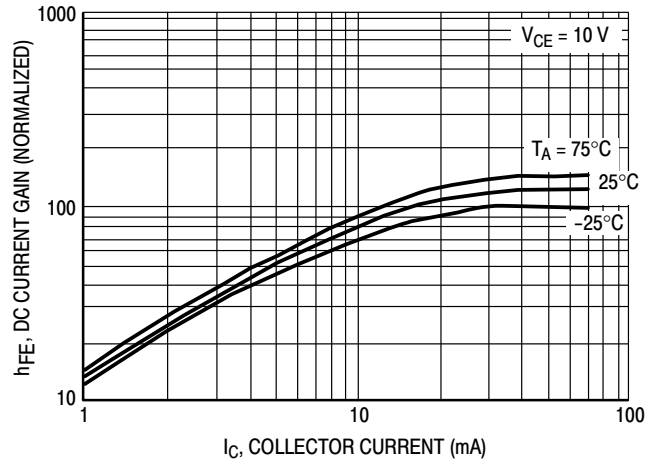


Figure 3. DC Current Gain

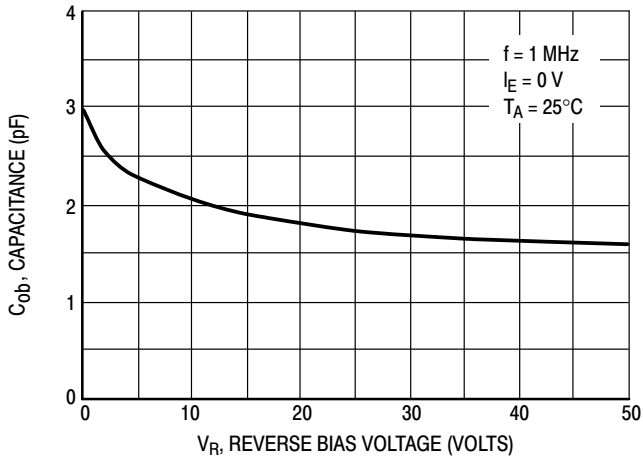


Figure 4. Output Capacitance

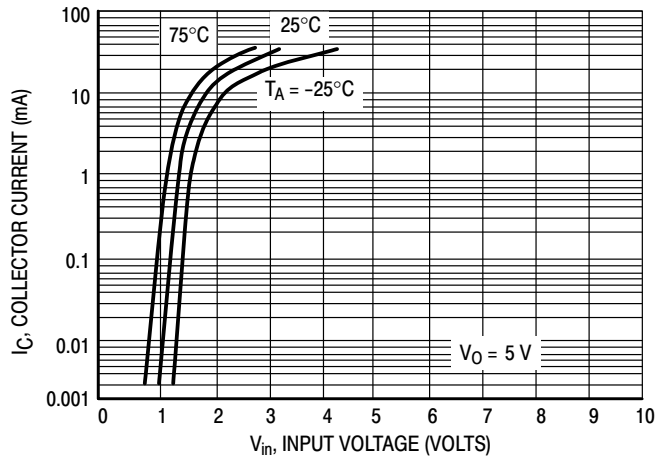


Figure 5. Output Current versus Input Voltage

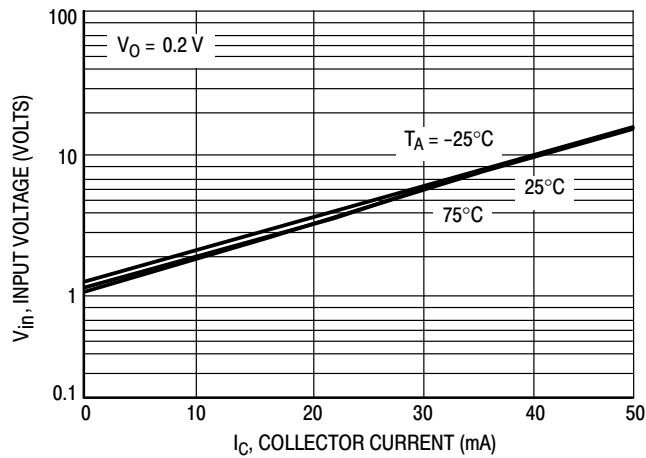


Figure 6. Input Voltage versus Output Current

NSTB1005DXV5T1G

TYPICAL ELECTRICAL CHARACTERISTICS — NPN TRANSISTOR

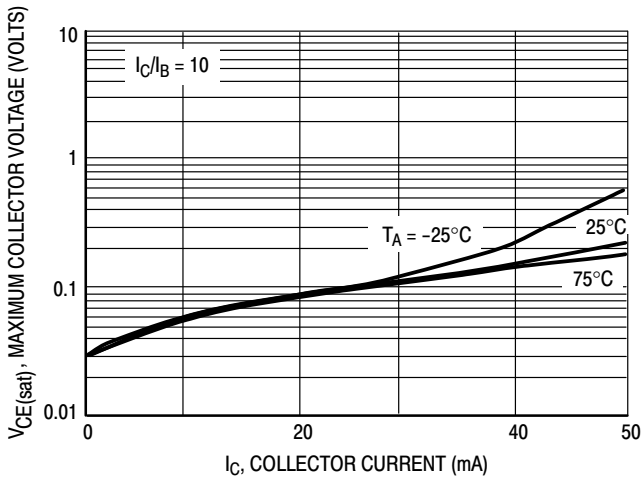


Figure 7. $V_{CE(sat)}$ versus I_C

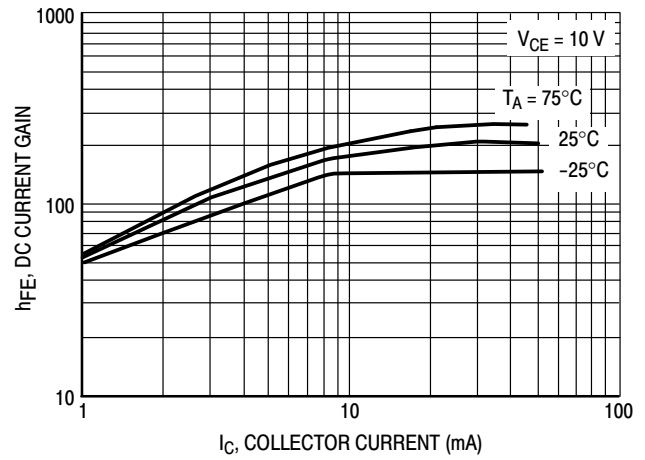


Figure 8. DC Current Gain

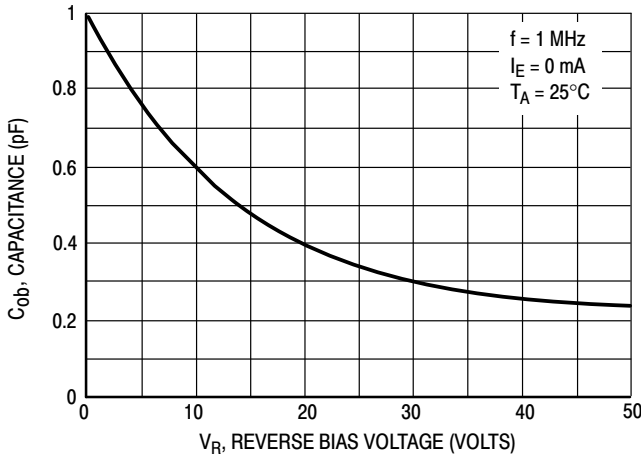


Figure 9. Output Capacitance

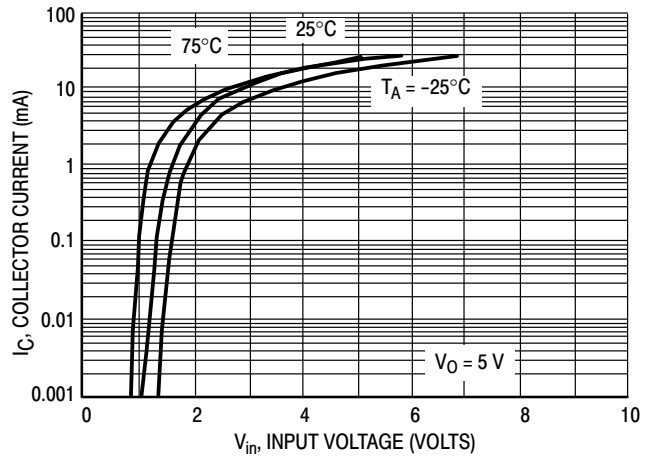


Figure 10. Output Current versus Input Voltage

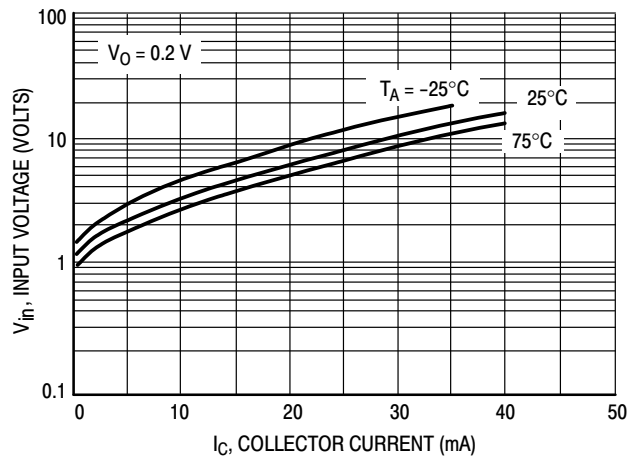
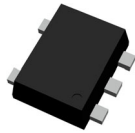


Figure 11. Input Voltage versus Output Current

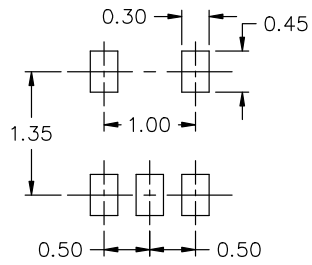
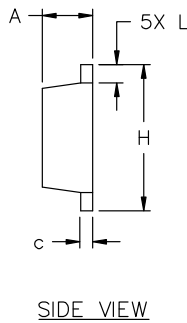
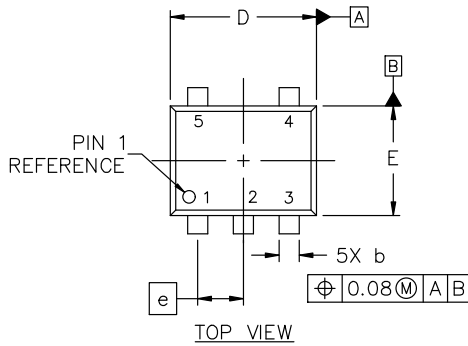
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



SOT-553-5 1.60x1.20x0.55, 0.50P
CASE 463B
ISSUE D

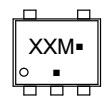
DATE 21 FEB 2024



- NOTES:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
 2. ALL DIMENSION ARE IN MILLIMETERS.
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
b	0.17	0.22	0.27
c	0.08	0.13	0.18
D	1.55	1.60	1.65
E	1.15	1.20	1.25
e	0.50 BSC		
H	1.55	1.60	1.65
L	0.10	0.20	0.30

GENERIC MARKING DIAGRAM*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED MOUNTING FOOTPRINT*
 * FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

- | | | | | |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>STYLE 1:
 PIN 1. BASE
 2. EMITTER
 3. BASE
 4. COLLECTOR
 5. COLLECTOR</p> | <p>STYLE 2:
 PIN 1. CATHODE
 2. COMMON ANODE
 3. CATHODE 2
 4. CATHODE 3
 5. CATHODE 4</p> | <p>STYLE 3:
 PIN 1. ANODE 1
 2. N/C
 3. ANODE 2
 4. CATHODE 2
 5. CATHODE 1</p> | <p>STYLE 4:
 PIN 1. SOURCE 1
 2. DRAIN 1/2
 3. SOURCE 1
 4. GATE 1
 5. GATE 2</p> | <p>STYLE 5:
 PIN 1. ANODE
 2. EMITTER
 3. BASE
 4. COLLECTOR
 5. CATHODE</p> |
| <p>STYLE 6:
 PIN 1. EMITTER 2
 2. BASE 2
 3. EMITTER 1
 4. COLLECTOR 1
 5. COLLECTOR 2/BASE 1</p> | <p>STYLE 7:
 PIN 1. BASE
 2. EMITTER
 3. BASE
 4. COLLECTOR
 5. COLLECTOR</p> | <p>STYLE 8:
 PIN 1. CATHODE
 2. COLLECTOR
 3. N/C
 4. BASE
 5. EMITTER</p> | <p>STYLE 9:
 PIN 1. ANODE
 2. CATHODE
 3. ANODE
 4. ANODE
 5. ANODE</p> | |

DOCUMENT NUMBER:	98AON11127D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOT-553-5 1.60x1.20x0.55, 0.50P	PAGE 1 OF 1

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales