

# NLSV4T240E

## 4-Bit Dual-Supply Inverting Level Translator

The NLSV4T240E is a 4-bit configurable dual-supply voltage level translator. The input  $A_n$  and output  $B_n$  ports are designed to track two different power supply rails,  $V_{CCA}$  and  $V_{CCB}$  respectively. Both supply rails are configurable from 0.9 V to 4.5 V allowing universal low-voltage translation from the input  $A_n$  to the output  $B_n$  port.

The NLSV4T240E is similar to the NLSV4T240; however, it has enhanced power-off characteristics.

### Features

- Wide  $V_{CCA}$  and  $V_{CCB}$  Operating Range: 0.9 V to 4.5 V
- High-Speed w/ Balanced Propagation Delay
- Inputs and Outputs have OVT Protection to 4.5 V
- Non-preferential  $V_{CCA}$  and  $V_{CCB}$  Sequencing
- Outputs at 3-State until Active  $V_{CC}$  is Reached
- Power-Off Protection
- Outputs Switch to 3-State with  $V_{CCB}$  at GND
- Ultra-Small Packaging: 1.7 mm x 2.0 mm UQFN12
- This is a Pb-Free Device

### Typical Applications

- Mobile Phones, PDAs, Other Portable Devices

### Important Information

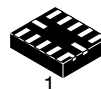
- ESD Protection for All Pins:  
HBM (Human Body Model) > 6000 V  
MM (Machine Model) > 300 V



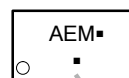
ON Semiconductor®

<http://onsemi.com>

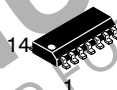
### MARKING DIAGRAMS



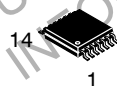
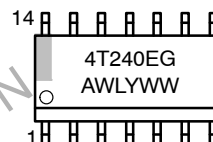
UQFN12  
MU SUFFIX  
CASE 523AE



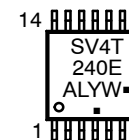
AE = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)



SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DT SUFFIX  
CASE 948G



A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week  
G or ▪ = Pb-Free Package  
(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NLSV4T240EMUTAG	UQFN12 (Pb-Free)	3000/Tape & Reel
NLSV4T240EDR2G	SO-14 (Pb-Free)	2500/Tape & Reel
NLSV4T240EDTR2G	TSSOP14 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NLSV4T240E

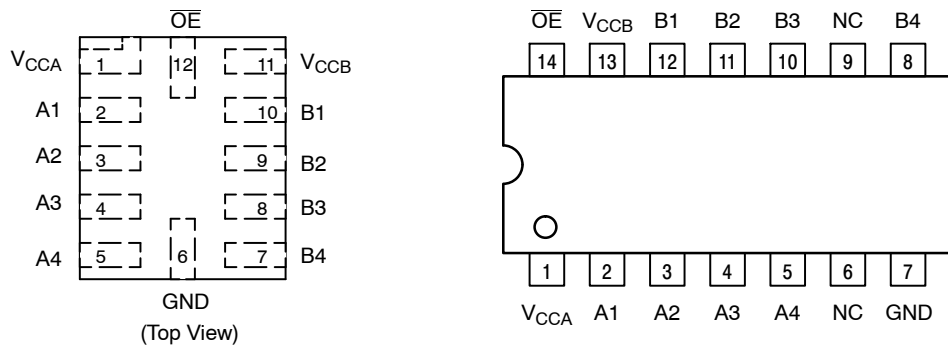


Figure 1. Pin Assignments

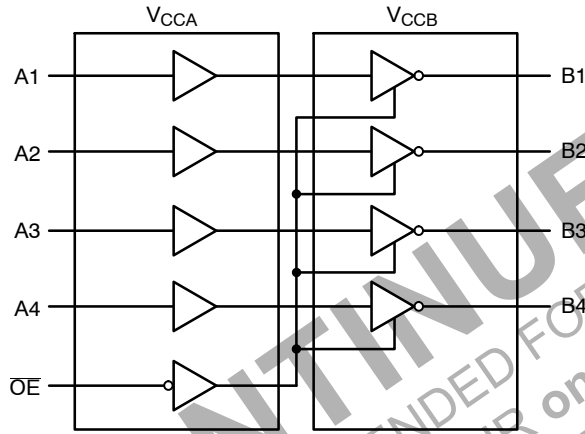


Figure 2. Logic Diagram

## PIN ASSIGNMENT

Pin	Function
V <sub>CCA</sub>	Input Port DC Power Supply
V <sub>CCB</sub>	Output Port DC Power Supply
GND	Ground
A <sub>n</sub>	Input Port
B <sub>n</sub>	Output Port
OE	Output Enable

## TRUTH TABLE

Inputs		Outputs
OE	A <sub>n</sub>	B <sub>n</sub>
L	L	H
L	H	L
H	X	3-State

# NLSV4T240E

## MAXIMUM RATINGS

Symbol	Rating	Value	Condition	Unit
$V_{CCA}, V_{CCB}$	DC Supply Voltage	-0.5 to +5.5		V
$V_I$	DC Input Voltage $A_n$	-0.5 to +5.5		V
$V_C$	Control Input $\overline{OE}$	-0.5 to +5.5		V
$V_O$	DC Output Voltage (Power Down) $B_n$	-0.5 to +5.5	$V_{CCA} = V_{CCB} = 0$	V
	(Active Mode) $B_n$	-0.5 to +5.5		V
	(Tri-State Mode) $B_n$	-0.5 to +5.5		V
$I_{IK}$	DC Input Diode Current	-20	$V_I < \text{GND}$	mA
$I_{OK}$	DC Output Diode Current	-50	$V_O < \text{GND}$	mA
$I_O$	DC Output Source/Sink Current	$\pm 50$		mA
$I_{CCA}, I_{CCB}$	DC Supply Current Per Supply Pin	$\pm 100$		mA
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 100$		mA
$T_{STG}$	Storage Temperature	-65 to +150		$^{\circ}\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CCA}, V_{CCB}$	Positive DC Supply Voltage	0.9	4.5	V
$V_I$	Bus Input Voltage	GND	4.5	V
$V_C$	Control Input $\overline{OE}$	GND	4.5	V
$V_{IO}$	Bus Output Voltage (Power Down Mode) $B_n$	GND	4.5	V
	(Active Mode) $B_n$	GND	$V_{CCB}$	V
	(Tri-State Mode) $B_n$	GND	4.5	V
$T_A$	Operating Temperature Range	-40	+85	$^{\circ}\text{C}$
$\Delta t / \Delta V$	Input Transition Rise or Rate $V_I$ , from 30% to 70% of $V_{CC}$ ; $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0	10	nS

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	$V_{CCA}$ (V)	$V_{CCB}$ (V)	-40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$		Unit
					Min	Max	
$V_{IH}$	Input HIGH Voltage (An, $\overline{OE}$ )		3.6 – 4.5	0.9 – 4.5	2.7	-	V
			2.7 – 3.6		2.0	-	
			2.3 – 2.7		1.7	-	
			1.4 – 2.3		$0.75 * V_{CCA}$	-	
			0.9 – 1.4		$0.9 * V_{CCA}$	-	
$V_{IL}$	Input LOW Voltage (An, $\overline{OE}$ )		3.6 – 4.5	0.9 – 4.5	-	0.8	V
			2.7 – 3.6		-	0.8	
			2.3 – 2.7		-	0.7	
			1.4 – 2.3		-	$0.35 * V_{CCA}$	
			0.9 – 1.4		-	$0.1 * V_{CCA}$	

# NLSV4T240E

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	-40°C to +85°C		Unit
					Min	Max	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -100 μA; V <sub>I</sub> = V <sub>IH</sub>	0.9 – 4.5	0.9 – 4.5	V <sub>CCB</sub> – 0.2	–	V
		I <sub>OH</sub> = -0.5 mA; V <sub>I</sub> = V <sub>IH</sub>	0.9	0.9	0.75 * V <sub>CCB</sub>	–	
		I <sub>OH</sub> = -2 mA; V <sub>I</sub> = V <sub>IH</sub>	1.4	1.4	1.05	–	
		I <sub>OH</sub> = -6 mA; V <sub>I</sub> = V <sub>IH</sub>	1.65	1.65	1.25	–	
			2.3	2.3	2.0	–	
		I <sub>OH</sub> = -12 mA; V <sub>I</sub> = V <sub>IH</sub>	2.3	2.3	1.8	–	
			2.7	2.7	2.2	–	
		I <sub>OH</sub> = -18 mA; V <sub>I</sub> = V <sub>IH</sub>	2.3	2.3	1.7	–	
3.0	3.0		2.4	–			
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 100 μA; V <sub>I</sub> = V <sub>IL</sub>	0.9 – 4.5	0.9 – 4.5	–	0.2	V
		I <sub>OL</sub> = 0.5 mA; V <sub>I</sub> = V <sub>IH</sub>	1.1	1.1	–	0.3	
		I <sub>OL</sub> = 2 mA; V <sub>I</sub> = V <sub>IH</sub>	1.4	1.4	–	0.35	
		I <sub>OL</sub> = 6 mA; V <sub>I</sub> = V <sub>IL</sub>	1.65	1.65	–	0.3	
			2.3	2.3	–	0.4	
		I <sub>OL</sub> = 12 mA; V <sub>I</sub> = V <sub>IL</sub>	2.3	2.3	–	0.4	
			2.7	2.7	–	0.4	
		I <sub>OL</sub> = 18 mA; V <sub>I</sub> = V <sub>IL</sub>	2.3	2.3	–	0.6	
3.0	3.0		–	0.4			
I <sub>OL</sub> = 24 mA; V <sub>I</sub> = V <sub>IL</sub>	3.0	3.0	–	0.55			
I <sub>I</sub>	Input Leakage Current	V <sub>I</sub> = V <sub>CCA</sub> or GND	0.9 – 4.5	0.9 – 4.5	-1.0	1.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	OE = 0 V	0	0.9 – 4.5	-1.0	1.0	μA
			0.9 – 4.5	0	-1.0	1.0	
I <sub>CCA</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CCA</sub> or GND; I <sub>O</sub> = 0, V <sub>CCA</sub> = V <sub>CCB</sub>	0.9 – 4.5	0.9 – 4.5	–	2.0	μA
I <sub>CCB</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CCA</sub> or GND; I <sub>O</sub> = 0, V <sub>CCA</sub> = V <sub>CCB</sub>	0.9 – 4.5	0.9 – 4.5	–	2.0	μA
I <sub>CCA</sub> + I <sub>CCB</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CCA</sub> or GND; I <sub>O</sub> = 0, V <sub>CCA</sub> = V <sub>CCB</sub>	0.9 – 4.5	0.9 – 4.5	–	4.0	μA
ΔI <sub>CCA</sub>	Increase in I <sub>CC</sub> per Input Voltage, Other Inputs at V <sub>CCA</sub> or GND	V <sub>I</sub> = V <sub>CCA</sub> – 0.6 V; V <sub>I</sub> = V <sub>CCA</sub> or GND	4.5	4.5	–	10	μA
			3.6	3.6	–	5.0	
ΔI <sub>CCB</sub>	Increase in I <sub>CC</sub> per Input Voltage, Other Inputs at V <sub>CCA</sub> or GND	V <sub>I</sub> = V <sub>CCA</sub> – 0.6 V; V <sub>I</sub> = V <sub>CCA</sub> or GND	4.5	4.5	–	10	μA
			3.6	3.6	–	5.0	
I <sub>OZ</sub>	I/O Tri-State Output Leakage Current (T <sub>A</sub> = 25°C, OE = V <sub>CCA</sub> )	V <sub>O</sub> = 0 V	4.5	4.5	–	1.0	μA
		V <sub>O</sub> = 4.5 V	4.5	4.5	–	10	
		V <sub>O</sub> = 0 to 4.5 V	2.5	3.5	–	105	
			3.0	3.75	–	110	
			3.3	3.0	–	75	
3.75	1.5	–	10				

# NLSV4T240E

## TOTAL STATIC POWER CONSUMPTION ( $I_{CCA} + I_{CCB}$ )

$V_{CCA}$ (V)	-40°C to +85°C										Unit
	$V_{CCB}$ (V)										
	4.5		3.3		2.8		1.8		0.9		
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
4.5		2		2		2		2		< 1.5	$\mu$ A
3.3		2		2		2		2		< 1.5	$\mu$ A
2.8		< 2		< 1		< 1		< 0.5		< 0.5	$\mu$ A
1.8		< 1		< 1		< 0.5		< 0.5		< 0.5	$\mu$ A
0.9		< 0.5		< 0.5		< 0.5		< 0.5		< 0.5	$\mu$ A

NOTE: Connect ground before applying supply voltage  $V_{CCA}$  or  $V_{CCB}$ . This device is designed with the feature that the power-up sequence of  $V_{CCA}$  and  $V_{CCB}$  will not damage the IC.

## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	$V_{CCA}$ (V)	-40°C to +85°C										Unit
			$V_{CCB}$ (V)										
			4.5		3.3		2.8		1.8		1.5		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{PLH}$ , $t_{PHL}$ (Note 1)	Propagation Delay, $A_n$ to $B_n$	4.5		3.0		3.2		3.4		3.7		4.0	nS
		3.6		3.3		3.5		3.7		4.0		4.3	
		2.8		3.5		3.7		3.9		4.2		4.5	
		1.8		3.8		4.0		4.2		4.5		4.8	
		1.5		4.1		4.3		4.5		4.8		5.0	
$t_{PZH}$ , $t_{PZL}$ (Note 1)	Output Enable, $OE$ to $B_n$	4.5		4.4		4.8		5.2		5.7		6.2	nS
		3.3		4.7		5.1		5.5		6.0		6.5	
		2.8		4.9		5.3		5.7		6.2		6.7	
		1.8		5.2		5.6		6.0		6.5		7.0	
		1.5		5.5		5.9		6.3		6.8		7.3	
$t_{PHZ}$ , $t_{PLZ}$ (Note 1)	Output Disable, $OE$ to $B_n$	4.5		4.4		4.8		5.2		5.7		6.2	nS
		3.3		4.7		5.1		5.5		6.0		6.5	
		2.8		4.9		5.3		5.7		6.2		6.7	
		1.8		5.2		5.6		6.0		6.5		7.0	
		1.5		5.5		5.9		6.3		6.8		7.3	
$t_{OSHL}$ , $t_{OSLH}$ (Note 1)	Output to Output Skew, Data to Output	4.1		0.15		0.15		0.15		0.15		0.15	nS
		3.6		0.15		0.15		0.15		0.15		0.15	
		2.8		0.15		0.15		0.15		0.15		0.15	
		1.8		0.15		0.15		0.15		0.15		0.15	
		1.2		0.15		0.15		0.15		0.15		0.15	

1. Propagation delays defined per Figures 3 and 4.

## CAPACITANCE

Symbol	Parameter	Test Conditions	Typ (Note 2)	Unit
$C_{IN}$	Control Pin Input Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA/B}$	3.5	pF
$C_{I/O}$	I/O Pin Input Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA/B}$	5.0	pF
$C_{PD}$	Power Dissipation Capacitance	$V_{CCA} = V_{CCB} = 3.3$ V, $V_I = 0$ V or $V_{CCA}$ , $f = 10$ MHz	20	pF

2. Typical values are at  $T_A = +25^\circ\text{C}$ .

3.  $C_{PD}$  is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from:  
 $I_{CC(\text{operating})} \cong C_{PD} \times V_{CC} \times f_{IN} \times N_{SW}$  where  $I_{CC} = I_{CCA} + I_{CCB}$  and  $N_{SW}$  = total number of outputs switching.

# NLSV4T240E

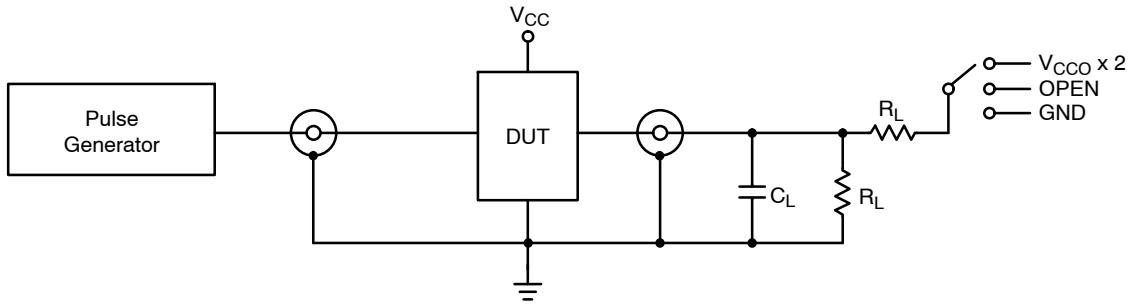
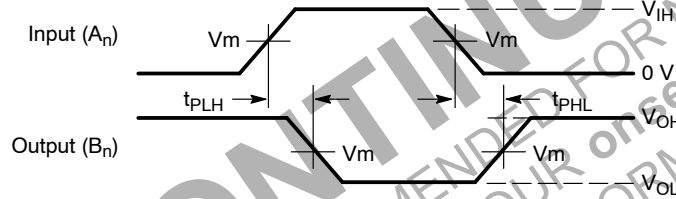


Figure 3. AC (Propagation Delay) Test Circuit

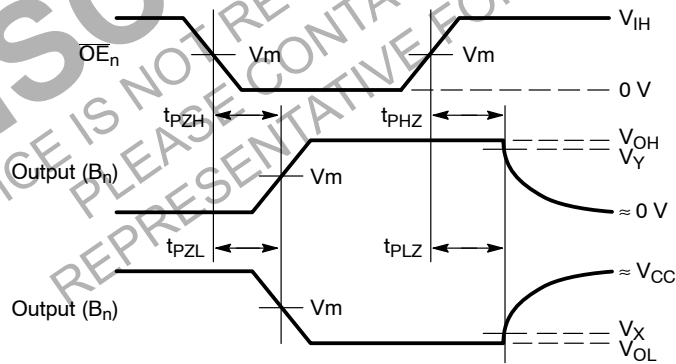
Test	Switch
$t_{PLH}$ , $t_{PHL}$	OPEN
$t_{PLZ}$ , $t_{PZL}$	$V_{CCO} \times 2$
$t_{PHZ}$ , $t_{PZH}$	GND

$C_L = 15 \text{ pF}$  or equivalent (includes probe and jig capacitance)  
 $R_L = 2 \text{ k}\Omega$  or equivalent  
 $Z_{OUT}$  of pulse generator =  $50 \Omega$



Waveform 1 - Propagation Delays

$t_R = t_F = 2.0 \text{ ns}$ , 10% to 90%;  $f = 1 \text{ MHz}$ ;  $t_W = 500 \text{ ns}$



Waveform 2 - Output Enable and Disable Times

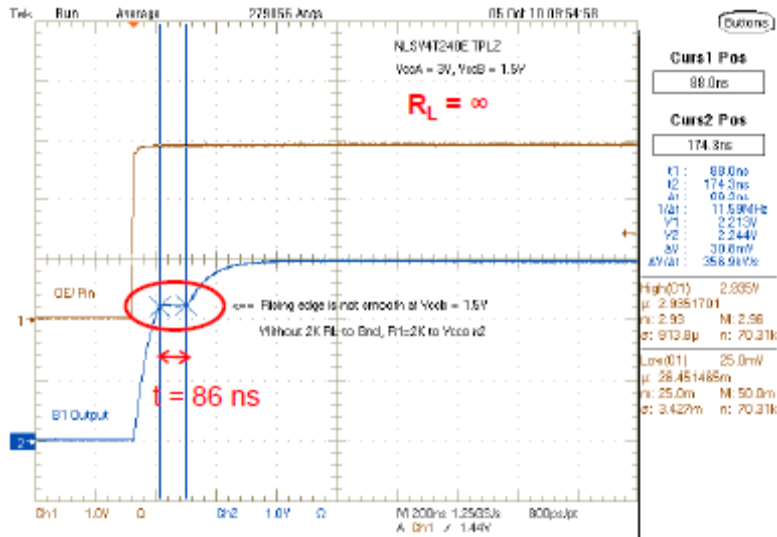
$t_R = t_F = 2.0 \text{ ns}$ , 10% to 90%;  $f = 1 \text{ MHz}$ ;  $t_W = 500 \text{ ns}$

Figure 4. AC (Propagation Delay) Test Circuit Waveforms

Symbol	$V_{CC}$				
	3.0 V – 4.5 V	2.3 V – 2.7 V	1.65 V – 1.95 V	1.4 V – 1.6 V	0.9 V – 1.3 V
$V_{mA}$	$V_{CCA}/2$	$V_{CCA}/2$	$V_{CCA}/2$	$V_{CCA}/2$	$V_{CCA}/2$
$V_{mB}$	$V_{CCB}/2$	$V_{CCB}/2$	$V_{CCB}/2$	$V_{CCB}/2$	$V_{CCB}/2$
$V_X$	$V_{OL} \times 0.1$	$V_{OL} \times 0.1$	$V_{OL} \times 0.1$	$V_{OL} \times 0.1$	$V_{OL} \times 0.1$
$V_Y$	$V_{OH} \times 0.9$	$V_{OH} \times 0.9$	$V_{OH} \times 0.9$	$V_{OH} \times 0.9$	$V_{OH} \times 0.9$

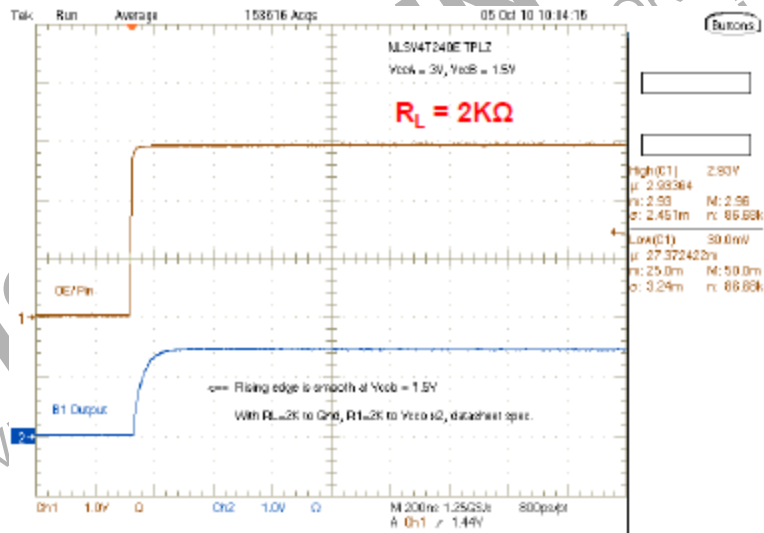
# NLSV4T240E

## APPLICATIONS INFORMATION



( $C_L = 50$  pF,  $R_L = 2$  k $\Omega$ ,  $R_{pull-up} = 50$  k $\Omega$ , test circuit shown in Figure 3)

**Figure 5. Typical Tri-State Output**



( $C_L = 50$  pF,  $R_L = \infty$ ,  $R_{pull-up} = 2$  k $\Omega$ , test circuit shown in Figure 3)

**Figure 6. Typical Tri-State Output**

Typical tri-state output waveforms of the NLSX4T240E are shown in Figures 5 and 6. The shape of the output waveform during a tri-state condition corresponding to the disable time ( $t_{PHZ}$ ,  $t_{PLZ}$ ) depends on the configuration of the pull-up circuit. Figure 5 shows a smooth monotonically increasing exponentially waveform because a 2 k $\Omega$  resistance is connected between the output and ground.

Figure 6 shows that the output may have a ‘shelf’ or a short duration where the slope of the waveform is equal to zero if no load resistance is connected to ground. The NLSX4T240E was created from the NLSV4T240 to minimize the ‘shelf’ of the waveform during the disable time.

# MECHANICAL CASE OUTLINE

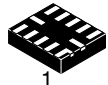
## PACKAGE DIMENSIONS

ON Semiconductor®

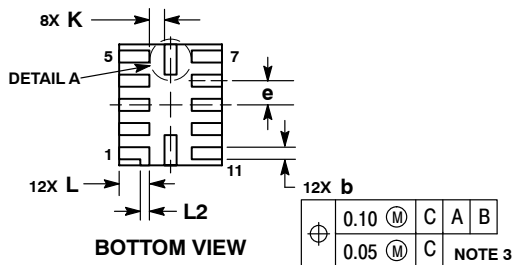
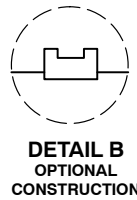
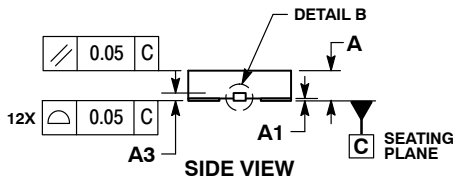
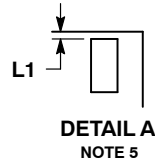
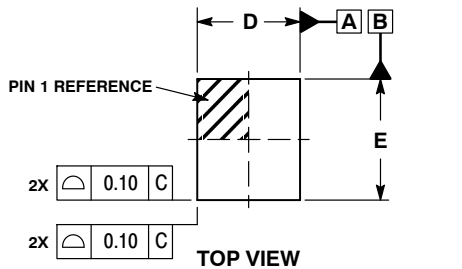


UQFN12 1.7x2.0, 0.4P  
CASE 523AE-01  
ISSUE A

DATE 11 JUN 2007



SCALE 4:1

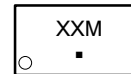


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH 0.03 MAX ON BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.70 BSC	
E	2.00 BSC	
e	0.40 BSC	
K	0.20	---
L	0.45	0.55
L1	0.00	0.03
L2	0.15 REF	

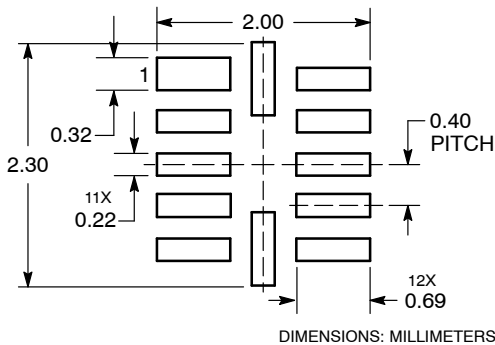
GENERIC MARKING DIAGRAM\*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

MOUNTING FOOTPRINT  
SOLDERMASK DEFINED

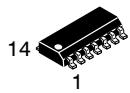


DOCUMENT NUMBER:	98AON23418D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	UQFN12 1.7 X 2.0, 0.4P	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.



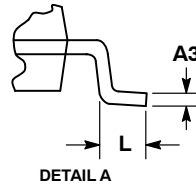
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-14 NB	PAGE 1 OF 2

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**SOIC-14**  
**CASE 751A-03**  
**ISSUE L**

DATE 03 FEB 2016

STYLE 1:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. NO CONNECTION  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 2:  
 CANCELLED

STYLE 3:  
 PIN 1. NO CONNECTION  
 2. ANODE  
 3. ANODE  
 4. NO CONNECTION  
 5. ANODE  
 6. NO CONNECTION  
 7. ANODE  
 8. ANODE  
 9. ANODE  
 10. NO CONNECTION  
 11. ANODE  
 12. ANODE  
 13. NO CONNECTION  
 14. COMMON CATHODE

STYLE 4:  
 PIN 1. NO CONNECTION  
 2. CATHODE  
 3. CATHODE  
 4. NO CONNECTION  
 5. CATHODE  
 6. NO CONNECTION  
 7. CATHODE  
 8. CATHODE  
 9. CATHODE  
 10. NO CONNECTION  
 11. CATHODE  
 12. CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 5:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. NO CONNECTION  
 7. COMMON ANODE  
 8. COMMON CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. ANODE/CATHODE  
 12. ANODE/CATHODE  
 13. NO CONNECTION  
 14. COMMON ANODE

STYLE 6:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE  
 7. CATHODE  
 8. ANODE  
 9. ANODE  
 10. ANODE  
 11. ANODE  
 12. ANODE  
 13. ANODE  
 14. ANODE

STYLE 7:  
 PIN 1. ANODE/CATHODE  
 2. COMMON ANODE  
 3. COMMON CATHODE  
 4. ANODE/CATHODE  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. ANODE/CATHODE  
 8. ANODE/CATHODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. COMMON CATHODE  
 12. COMMON ANODE  
 13. ANODE/CATHODE  
 14. ANODE/CATHODE

STYLE 8:  
 PIN 1. COMMON CATHODE  
 2. ANODE/CATHODE  
 3. ANODE/CATHODE  
 4. NO CONNECTION  
 5. ANODE/CATHODE  
 6. ANODE/CATHODE  
 7. COMMON ANODE  
 8. COMMON ANODE  
 9. ANODE/CATHODE  
 10. ANODE/CATHODE  
 11. NO CONNECTION  
 12. ANODE/CATHODE  
 13. ANODE/CATHODE  
 14. COMMON CATHODE

<b>DOCUMENT NUMBER:</b>	<b>98ASB42565B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOIC-14 NB</b>	<b>PAGE 2 OF 2</b>

**onsemi** and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**TSSOP-14 WB**  
CASE 948G  
ISSUE C

DATE 17 FEB 2016

SCALE 2:1



**NOTES:**

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**GENERIC MARKING DIAGRAM\***

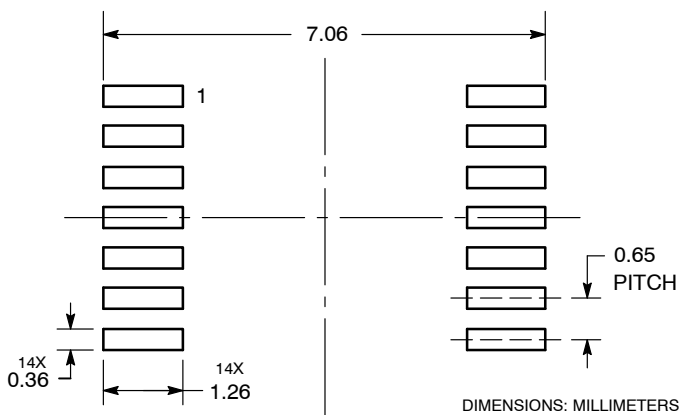


- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**SOLDERING FOOTPRINT**



<b>DOCUMENT NUMBER:</b>	<b>98ASH70246A</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>TSSOP-14 WB</b>	<b>PAGE 1 OF 1</b>

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)