

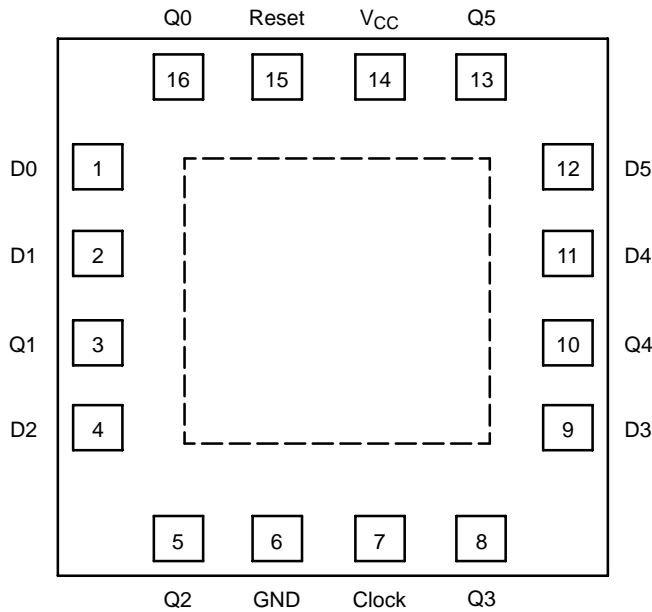
NLSF1174

Hex D Flip-Flop with Common Clock and Reset

This device consists of six D flip-flops with common Clock and Reset inputs. Each flip-flop is loaded with a low-to-high transition of the Clock input. Reset is asynchronous and active low. All inputs/outputs are standard CMOS compatible.

Features

- Output Drive Compatibility: 10 LSTTL Loads
- Outputs Directly Interface to CMOS
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- MSL Level 1
- Chip Complexity: 162 FET
- Pb-Free Package is Available*



Center pad on bottom may be connected to V_{CC} of device.
This pad must be isolated or connected to V_{CC}.

Figure 1. PIN ASSIGNMENT (Top View)



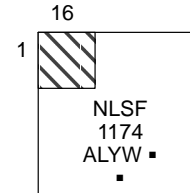
ON Semiconductor®

<http://onsemi.com>



QFN-16
MN SUFFIX
CASE 485G

MARKING DIAGRAM



NLSF1174 = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package
(Note: Microdot may be in either location)

FUNCTION TABLE

| Inputs | | | Output |
|--------|-------|---|-----------|
| Reset | Clock | D | Q |
| L | X | X | L |
| H | | H | H |
| H | | L | L |
| H | L | X | No Change |
| H | | X | No Change |

ORDERING INFORMATION

| Device | Package | Shipping† |
|---------------|---------------------|--------------------|
| NLSF1174MNR2 | QFN-16 | 3000 / Tape & Reel |
| NLSF1174MNR2G | QFN-16 (Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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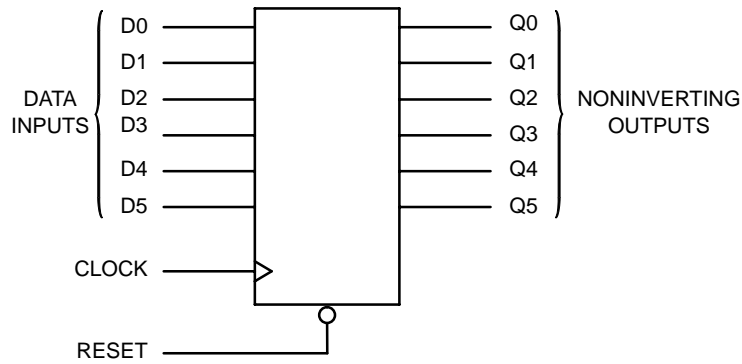


Figure 2. LOGIC DIAGRAM

DESIGN/VALUE TABLE

| Design Criteria | Value | Unit |
|---------------------------------|-------|---------|
| Internal Gate Count* | 40.5 | ea |
| Internal Gate Propagation Delay | 1.5 | ns |
| Internal Gate Power Dissipation | 5.0 | μ W |
| Speed Power Product | .0075 | pJ |

*Equivalent to a two-input NAND gate.

MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|--|---------------|--------------------------|----------------|
| DC Supply Voltage (Referenced to GND) | V_{CC} | -0.5 to +7.0 | V |
| DC Input Voltage (Referenced to GND) | V_{IN} | -1.5 to $V_{CC} + 1.5$ | V |
| DC Output Voltage (Referenced to GND) (Note 1) | V_{OUT} | -0.5 to $V_{CC} + 0.5$ | V |
| DC Input Current, per Pin | I_{IN} | ± 20 | mA |
| DC Output Current, per Pin | I_{OUT} | ± 25 | mA |
| DC Supply Current, V_{CC} and GND Pins | I_{CC} | ± 50 | mA |
| Storage Temperature Range | T_{STG} | -65 to +150 | $^{\circ}$ C |
| Lead Temperature, 1 mm from Case for 10 Seconds PDIP, SOIC, TSSOP | T_L | 260 | $^{\circ}$ C |
| Junction Temperature Under Bias | T_J | +150 | $^{\circ}$ C |
| Thermal Resistance QFN | θ_{JA} | 80 | $^{\circ}$ C/W |
| Power Dissipation in Still Air at 85 $^{\circ}$ C QFN | P_D | 800 | mW |
| Moisture Sensitivity | MSL | Level 1 | |
| Flammability Rating Oxygen Index: 30 to 35 | F_R | UL 94 V-0 @ 0.125 in | |
| ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4) | V_{ESD} | > 2000 > 100 > 500 | V |
| Latchup Performance Above V_{CC} and Below GND at 85 $^{\circ}$ C (Note 5) | $I_{LATCHUP}$ | ± 300 | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. I_O absolute maximum rating must be observed.

2. Tested to EIA/JESD22-A114-A.

3. Tested to EIA/JESD22-A115-A.

4. Tested to JESD22-C101-A.

5. Tested to EIA/JESD78.

6. For high frequency or heavy load considerations, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Unit |
|---|-------------------------|-----|----------|------|
| DC Supply Voltage (Referenced to GND) | V_{CC} | 2.0 | 6.0 | V |
| DC Input Voltage, Output Voltage (Referenced to GND) (Note 7) | V_{IN}, V_{OUT} | 0 | V_{CC} | V |
| Operating Temperature, All Package Types | T_A | -55 | +125 | °C |
| Input Rise and Fall Time (Figure 4) | t_r, t_f | 0 | 1000 | ns |
| | $V_{CC} = 2.0\text{ V}$ | 0 | 500 | |
| | $V_{CC} = 4.5\text{ V}$ | 0 | 500 | |
| | $V_{CC} = 6.0\text{ V}$ | 0 | 400 | |

7. Unused inputs may not be left open. All inputs must be tied to a high- or low-logic input voltage level.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Parameter | Test Conditions | Symbol | V_{CC} V | Guaranteed Limit | | | Unit |
|--|---|----------|---------------|------------------|-------|--------|------|
| | | | | -55°C to 25°C | ≤85°C | ≤125°C | |
| Minimum High-Level Input Voltage | $V_{OUT} = 0.1\text{ V}$ or $V_{CC} - 0.1\text{ V}$ $ I_{OUT} \leq 20\ \mu\text{A}$ | V_{IH} | 2.0 | 1.5 | 1.5 | 1.5 | V |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.2 | 4.2 | 4.2 | |
| Maximum Low-Level Input Voltage | $V_{OUT} = 0.1\text{ V}$ or $V_{CC} - 0.1\text{ V}$ $ I_{OUT} \leq 20\ \mu\text{A}$ | V_{IL} | 2.0 | 0.5 | 0.5 | 0.5 | V |
| | | | 4.5 | 1.35 | 1.35 | 1.35 | |
| | | | 6.0 | 1.8 | 1.8 | 1.8 | |
| Minimum High-Level Output Voltage | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20\ \mu\text{A}$ | V_{OH} | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0\text{ mA}$ $ I_{OUT} \leq 5.2\text{ mA}$ | | 4.5 | 3.98 | 3.84 | 3.7 | |
| | | | 6.0 | 5.48 | 5.34 | 5.2 | |
| Maximum Low-Level Output Voltage | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20\ \mu\text{A}$ | V_{OL} | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0\text{ mA}$ $ I_{OUT} \leq 5.2\text{ mA}$ | | 4.5 | 0.26 | 0.33 | 0.4 | |
| | | | 6.0 | 0.26 | 0.33 | 0.4 | |
| Maximum Input Leakage Current | $V_{IN} = V_{CC}$ or GND | I_{IN} | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| Maximum Quiescent Supply Current (per Package) | $V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\ \mu\text{A}$ | I_{CC} | 6.0 | 4.0 | 40 | 160 | μA |

8. Information on typical parametric values, along with high frequency or heavy load considerations, can be found in the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{ pF}$, Input $t_r = t_f = 6.0\text{ ns}$)

| Parameter | Symbol | V_{CC} V | Guaranteed Limit | | | Unit |
|--|------------------------|---|------------------|-------|--------|------|
| | | | -55°C to 25°C | ≤85°C | ≤125°C | |
| Maximum Clock Frequency (50% Duty Cycle) (Figures 4 and 7) | f_{max} | 2.0 | 6.0 | 4.8 | 4.0 | MHz |
| | | 4.5 | 30 | 24 | 20 | |
| | | 6.0 | 35 | 28 | 24 | |
| Maximum Propagation Delay, Clock to Q (Figures 5 and 7) | t_{PLH} t_{PHL} | 2.0 | 110 | 140 | 165 | ns |
| | | 4.5 | 22 | 28 | 33 | |
| | | 6.0 | 19 | 24 | 28 | |
| Maximum Propagation Delay, Reset to Q (Figures 2 and 7) | t_{PLH} t_{PHL} | 2.0 | 110 | 140 | 160 | ns |
| | | 4.5 | 21 | 28 | 32 | |
| | | 6.0 | 19 | 24 | 27 | |
| Maximum Output Transition Time, Any Output (Figures 4 and 7) | t_{TLH} t_{THL} | 2.0 | 75 | 95 | 110 | ns |
| | | 4.5 | 15 | 19 | 22 | |
| | | 6.0 | 13 | 16 | 19 | |
| Maximum Input Capacitance | C_{in} | | 10 | 10 | 10 | pF |
| Power Dissipation Capacitance, per Enabled Output (Note 10) | C_{PD} | Typical @ 25°C, $V_{CC} = 5.0\text{ V}$ | | | | pF |
| | | 62 | | | | |

9. For propagation delays with loads other than 50 pF, and information on typical parametric values, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

10. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

NLSF1174

TIMING REQUIREMENTS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6.0 \text{ ns}$)

| Parameter | Figure | Symbol | V_{CC} V | Guaranteed Limit | | | | | | Unit |
|---|--------|------------|-------------------|-------------------|--------------------|-------------------|--------------------|-------------------|--------------------|------|
| | | | | -55°C to 25°C | | ≤ 85°C | | ≤ 125°C | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| Minimum Setup Time, Data to Clock | 6 | t_{su} | 2.0 4.5 6.0 | 50 10 9.0 | | 65 13 11 | | 75 15 13 | | ns |
| Minimum Hold Time, Clock to Data | 6 | t_h | 2.0 4.5 6.0 | 5.0 5.0 5.0 | | 5.0 5.0 5.0 | | 5.0 5.0 5.0 | | ns |
| Minimum Recovery Time, Reset Inactive to Clock | 5 | t_{rec} | 2.0 4.5 6.0 | 5.0 5.0 5.0 | | 5.0 5.0 5.0 | | 5.0 5.0 5.0 | | ns |
| Minimum Pulse Width, Clock | 4 | t_w | 2.0 4.5 6.0 | 75 15 13 | | 95 19 16 | | 110 22 19 | | ns |
| Minimum Pulse Width, Reset | 5 | t_w | 2.0 4.5 6.0 | 75 15 13 | | 95 19 16 | | 110 22 19 | | ns |
| Maximum Input Rise and Fall Times | 4 | t_r, t_f | 2.0 4.5 6.0 | | 1000 500 400 | | 1000 500 400 | | 1000 500 400 | ns |

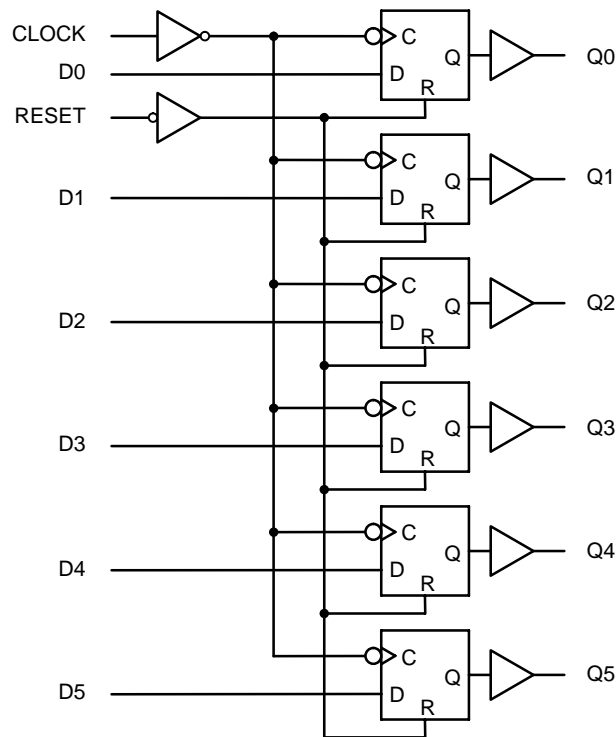


Figure 3. Expanded Logic Diagram

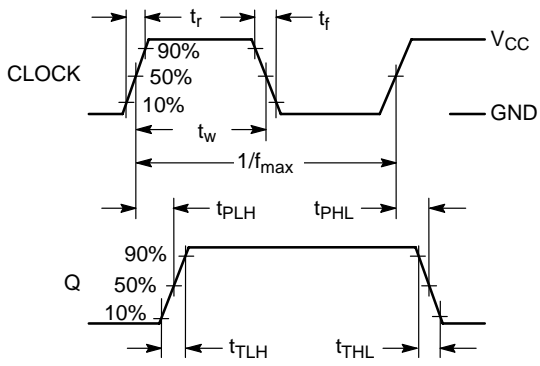


Figure 4. Switching Waveform

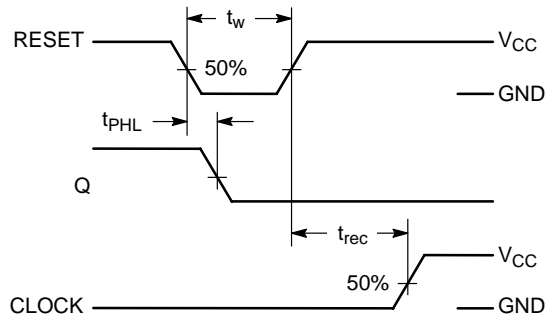


Figure 5. Switching Waveform

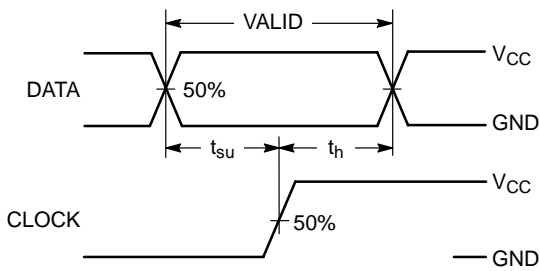
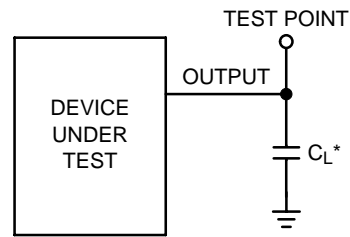


Figure 6. Switching Waveform



*Includes all probe and jig capacitance

Figure 7. Test Circuit

PIN1/PRODUCT ORIENTATION CARRIER TAPE

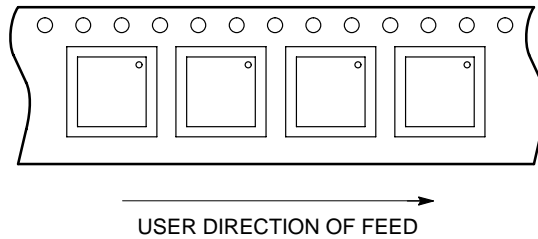


Figure 8.

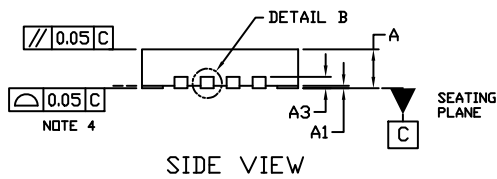
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

QFN16 3x3, 0.5P
CASE 485G
ISSUE G

DATE 08 OCT 2021

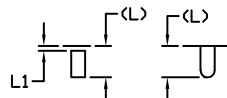


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



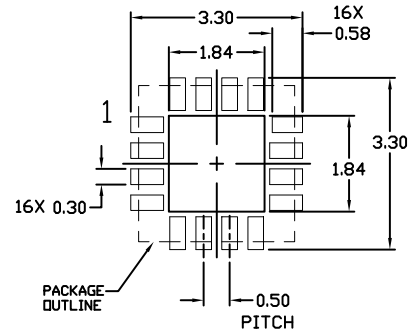
DETAIL B
ALTERNATE
CONSTRUCTIONS



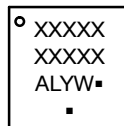
DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS

| DIM | MILLIMETERS | | |
|----------|-------------|------|------|
| | MIN. | NDM. | MAX. |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.03 | 0.05 |
| A3 | 0.20 REF | | |
| <i>b</i> | 0.18 | 0.24 | 0.30 |
| D | 3.00 BSC | | |
| D2 | 1.65 | 1.75 | 1.85 |
| E | 3.00 BSC | | |
| E2 | 1.65 | 1.75 | 1.85 |
| <i>e</i> | 0.50 BSC | | |
| <i>k</i> | 0.18 TYP | | |
| L | 0.30 | 0.40 | 0.50 |
| L1 | 0.00 | 0.08 | 0.15 |

MOUNTING FOOTPRINT



GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
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