

Dual Unbuffered Inverter

NL27WZU04

The NL27WZU04 is a high performance dual unbuffered inverter operating from a 1.65 to 5.5 V supply.

Features

- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Input Overvoltage Tolerant up to 5.5 V
- I_{OFF} Supports Partial Power Down Protection
- Source/Sink 24 mA at 3.0 V
- Available in SC-88, SC-74 and UDFN6 Packages
- Chip Complexity < 100 FETs
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

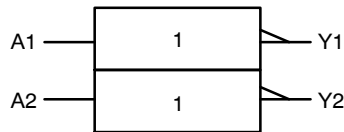
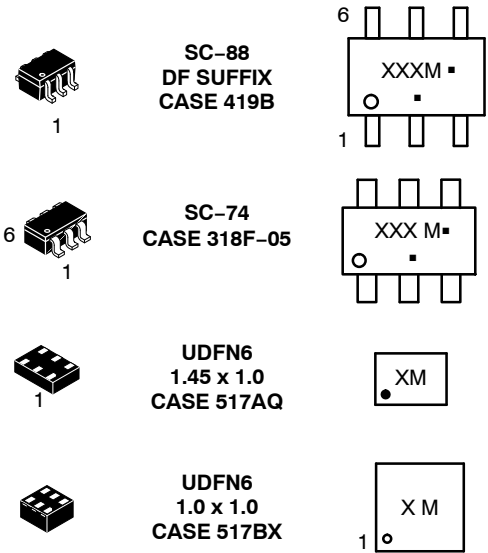


Figure 1. Logic Symbol

MARKING DIAGRAMS



X, XXX = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 7 of this data sheet.

NL27WZU04

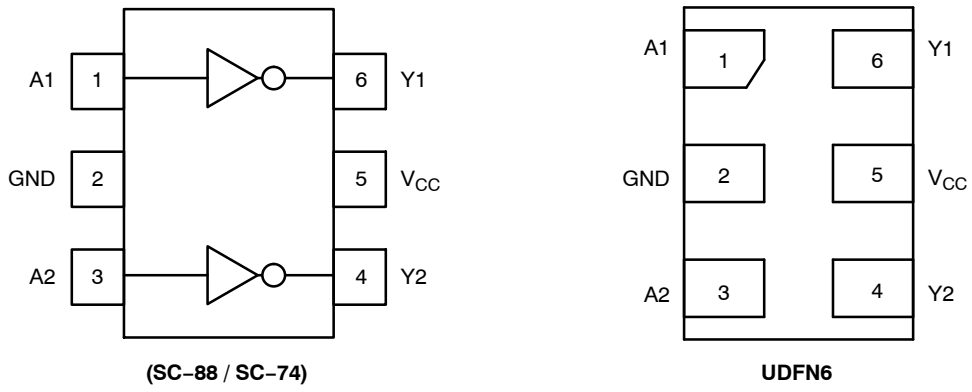


Figure 2. Pinout (Top View)

PIN ASSIGNMENT

Pin	Function
1	A1
2	GND
3	A2
4	Y2
5	V _{CC}
6	Y1

FUNCTION TABLE

A Input	Y Output
L	H
H	L

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MAXIMUM RATINGS

Symbol	Characteristics	Value	Unit	
V _{CC}	DC Supply Voltage	-0.5 to +6.5	V	
V _{IN}	DC Input Voltage	-0.5 to +6.5	V	
V _{OUT}	DC Output Voltage	-0.5 to V _{CC} + 0.5	V	
I _{IK}	DC Input Diode Current V _{IN} < GND	-50	mA	
I _{OK}	DC Output Diode Current	±50	mA	
I _{OUT}	DC Output Source/Sink Current	±50	mA	
I _{CC} or I _{GND}	DC Supply Current per Supply Pin or Ground Pin	±100	mA	
T _{STG}	Storage Temperature Range	-65 to +150	°C	
T _L	Lead Temperature, 1 mm from Case for 10 secs	260	°C	
T _J	Junction Temperature Under Bias	+150	°C	
θ _{JA}	Thermal Resistance (Note 2)	SC-88 SC-74 UDFN6	377 320 154	°C/W
P _D	Power Dissipation in Still Air	SC-88 SC-74 UDFN6	332 300 812	mW
MSL	Moisture Sensitivity	Level 1	-	
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	-	
V _{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 1000	V
I _{Latchup}	Latchup Performance (Note 4)	±100	mA	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 10mm-by-1inch, 2 ounce copper trace no air flow per JESD51-7.
3. HBM tested to ANSI/ESDA/JEDEC JS-001-2017. CDM tested to EIA/JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115-A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit	
V _{CC}	Positive DC Supply Voltage	1.65	5.5	V	
V _{IN}	DC Input Voltage	0	5.5	V	
V _{OUT}	DC Output Voltage	0	V _{CC}		
T _A	Operating Temperature Range	-55	+125	°C	
t _r , t _f	Input Rise and Fall Time	V _{CC} = 1.65 V to 1.95 V V _{CC} = 2.3 V to 2.7 V V _{CC} = 3.0 V to 3.6 V V _{CC} = 4.5 V to 5.5 V	0 0 0 0	20 20 10 5	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-55°C ≤ T _A ≤ 125°C		Units
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		1.65 to 1.95	0.85 V _{CC}	-	-	0.85 V _{CC}	-	V
			2.3 to 5.5	0.80 V _{CC}	-	-	0.80 V _{CC}	-	
V _{IL}	Low-Level Input Voltage		1.65 to 1.95	-	-	0.15 V _{CC}	-	0.15 V _{CC}	V
			2.3 to 5.5	-	-	0.20 V _{CC}	-	0.20 V _{CC}	
V _{OH}	High-Level Output Voltage	V _{IN} = GND I _{OH} = -100 μA I _{OH} = -4 mA I _{OH} = -8 mA I _{OH} = -12 mA I _{OH} = -16 mA I _{OH} = -24 mA I _{OH} = -32 mA	1.65 to 5.5	V _{CC} - 0.1	V _{CC}	-	V _{CC} - 0.1	-	V
			1.65	1.29	1.4	-	1.29	-	
			2.3	1.9	2.1	-	1.9	-	
			2.7	2.2	2.4	-	2.2	-	
			3.0	2.4	2.7	-	2.4	-	
			3.0	2.3	2.5	-	2.3	-	
			4.5	3.8	4.0	-	3.8	-	
V _{OL}	Low-Level Output Voltage	V _{IN} = V _{CC} I _{OL} = 100 μA I _{OL} = 4 mA I _{OL} = 8 mA I _{OL} = 12 mA I _{OL} = 16 mA I _{OL} = 24 mA I _{OL} = 32 mA	1.65 to 5.5	-	-	0.1	-	0.1	V
			1.65	-	0.08	0.24	-	0.24	
			2.3	-	0.2	0.3	-	0.3	
			2.7	-	0.22	0.4	-	0.4	
			3.0	-	0.28	0.4	-	0.4	
			3.0	-	0.38	0.55	-	0.55	
			4.5	-	0.42	0.55	-	0.55	
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	1.65 to 5.5	-	-	±0.1	-	±1.0	μA
I _{OFF}	Power Off Leakage Current	V _{IN} = 5.5 V	0	-	-	1.0	-	10	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5	-	-	1.0	-	10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-55°C ≤ T _A ≤ 125°C		Units
				Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay Input A to Y (Figure 3 and 4)	R _L = 1 MΩ, C _L = 15 pF	1.65 to 1.95	-	5.5	9.8	-	11.0	ns
		R _L = 1 MΩ, C _L = 15 pF	2.3 to 2.7	-	3.3	5.7	-	6.3	
		R _L = 1 MΩ, C _L = 15 pF	3.0 to 3.6	-	2.7	4.1	-	4.5	
		R _L = 500 Ω, C _L = 50 pF		-	4.0	6.4	-	7.0	
		R _L = 1 MΩ, C _L = 15 pF	4.5 to 5.5	-	2.2	3.3	-	3.6	
		R _L = 500 Ω, C _L = 50 pF		-	3.4	5.6	-	6.2	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = 5.5 V, V _{IN} = 0 V or V _{CC}	2.5	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.5 V, V _{IN} = 0 V or V _{CC}	4.0	pF
C _{PD}	Power Dissipation Capacitance (Note 5)	10 MHz, V _{CC} = 5.5 V, V _{IN} = 0 V or V _{CC}	4.0	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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C_L includes probe and jig capacitance
 R_T is Z_{OUT} of pulse generator (typically 50 Ω)
 $f = 1$ MHz

Figure 3. Test Circuit

Test	Switch Position	C_L , pF	R_L , Ω	R_1 , Ω
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table		
t_{PLZ} / t_{PZL}	$2 \times V_{CC}$	50	500	500
t_{PHZ} / t_{PZH}	GND	50	500	500

X = Don't Care



Figure 4. Switching Waveforms

V_{CC} , V	V_{mi} , V	V_{mo} , V		V_Y , V
		t_{PLH} , t_{PHL}	t_{PZL} , t_{PLZ} , t_{PZH} , t_{PHZ}	
1.65 to 1.95	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.15
2.3 to 2.7	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.15
3.0 to 3.6	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.3
4.5 to 5.5	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.3

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DEVICE ORDERING INFORMATION

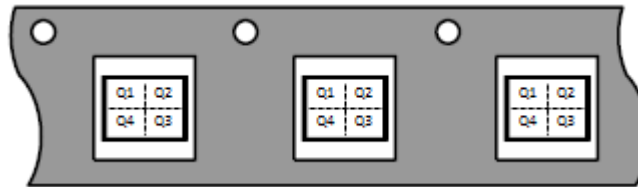
Device	Packages	Specific Device Code	Pin 1 Orientation (See below)	Shipping [†]
NL27WZU04DFT2G	SC-88	M6	Q4	3000 / Tape & Reel
NL27WZU04DFT2G-Q*	SC-88	M6	Q4	3000 / Tape & Reel
NL27WZU04DBVT1G	SC-74	M6	Q4	3000 / Tape & Reel
NL27WZU04MU1TCG (In Development)	UDFN6, 1.45 x 1.0, 0.5P	TBD	Q4	3000 / Tape & Reel
NL27WZU04MU3TCG (In Development)	UDFN6, 1.0 x 1.0, 0.35P	TBD	Q4	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

Pin 1 Orientation in Tape and Reel

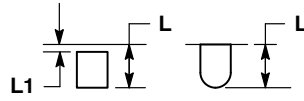
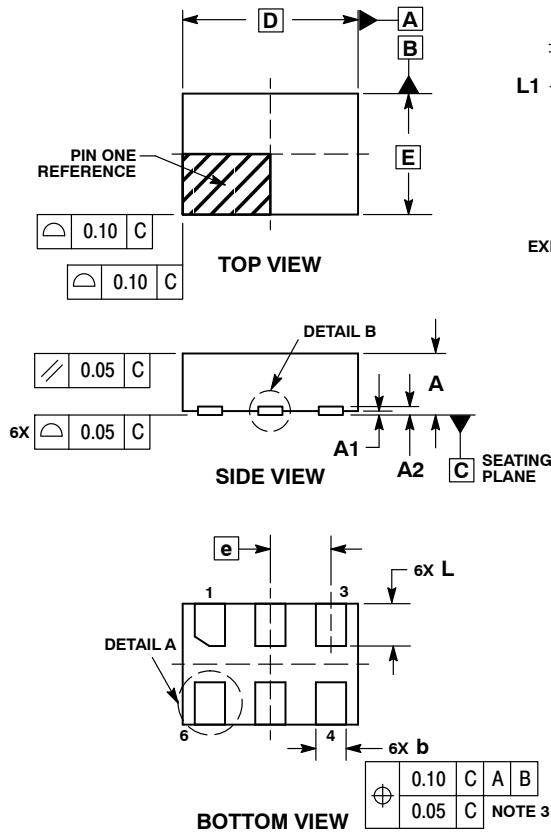
Direction of Feed



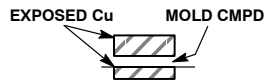
NL27WZU04

PACKAGE DIMENSIONS

UDFN6, 1.45x1.0, 0.5P
CASE 517AQ
ISSUE O



DETAIL A
OPTIONAL
CONSTRUCTIONS



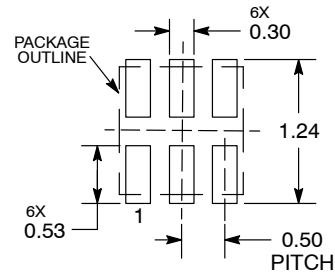
DETAIL B
OPTIONAL
CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A2	0.07	REF
b	0.20	0.30
D	1.45	BSC
E	1.00	BSC
e	0.50	BSC
L	0.30	0.40
L1	---	0.15

MOUNTING FOOTPRINT



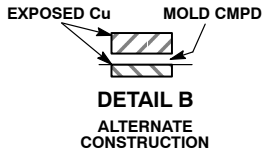
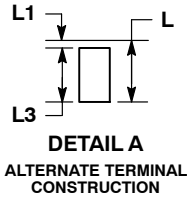
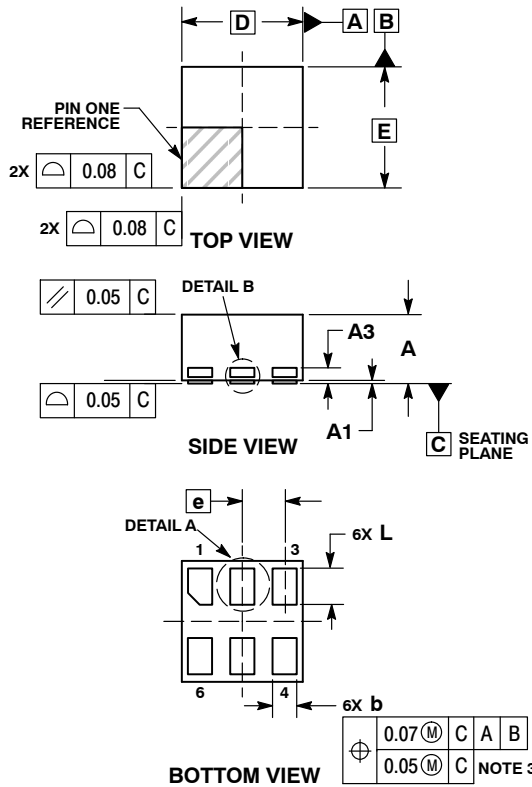
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NL27WZU04

PACKAGE DIMENSIONS

UDFN6, 1x1, 0.35P
CASE 517BX
ISSUE O

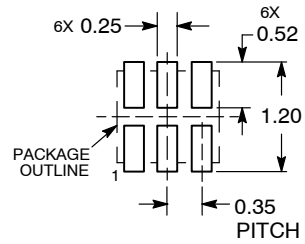


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

DIM	MILLIMETERS	
	MIN	MAX
A	0.50	0.65
A1	0.00	0.05
A3	0.13 REF	
b	0.17	0.23
D	1.00 BSC	
E	1.00 BSC	
e	0.35	
L	0.20	0.40
L1	---	0.15
L3	0.26	0.33

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

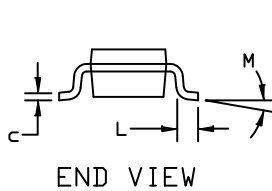
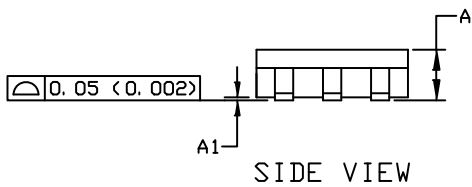
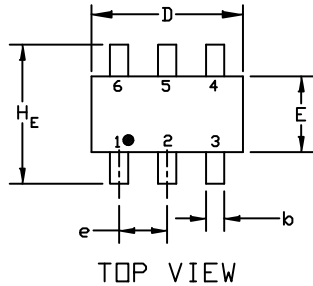
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



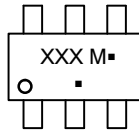
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SC-74
CASE 318F
ISSUE P

DATE 07 OCT 2021



GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

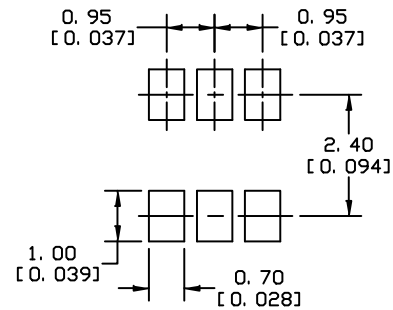
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994
2. CONTROLLING DIMENSION: INCHES
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
HE	2.50	2.75	3.00	0.099	0.108	0.118
L	0.20	0.40	0.60	0.008	0.016	0.024
M	0*	---	10*	0*	---	10*



* For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

SOLDERING FOOTPRINT

- | | | | | | |
|---|--|---|--|---|---|
| <p>STYLE 1:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE</p> | <p>STYLE 2:
PIN 1. NO CONNECTION
2. COLLECTOR
3. EMITTER
4. NO CONNECTION
5. COLLECTOR
6. BASE</p> | <p>STYLE 3:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1</p> | <p>STYLE 4:
PIN 1. COLLECTOR 2
2. EMITTER 1/EMITTER 2
3. COLLECTOR 1
4. EMITTER 3
5. BASE 1/BASE 2/COLLECTOR 3
6. BASE 3</p> | <p>STYLE 5:
PIN 1. CHANNEL 1
2. ANODE
3. CHANNEL 2
4. CHANNEL 3
5. CATHODE
6. CHANNEL 4</p> | <p>STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE</p> |
| <p>STYLE 7:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1</p> | <p>STYLE 8:
PIN 1. EMITTER 1
2. BASE 2
3. COLLECTOR 2
4. EMITTER 2
5. BASE 1
6. COLLECTOR 1</p> | <p>STYLE 9:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2</p> | <p>STYLE 10:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE</p> | <p>STYLE 11:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR</p> | |

DOCUMENT NUMBER:	98ASB42973B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SC-74	PAGE 1 OF 1

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

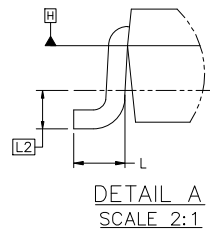
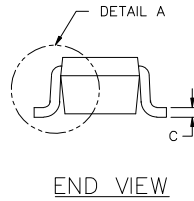
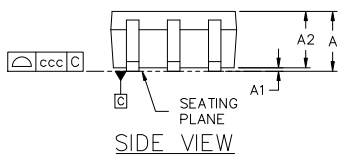
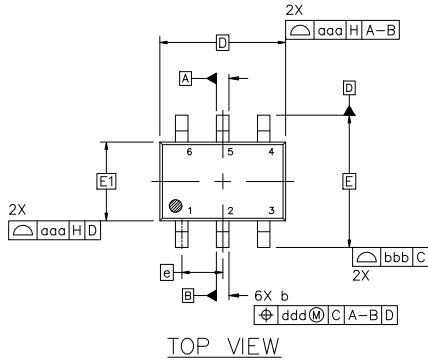


SC-88 2.00x1.25x0.90, 0.65P
CASE 419B-02
ISSUE Z

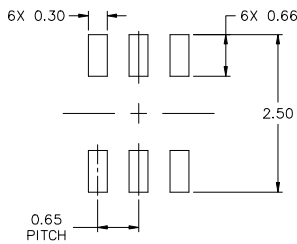
DATE 18 APR 2024

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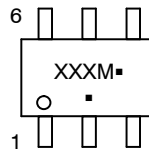
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.00	---	0.10
A2	0.70	0.90	1.00
b	0.15	0.20	0.25
c	0.08	0.15	0.22
D	2.00 BSC		
E	2.10 BSC		
E1	1.25 BSC		
e	0.65 BSC		
L	0.26	0.36	0.46
L2	0.15 BSC		
aaa	0.15		
bbb	0.30		
ccc	0.10		
ddd	0.10		



GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- M = Date Code*
- = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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CASE 419B-02
ISSUE Z

DATE 18 APR 2024

STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 2: CANCELLED	STYLE 3: CANCELLED	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	STYLE 8: CANCELLED	STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
STYLE 13: PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 14: PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	STYLE 15: PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	STYLE 16: PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	STYLE 17: PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	STYLE 18: PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
STYLE 19: PIN 1. IOUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	STYLE 20: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	STYLE 21: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	STYLE 22: PIN 1. D1 (i) 2. GND 3. D2 (j) 4. D2 (c) 5. VBUS 6. D1 (c)	STYLE 23: PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	STYLE 24: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
STYLE 25: PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	STYLE 26: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	STYLE 27: PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	STYLE 28: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 29: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	STYLE 30: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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