# NL17SHT08

# 2-Input AND Gate / CMOS Logic Level Shifter

The NL17SHT08 is an advanced high speed CMOS 2−input AND gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL−type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic−level translator from 3 V CMOS logic to 5 V CMOS Logic or from 1.8 V CMOS logic to 3 V CMOS Logic while operating at the high−voltage power supply.

The NL17SHT08 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the NL17SHT08 to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when $V_{CC}$ = 0 V. These input and output structures help prevent device destruction caused by supply voltage − input/output voltage mismatch, battery backup, hot insertion, etc.

### Features

- High Speed: $t_{PD}$ = 3.5 ns (Typ) at $V_{CC}$ = 5 V
- Low Power Dissipation: $I_{CC}$ = 1 μA (Max) at $T_A$ = 25°C
- TTL−Compatible Inputs: $V_{IL}$ = 0.8 V; $V_{IH}$ = 2 V
- CMOS−Compatible Outputs: $V_{OH}$ > 0.8 $V_{CC}$; $V_{OL}$ < 0.1 $V_{CC}$ @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- These are Pb−Free Devices

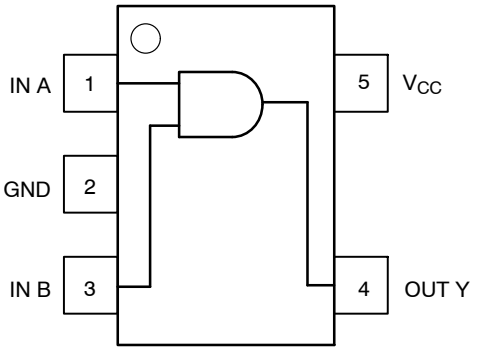



**Figure 1. Pinout** (Top View)

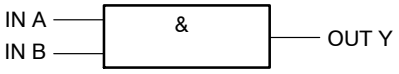


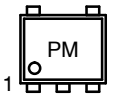

**Figure 2. Logic Symbol**

**ON Semiconductor®**

**http://onsemi.com**

**MARKING DIAGRAM**

**SOT−953**
**CASE 527AE**




P = Specific Device Code
M = Month Code

| PIN ASSIGNMENT | |
|---|---|
| 1 | IN A |
| 2 | GND |
| 3 | IN B |
| 4 | OUT Y |
| 5 | $V_{CC}$ |

**FUNCTION TABLE**

| Inputs | | Output |
|---|---|---|
| **A** | **B** | **Y** |
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

**MAXIMUM RATINGS**

| Symbol | Characteristics | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | −0.5 to +7.0 | V |
| $V_{IN}$ | DC Input Voltage | | −0.5 to +7.0 | V |
| $V_{OUT}$ | DC Output Voltage | $V_{CC}$ = 0<br>High or Low State | −0.5 to 7.0<br>−0.5 to $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input Diode Current | | −20 | mA |
| $I_{OK}$ | Output Diode Current | $V_{OUT}$ < GND; $V_{OUT}$ > $V_{CC}$ | ±20 | mA |
| $I_{OUT}$ | DC Output Current | | ±25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND | | 50 | mA |
| $P_D$ | Power dissipation in still air | | 50 | mW |
| $T_L$ | Lead temperature, 1 mm from case for 10 s | | 260 | °C |
| $T_J$ | Junction temperature under bias | | +150 | °C |
| $T_{stg}$ | Storage temperature | | −65 to +150 | °C |
| $I_{Latchup}$ | Latchup Performance | Above $V_{CC}$ and Below GND at 125°C (Note 1) | ±100 | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tested to EIA/JESD78

**RECOMMENDED OPERATING CONDITIONS**

| Symbol | Characteristics | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | 3.0 | 5.5 | V |
| $V_{IN}$ | DC Input Voltage | | 0.0 | 5.5 | V |
| $V_{OUT}$ | DC Output Voltage | $V_{CC}$ = 0<br>High or Low State | 0.0<br>0.0 | 5.5<br>$V_{CC}$ | V |
| $T_A$ | Operating Temperature Range | | −55 | +125 | °C |
| $t_r$ , $t_f$ | Input Rise and Fall Time | $V_{CC}$ = 3.3 V ± 0.3 V<br>$V_{CC}$ = 5.0 V ± 0.5 V | 0<br>0 | 100<br>20 | ns/V |

**Device Junction Temperature versus Time to 0.1% Bond Failures**

| Junction Temperature °C | Time, Hours | Time, Years |
|---|---|---|
| 80 | 1,032,200 | 117.8 |
| 90 | 419,300 | 47.9 |
| 100 | 178,700 | 20.4 |
| 110 | 79,600 | 9.4 |
| 120 | 37,000 | 4.2 |
| 130 | 17,800 | 2.0 |
| 140 | 8,900 | 1.0 |

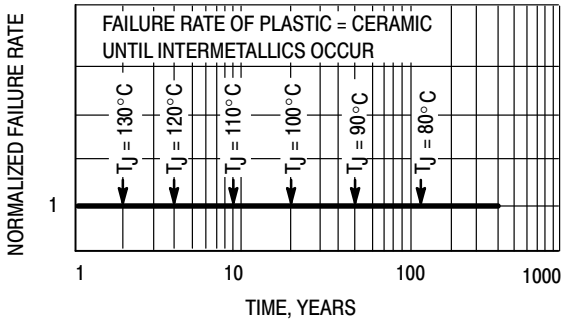



**Figure 3. Failure Rate vs. Time Junction Temperature**

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | $V_{CC}$ (V) | $T_A$ = 25°C | | | $T_A \le$ 85°C | | −55 ≤ $T_A \le$ 125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| $V_{IH}$ | Minimum High−Level Input Voltage | | 3.0<br>4.5<br>5.5 | 1.4<br>2.0<br>2.0 | | | 1.4<br>2.0<br>2.0 | | 1.4<br>2.0<br>2.0 | | V |
| $V_{IL}$ | Maximum Low−Level Input Voltage | | 3.0<br>4.5<br>5.5 | | | 0.53<br>0.8<br>0.8 | | 0.53<br>0.8<br>0.8 | | 0.53<br>0.8<br>0.8 | V |
| $V_{OH}$ | Minimum High−Level Output Voltage $V_{IN} = V_{IH}$ or $V_{IL}$ | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = −50 μA | 3.0<br>4.5 | 2.9<br>4.4 | 3.0<br>4.5 | | 2.9<br>4.4 | | 2.9<br>4.4 | | V |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = −4 mA<br>$I_{OH}$ = −8 mA | 3.0<br>4.5 | 2.58<br>3.94 | | | 2.48<br>3.80 | | 2.34<br>3.66 | | V |
| $V_{OL}$ | Maximum Low−Level Output Voltage $V_{IN} = V_{IH}$ or $V_{IL}$ | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OL}$ = 50 μA | 3.0<br>4.5 | | 0.0<br>0.0 | 0.1<br>0.1 | | 0.1<br>0.1 | | 0.1<br>0.1 | V |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OL}$ = 4 mA<br>$I_{OL}$ = 8 mA | 3.0<br>4.5 | | | 0.36<br>0.36 | | 0.44<br>0.44 | | 0.52<br>0.52 | V |
| $I_{IN}$ | Maximum Input Leakage Current | $V_{IN}$ = 5.5 V or GND | 0 to 5.5 | | | ±0.1 | | ±1.0 | | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{IN} = V_{CC}$ or GND | 5.5 | | | 1.0 | | 20 | | 40 | μA |
| $I_{CCT}$ | Quiescent Supply Current | Input: $V_{IN}$ = 3.4 V | 5.5 | | | 1.35 | | 1.50 | | 1.65 | mA |
| $I_{OPD}$ | Output Leakage Current | $V_{OUT}$ = 5.5 V | 0.0 | | | 0.5 | | 5.0 | | 10 | μA |

## AC ELECTRICAL CHARACTERISTICS $C_{load}$ = 50 pF, Input $t_r = t_f$ = 3.0 ns

| Symbol | Parameter | Test Conditions | $T_A$ = 25°C | | | $T_A \le$ 85°C | | −55 ≤ $T_A \le$ 125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Input A or B to Y | $V_{CC}$ = 3.3 ± 0.3 V $C_L$ = 15 pF<br>$C_L$ = 50 pF | | 4.1<br>5.9 | 8.8<br>12.3 | | 10.5<br>14.0 | | 12.5<br>16.5 | ns |
| | | $V_{CC}$ = 5.0 ± 0.5 V $C_L$ = 15 pF<br>$C_L$ = 50 pF | | 3.5<br>4.2 | 5.9<br>7.9 | | 7.0<br>9.0 | | 9.0<br>11.0 | |
| $C_{IN}$ | Maximum Input Capacitance | | | 5.5 | 10 | | 10 | | 10 | pF |

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Note 2) | 11 | pF |

2. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. $C_{PD}$ is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

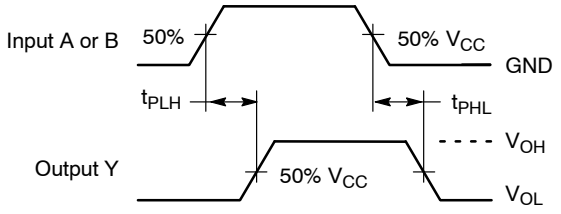
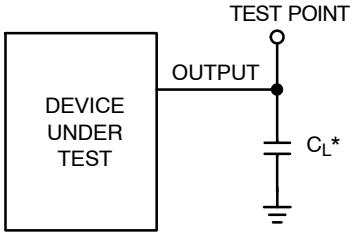



**Figure 4. Switching Waveforms**




*Includes all probe and jig capacitance

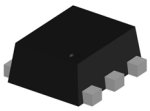
**Figure 5. Test Circuit**

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NL17SHT08P5T5G | SOT−953<br>(Pb−Free) | 8000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

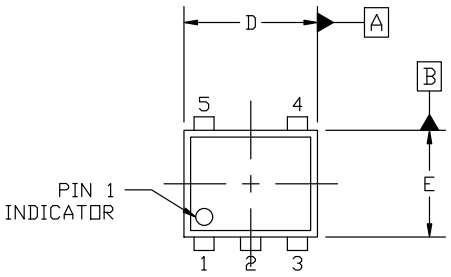


**SOT−953 1.00x0.80x0.37, 0.35P**
CASE 527AE
ISSUE F

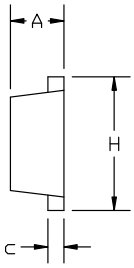
DATE 17 JAN 2024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

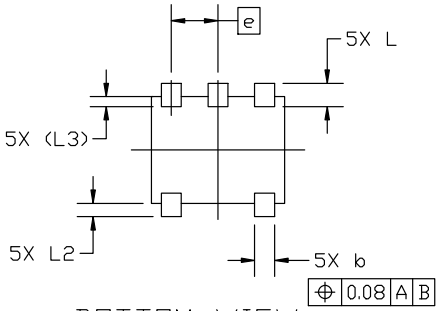
| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.34 | 0.37 | 0.40 |
| b | 0.10 | 0.15 | 0.20 |
| C | 0.07 | 0.12 | 0.17 |
| D | 0.95 | 1.00 | 1.05 |
| E | 0.75 | 0.80 | 0.85 |
| e | 0.35 BSC | | |
| H | 0.95 | 1.00 | 1.05 |
| L | 0.125 | 0.175 | 0.225 |
| L2 | 0.05 | 0.10 | 0.15 |
| L3 | 0.075 (REF) | | |



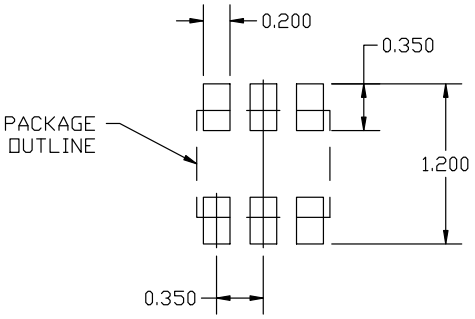

TOP VIEW




SIDE VIEW



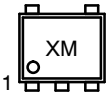

BOTTOM VIEW




RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC MARKING DIAGRAM***




X = Specific Device Code
M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98AON26457D** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. | |
| **DESCRIPTION:** | **SOT−953 1.00x0.80x0.37, 0.35P** | | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales