

NDF03N60Z, NDD03N60Z

N-Channel Power MOSFET 600 V, 3.6 Ω

Features

- Low ON Resistance
- Low Gate Charge
- ESD Diode–Protected Gate
- 100% Avalanche Tested
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	NDF	NDD	Unit
Drain–to–Source Voltage	V _{DSS}	600		V
Continuous Drain Current R _{θJC}	I _D	3.1 (Note 1)	2.6	A
Continuous Drain Current R _{θJC} T _A = 100°C	I _D	2.9 (Note 1)	1.65	A
Pulsed Drain Current, V _{GS} @ 10 V	I _{DM}	12	10	A
Power Dissipation R _{θJC}	P _D	27	61	W
Gate–to–Source Voltage	V _{GS}	±30		V
Single Pulse Avalanche Energy, I _D = 3.0 A	E _{AS}	100		mJ
ESD (HBM) (JESD 22–A114)	V _{esd}	3000		V
RMS Isolation Voltage (t = 0.3 sec., R.H. ≤ 30%, T _A = 25°C) (Figure 17)	V _{ISO}	4500		V
Peak Diode Recovery (Note 2)	dv/dt	4.5		V/ns
Continuous Source Current (Body Diode)	I _S	3.0		A
Maximum Temperature for Soldering Leads	T _L	260		°C
Operating Junction and Storage Temperature Range	T _J , T _{stg}	–55 to 150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

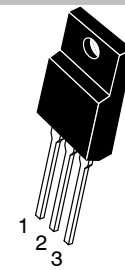
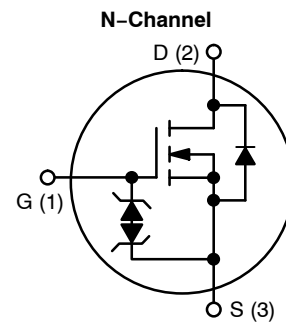
1. Limited by maximum junction temperature
2. I_{SD} = 3.0 A, di/dt ≤ 100 A/μs, V_{DD} ≤ BV_{DSS}, T_J = +150°C



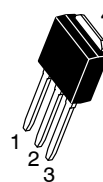
ON Semiconductor®

www.onsemi.com

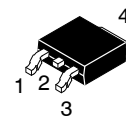
V _{DSS}	R _{DS(on)} (MAX) @ 1.2 A
600 V	3.6 Ω



NDF03N60ZG,
NDF03N60ZH
TO-220FP
CASE 221AH



NDD03N60Z-1G
IPAK
CASE 369D



NDD03N60ZT4G
DPAK
CASE 369AA

MARKING AND ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

NDF03N60Z, NDD03N60Z

THERMAL RESISTANCE

Parameter	Symbol	Value	Unit	
Junction-to-Case (Drain)	$R_{\theta JC}$	NDF03N60Z NDD03N60Z	4.7 2.0	°C/W
Junction-to-Ambient Steady State		(Note 3) NDF03N60Z (Note 4) NDD03N60Z (Note 3) NDD03N60Z-1	51 40 80	

3. Insertion mounted

4. Surface mounted on FR4 board using 1" sq. pad size, (Cu area = 1.127 in sq [2 oz] including traces).

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
----------------	-----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	BV_{DSS}	600			V
Breakdown Voltage Temperature Co-efficient	Reference to 25°C , $I_D = 1\text{ mA}$	$\Delta BV_{DSS}/\Delta T_J$		0.6		V/°C
Drain-to-Source Leakage Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	I_{DSS}	25°C		1	μA
			150°C		50	
Gate-to-Source Forward Leakage	$V_{GS} = \pm 20\text{ V}$	I_{GSS}			±10	μA

ON CHARACTERISTICS (Note 5)

Static Drain-to-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 1.2\text{ A}$	$R_{DS(on)}$		3.3	3.6	Ω
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 50\text{ }\mu\text{A}$	$V_{GS(th)}$	3.0	3.9	4.5	V
Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 1.5\text{ A}$	g_{FS}		2.0		S

DYNAMIC CHARACTERISTICS

Input Capacitance (Note 6)	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	C_{iss}	248	312	372	pF
Output Capacitance (Note 6)		C_{oss}	30	39	50	
Reverse Transfer Capacitance (Note 6)		C_{rss}	4	8	12	
Total Gate Charge (Note 6)	$V_{DD} = 300\text{ V}, I_D = 3.0\text{ A},$ $V_{GS} = 10\text{ V}$	Q_g	6	12	18	nC
Gate-to-Source Charge (Note 6)		Q_{gs}	1.5	2.5	4	
Gate-to-Drain ("Miller") Charge (Note 6)		Q_{gd}	3	6.1	9	
Plateau Voltage		V_{GP}		6.4		
Gate Resistance		R_g		6.0		Ω

RESISTIVE SWITCHING CHARACTERISTICS

Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 3.0\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 5\text{ }\Omega$	$t_{d(on)}$		9		ns
Rise Time		t_r		8		
Turn-Off Delay Time		$t_{d(off)}$		16		
Fall Time		t_f		10		

SOURCE-DRAIN DIODE CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Diode Forward Voltage	$I_S = 3.0\text{ A}, V_{GS} = 0\text{ V}$	V_{SD}			1.6	V
Reverse Recovery Time	$V_{GS} = 0\text{ V}, V_{DD} = 30\text{ V}$ $I_S = 3.0\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	t_{rr}		265		ns
Reverse Recovery Charge		Q_{rr}		0.9		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Width $\leq 380\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

6. Guaranteed by design.

NDF03N60Z, NDD03N60Z

TYPICAL CHARACTERISTICS

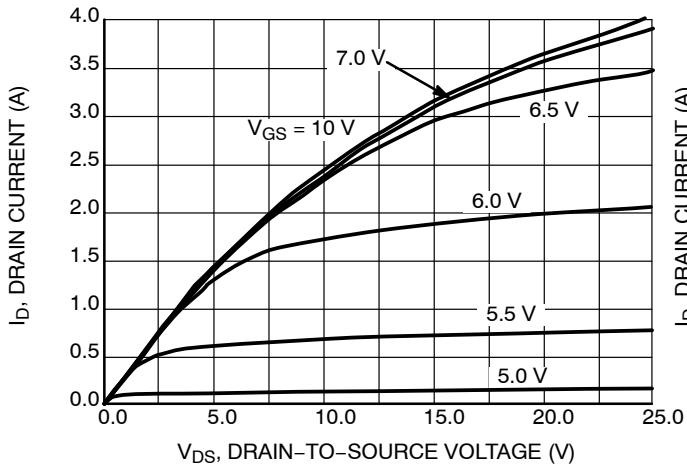


Figure 1. On-Region Characteristics

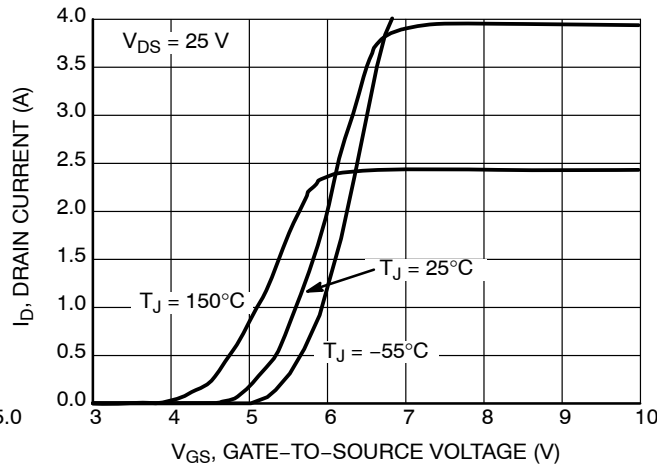


Figure 2. Transfer Characteristics

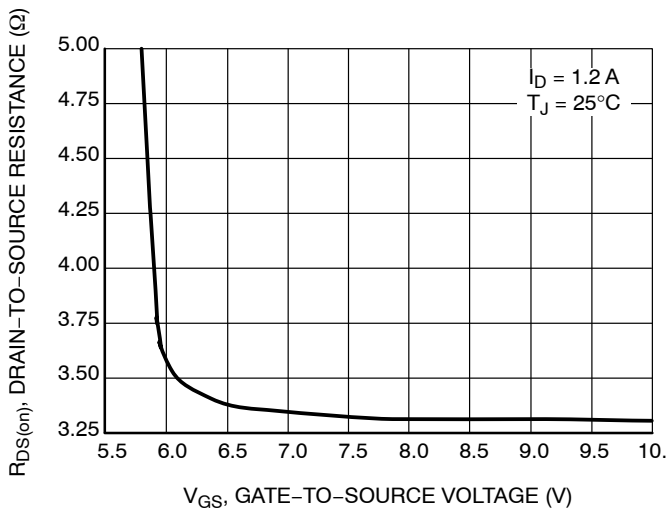


Figure 3. On-Region versus Gate-to-Source Voltage

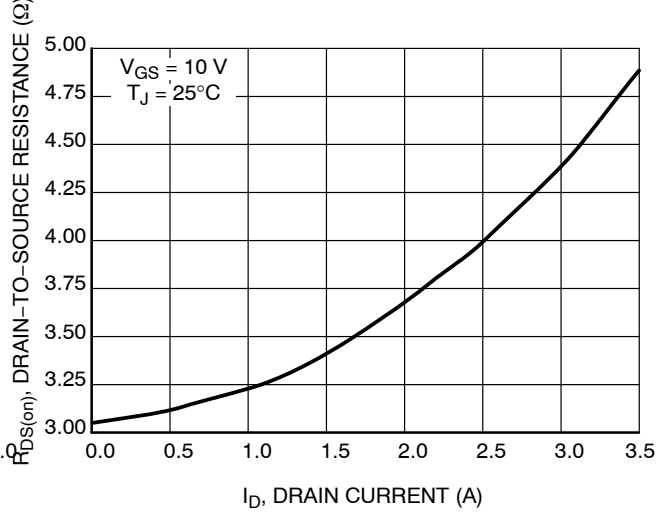


Figure 4. On-Resistance versus Drain Current and Gate Voltage

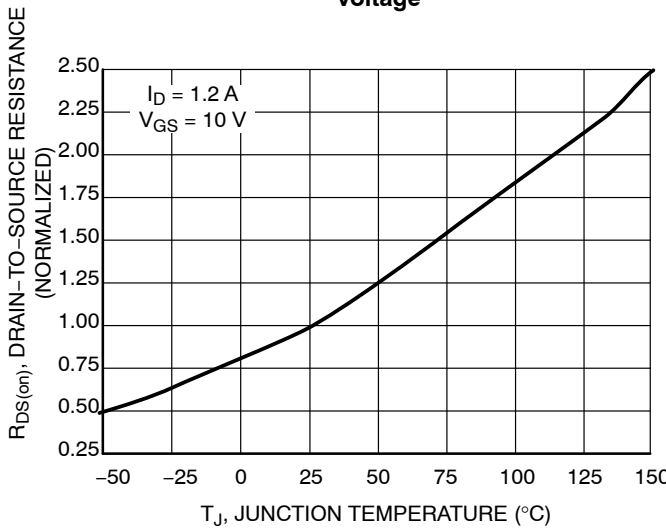


Figure 5. On-Resistance Variation with Temperature

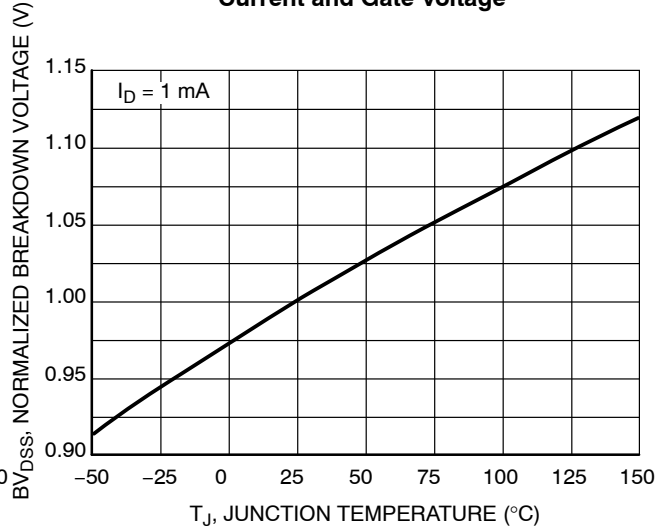


Figure 6. BV_{DSS} Variation with Temperature

NDF03N60Z, NDD03N60Z

TYPICAL CHARACTERISTICS

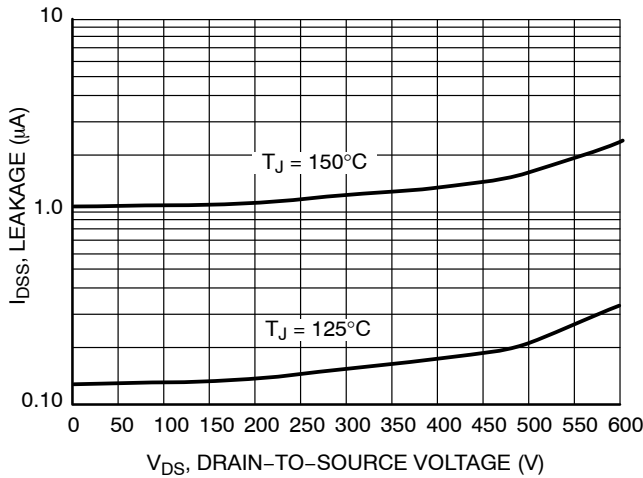


Figure 7. Drain-to-Source Leakage Current versus Voltage

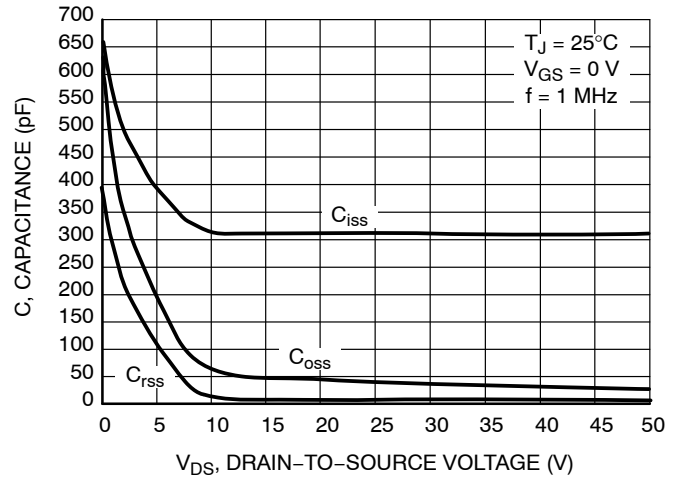


Figure 8. Capacitance Variation

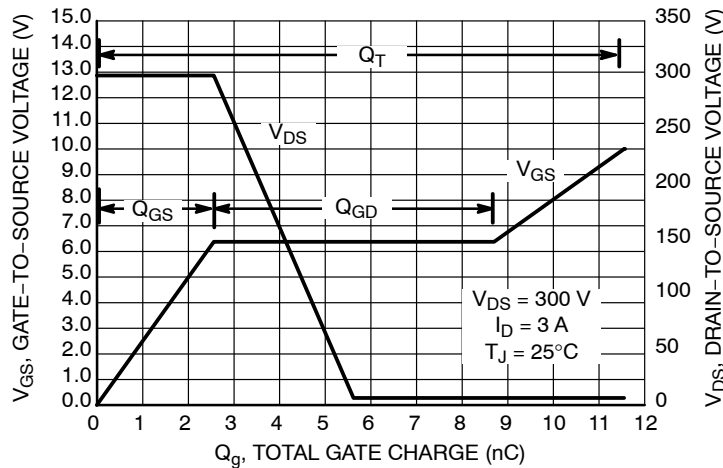


Figure 9. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge

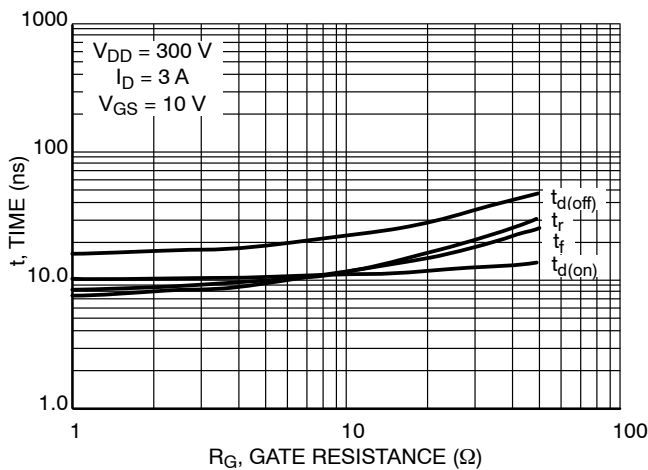


Figure 10. Resistive Switching Time Variation versus Gate Resistance

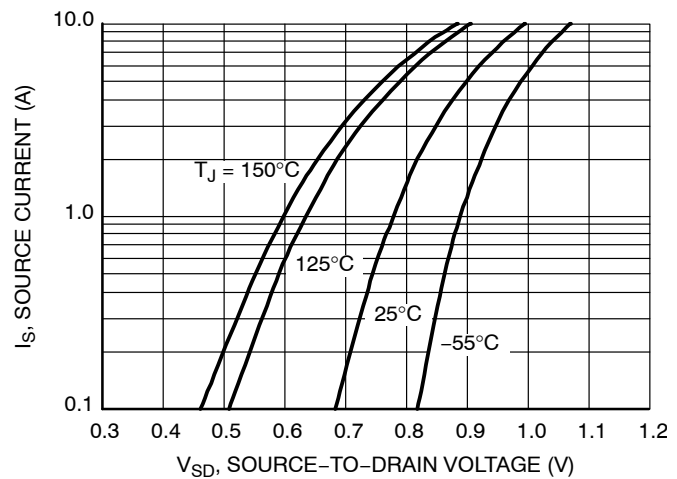


Figure 11. Diode Forward Voltage versus Current

NDF03N60Z, NDD03N60Z

TYPICAL CHARACTERISTICS

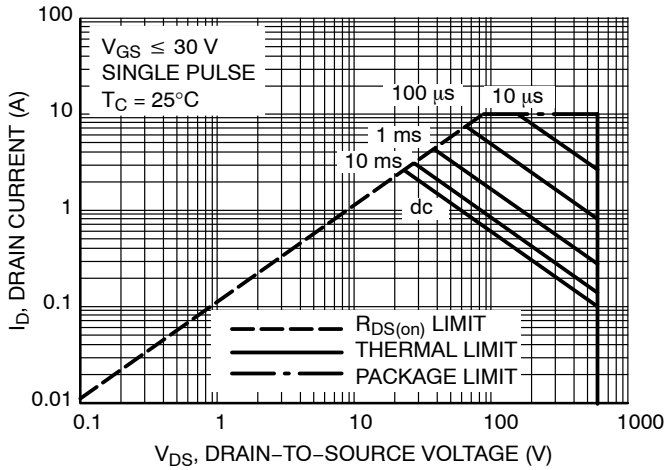


Figure 12. Maximum Rated Forward Biased Safe Operating Area NDD03N60Z

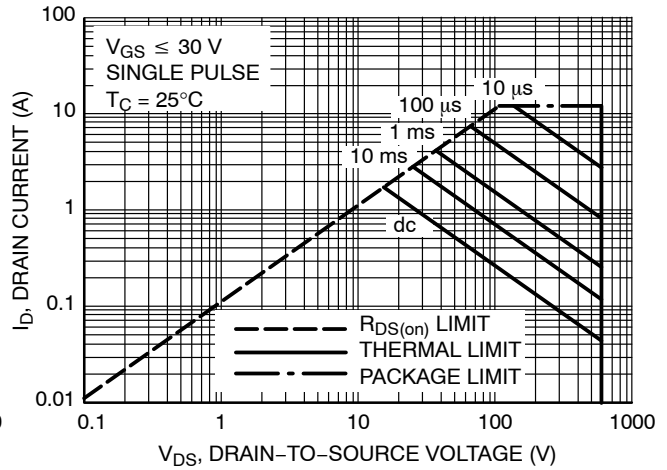


Figure 13. Maximum Rated Forward Biased Safe Operating Area NDF03N60Z

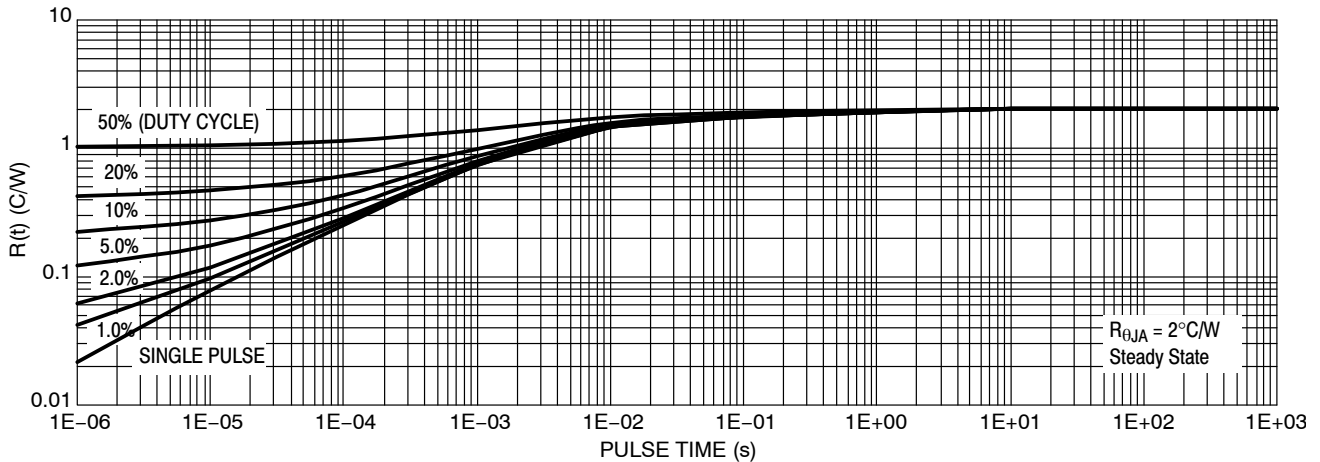


Figure 14. Thermal Impedance (Junction-to-Case) for NDD03N60Z

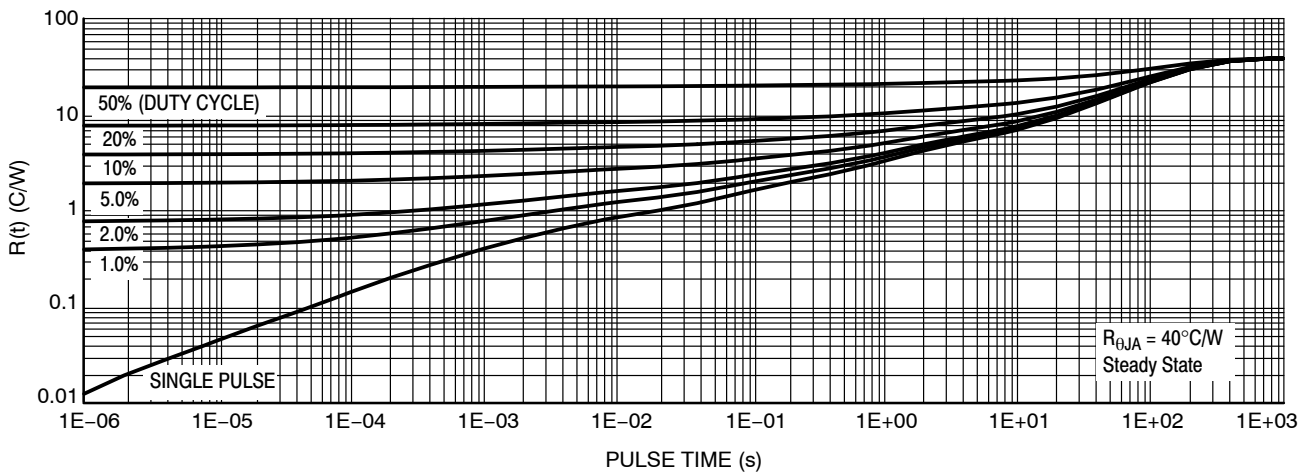


Figure 15. Thermal Impedance (Junction-to-Ambient) for NDD03N60Z

NDF03N60Z, NDD03N60Z

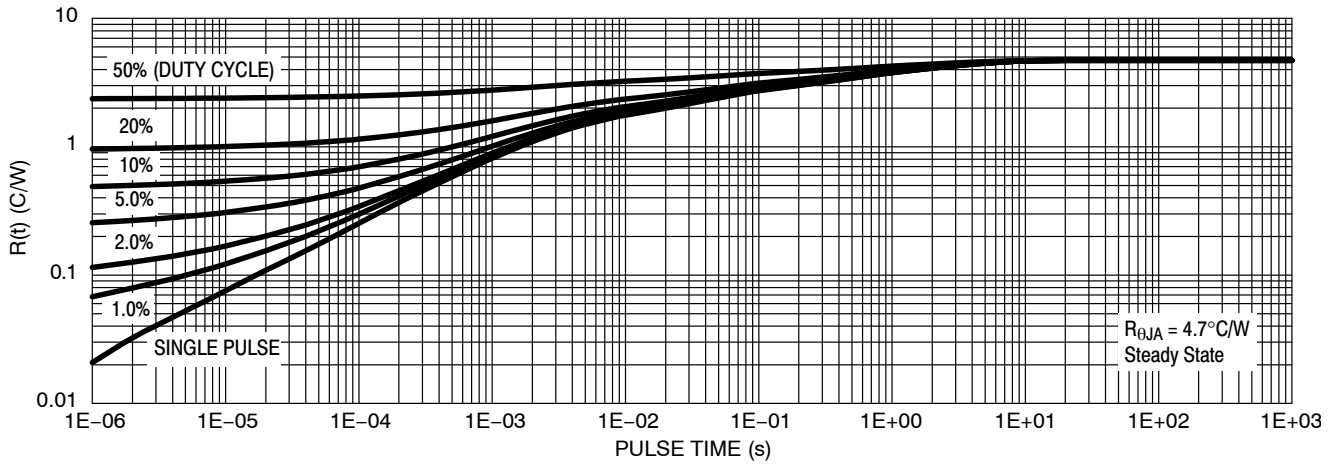


Figure 16. Thermal Impedance (Junction-to-Case) for NDF03N60Z

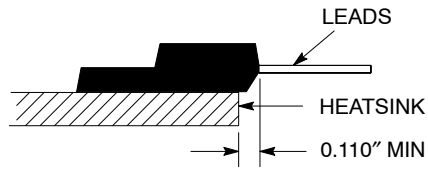


Figure 17. Isolation Test Diagram

Measurement made between leads and heatsink with all leads shorted together.

*For additional mounting information, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MECHANICAL CASE OUTLINE

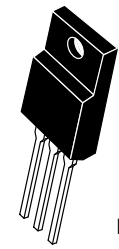
PACKAGE DIMENSIONS

ON Semiconductor®

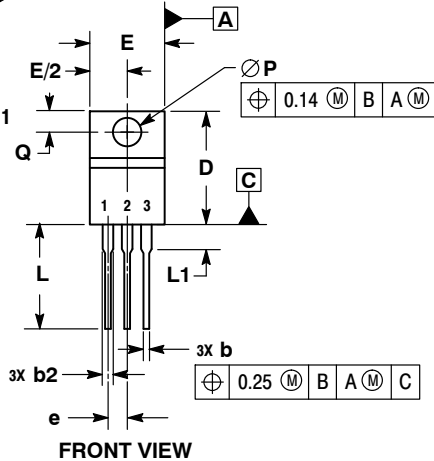


TO-220 FULLPACK, 3-LEAD CASE 221AH ISSUE F

DATE 30 SEP 2014



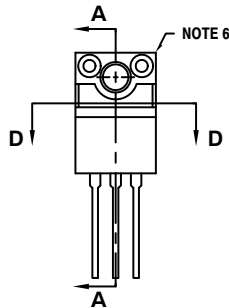
SCALE 1:1



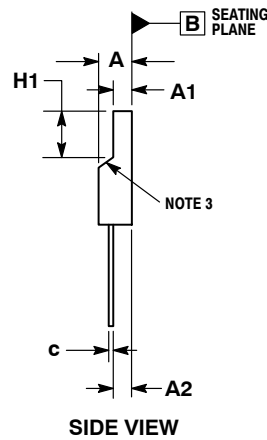
FRONT VIEW



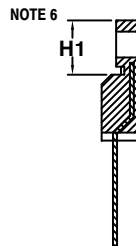
SECTION D-D



ALTERNATE CONSTRUCTION



SIDE VIEW



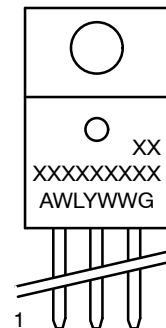
SECTION A-A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR UNCONTROLLED IN THIS AREA.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH AND GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.13 PER SIDE. THESE DIMENSIONS ARE TO BE MEASURED AT OUTERMOST EXTREME OF THE PLASTIC BODY.
5. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 2.00.
6. CONTOURS AND FEATURES OF THE MOLDED PACKAGE BODY MAY VARY WITHIN THE ENVELOPE DEFINED BY DIMENSIONS A1 AND H1 FOR MANUFACTURING PURPOSES.

MILLIMETERS		
DIM	MIN	MAX
A	4.30	4.70
A1	2.50	2.90
A2	2.50	2.90
b	0.54	0.84
b2	1.10	1.40
c	0.49	0.79
D	14.70	15.30
E	9.70	10.30
e	2.54 BSC	
H1	6.60	7.10
L	12.50	14.73
L1	---	2.80
P	3.00	3.40
Q	2.80	3.20

GENERIC MARKING DIAGRAM*



- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLE 1:

1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE

STYLE 2:

1. CATHODE
2. ANODE
3. GATE

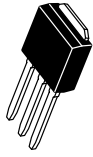
DOCUMENT NUMBER:	98AON52577E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TO-220 FULLPACK, 3-LEAD	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

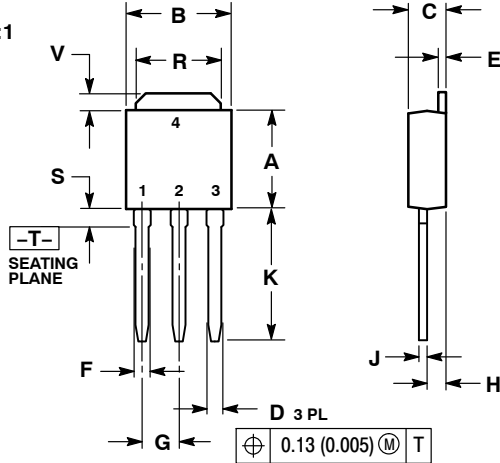
ON Semiconductor®



IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010

SCALE 1:1



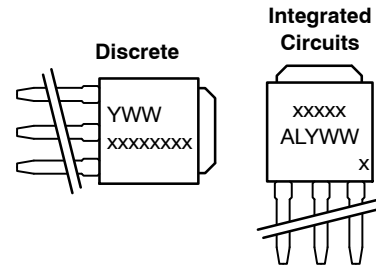
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- | | | | |
|--|---|--|--|
| <p>STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | <p>STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN</p> | <p>STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE</p> | <p>STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE</p> |
| <p>STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE</p> | <p>STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2</p> | <p>STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | |

MARKING DIAGRAMS



- xxxxxxxx = Device Code
- A = Assembly Location
- IL = Wafer Lot
- Y = Year
- WW = Work Week

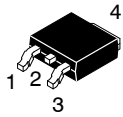
DOCUMENT NUMBER:	98AON10528D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	IPAK (DPAK INSERTION MOUNT)	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



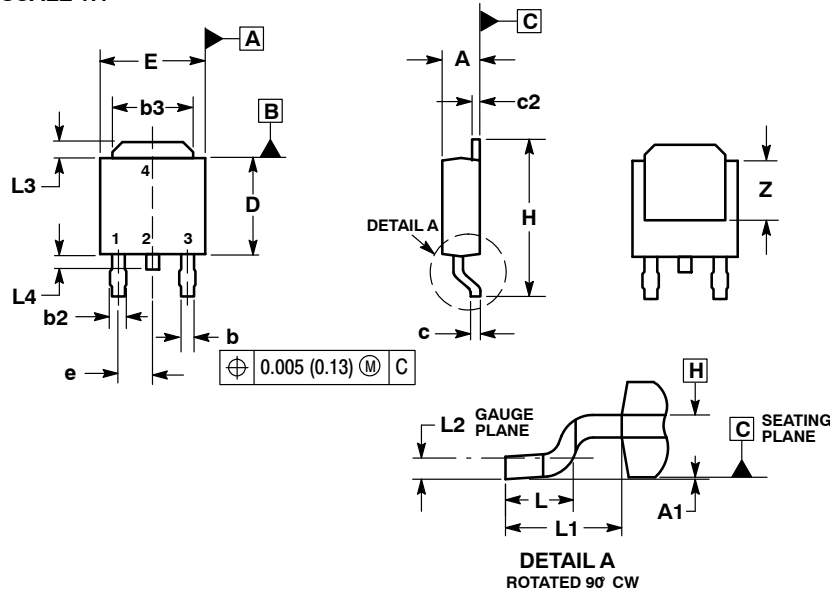
SCALE 1:1

DPAK (SINGLE GAUGE)

CASE 369AA-01

ISSUE B

DATE 03 JUN 2010



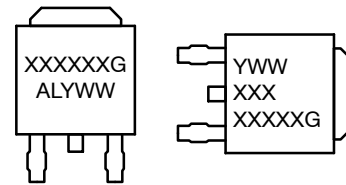
NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

- | | | | |
|--|---|--|--|
| <p>STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | <p>STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN</p> | <p>STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE</p> | <p>STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE</p> |
| <p>STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE</p> | <p>STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2</p> | <p>STYLE 7:
PIN 1. GATE
2. ANODE
3. EMITTER
4. COLLECTOR</p> | |

GENERIC MARKING DIAGRAM*

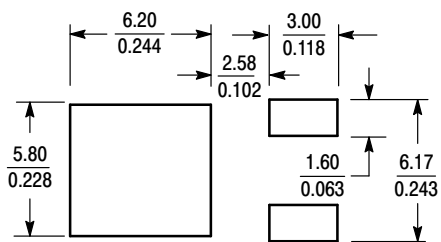


IC Discrete

- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*



SCALE 3:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON13126D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

