

# NDDL01N60Z, NDTL01N60Z

## N-Channel Power MOSFET 600 V, 15 $\Omega$

### Features

- 100% Avalanche Tested
- Gate Charge Minimized
- Zener-protected
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### ABSOLUTE MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	NDD	NDT	Unit
Drain-to-Source Voltage	$V_{DSS}$	600		V
Gate-to-Source Voltage	$V_{GS}$	$\pm 30$		V
Continuous Drain Current Steady State, $T_C = 25^\circ\text{C}$ (Note 1)	$I_D$	0.8	0.25	A
Continuous Drain Current Steady State, $T_C = 100^\circ\text{C}$ (Note 1)	$I_D$	0.5	0.15	A
Power Dissipation Steady State, $T_C = 25^\circ\text{C}$	$P_D$	26	2	W
Pulsed Drain Current, $t_p = 10 \mu\text{s}$	$I_{DM}$	3.4		A
Source Current (Body Diode)	$I_S$	2.5	1.7	A
Single Pulse Drain-to-Source Avalanche Energy ( $I_D = 0.8 \text{ A}$ )	EAS	12		mJ
Peak Diode Recovery (Note 2)	$dv/dt$	4.5		V/ns
Lead Temperature for Soldering Leads	$T_L$	260		$^\circ\text{C}$
Operating Junction and Storage Temperature	$T_J, T_{STG}$	-55 to +150		$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Limited by maximum junction temperature
2.  $I_S = 1.5 \text{ A}$ ,  $di/dt \leq 100 \text{ A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$

### THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain) NDDL1N60Z	$R_{\theta JC}$	4.8	$^\circ\text{C}/\text{W}$
Junction-to-Ambient (Note 4) NDDL1N60Z (Note 3) NDDL1N60Z-1 (Note 4) NDTL1N60Z (Note 5) NDTL1N60Z	$R_{\theta JA}$	42 96 62 151	$^\circ\text{C}/\text{W}$

3. Insertion mounted.
4. Surface-mounted on FR4 board using 1" sq. pad size (Cu area = 1.127" sq. [2 oz] including traces).
5. Surface-mounted on FR4 board using minimum recommended pad size (Cu area = 0.026" sq. [2 oz]).

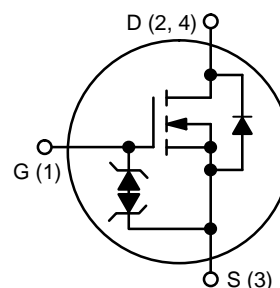


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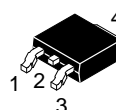
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$V_{(BR)DSS}$	$R_{DS(ON) MAX}$
600 V	15 $\Omega$ @ 10 V

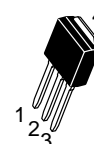
### N-Channel MOSFET



SOT-223  
CASE 318E  
STYLE 3



DPAK  
CASE 369C  
STYLE 2



IPAK  
CASE 369D  
STYLE 2

### MARKING & ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 3 of this data sheet.

# NDDL01N60Z, NDTL01N60Z

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA	600			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>	Reference to 25°C, I <sub>D</sub> = 1 mA		610		mV/°C
Drain-to-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V	T <sub>J</sub> = 25°C		1	μA
			T <sub>J</sub> = 125°C		50	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V			±100	nA

### ON CHARACTERISTICS (Note 6)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 50 μA	3	4.0	4.5	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			9.6		mV/°C
Static Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.4 A		12.2	15	Ω
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 0.4 A		0.7		S

### CHARGES, CAPACITANCES & GATE RESISTANCES

Input Capacitance (Note 7)	C <sub>iSS</sub>	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz		92		pF
Output Capacitance (Note 7)	C <sub>oSS</sub>			13		
Reverse Transfer Capacitance (Note 7)	C <sub>rSS</sub>			3		
Effective output capacitance, energy related (Note 9)	C <sub>o(er)</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 0 to 480 V		5.5		pF
Effective output capacitance, time related (Note 10)	C <sub>o(tr)</sub>	I <sub>D</sub> = constant, V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 0 to 480 V		8.1		
Total Gate Charge (Note 7)	Q <sub>g</sub>	V <sub>DS</sub> = 300 V, I <sub>D</sub> = 0.4 A, V <sub>GS</sub> = 10 V		4.9		nC
Gate-to-Source Charge (Note 7)	Q <sub>gs</sub>			1.2		
Gate-to-Drain Charge (Note 7)	Q <sub>gd</sub>			2.4		
Plateau Voltage	V <sub>GP</sub>			5.8		V
Gate Resistance	R <sub>g</sub>			6.6		Ω

### SWITCHING CHARACTERISTICS (Note 8)

Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 0.4 A, V <sub>GS</sub> = 10 V, R <sub>G</sub> = 0 Ω		10		ns
Rise Time	t <sub>r</sub>			5		
Turn-off Delay Time	t <sub>d(off)</sub>			13		
Fall Time	t <sub>f</sub>			18		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = 0.4 A, V <sub>GS</sub> = 0 V	T <sub>J</sub> = 25°C		0.8	1.2	V
			T <sub>J</sub> = 100°C		0.7		
Reverse Recovery Time	t <sub>rr</sub>	V <sub>GS</sub> = 0 V, V <sub>DD</sub> = 30 V, I <sub>S</sub> = 1 A, d <sub>i</sub> /d <sub>t</sub> = 100 A/μs		183		ns	
Charge Time	t <sub>a</sub>			33			
Discharge Time	t <sub>b</sub>			150			
Reverse Recovery Charge	Q <sub>rr</sub>			255			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

7. Guaranteed by design.

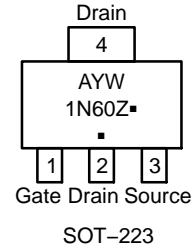
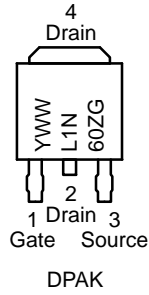
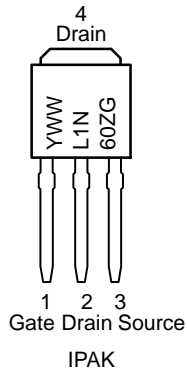
8. Switching characteristics are independent of operating junction temperatures.

9. C<sub>o(er)</sub> is a fixed capacitance that gives the same stored energy as C<sub>oSS</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>(BR)DSS</sub>

10. C<sub>o(tr)</sub> is a fixed capacitance that gives the same charging time as C<sub>oSS</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>(BR)DSS</sub>

# NDDL01N60Z, NDTL01N60Z

## MARKING DIAGRAMS



A = Assembly Location  
 Y = Year  
 W, WW = Work Week  
 L1N60Z, 1N60Z = Specific Device Codes  
 G or ■ = Pb-Free Package

(\*Note: Microdot may be in either location)

## ORDERING INFORMATION

Device	Package	Shipping†
NDDL01N60Z-1G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rail
NDDL01N60ZT4G	DPAK (Pb-Free, Halogen-Free)	2500 / Tape & Reel
NDTL01N60ZT1G	SOT-223 (Pb-Free, Halogen-Free)	1000 / Tape & Reel
NDTL01N60ZT3G	SOT-223 (Pb-Free, Halogen-Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

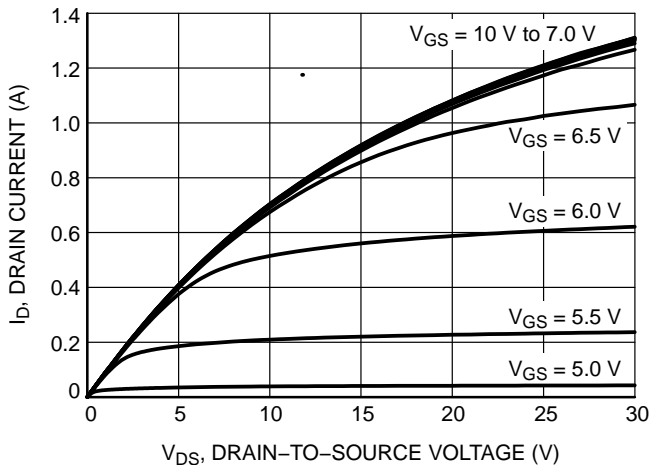


Figure 1. On-Region Characteristics

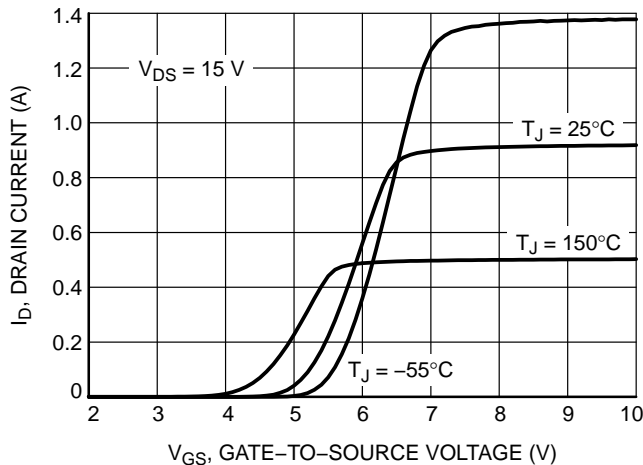


Figure 2. Transfer Characteristics

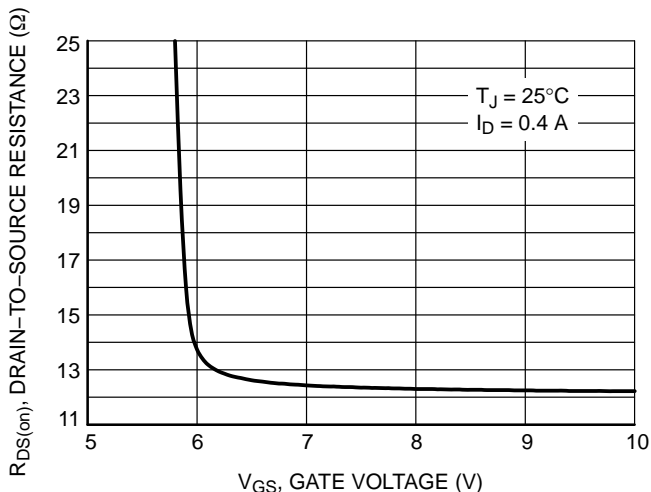


Figure 3. On-Resistance vs. Gate-to-Source Voltage

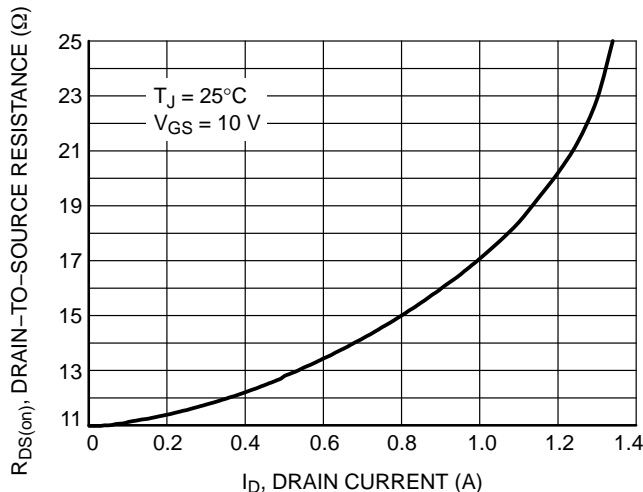


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

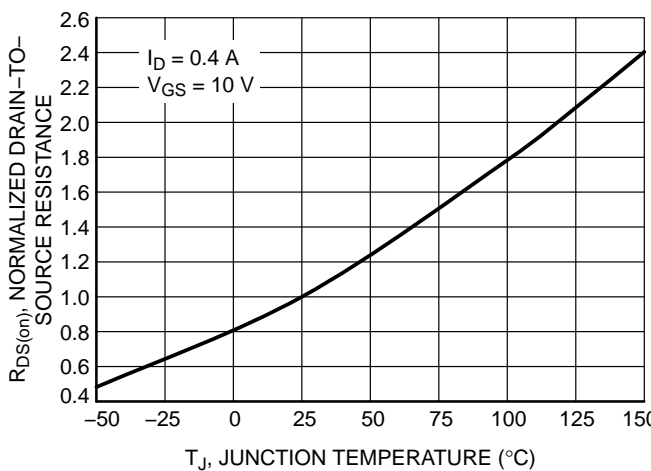


Figure 5. On-Resistance Variation with Temperature

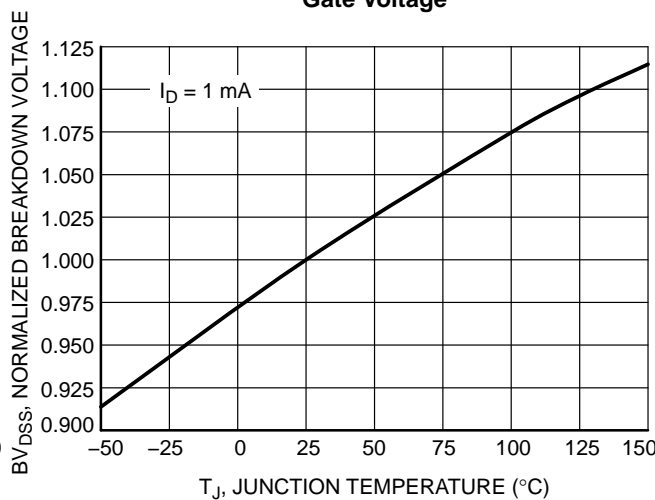
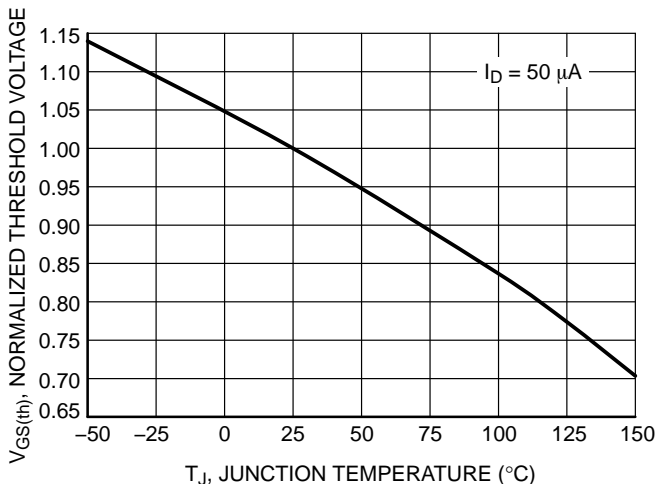


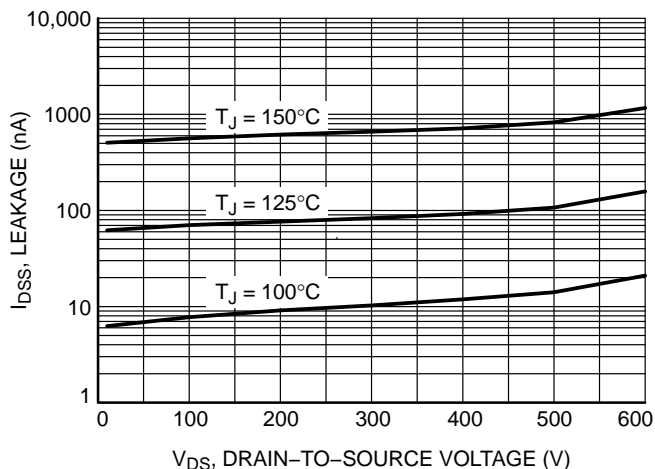
Figure 6. Breakdown Voltage Variation with Temperature

# NDDL01N60Z, NDTL01N60Z

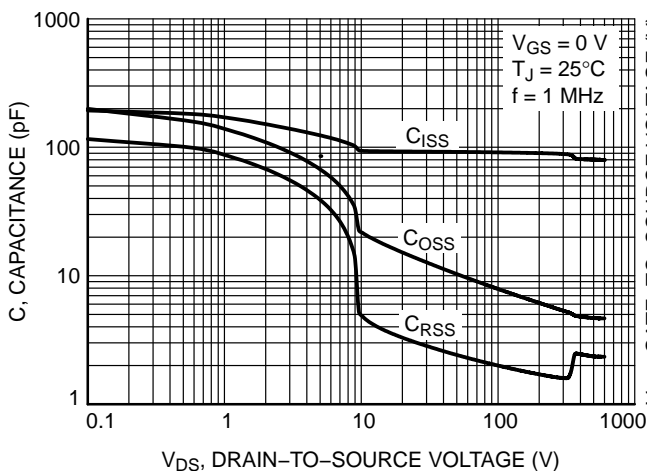
## TYPICAL CHARACTERISTICS



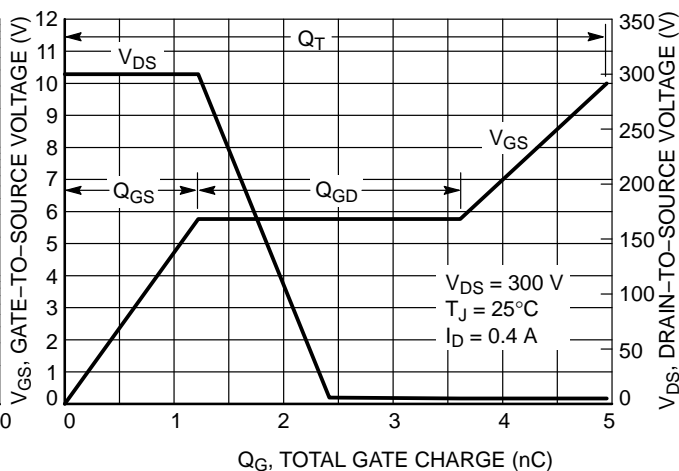
**Figure 7. Threshold Voltage Variation with Temperature**



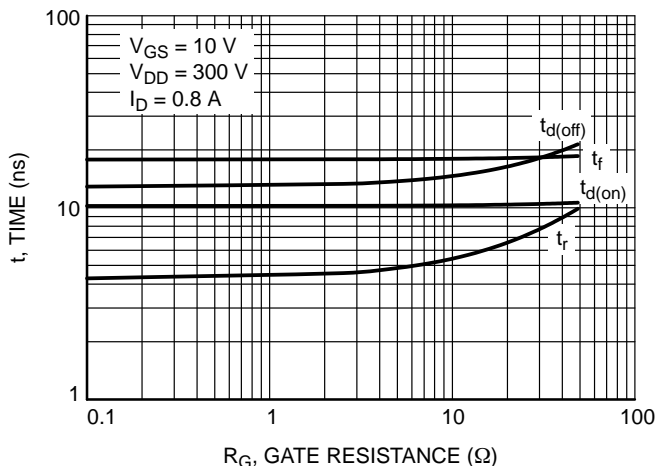
**Figure 8. Drain-to-Source Leakage Current vs. Voltage**



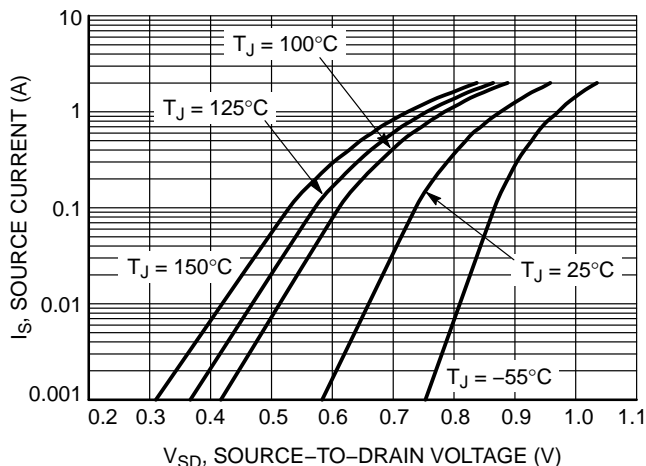
**Figure 9. Capacitance Variation**



**Figure 10. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**



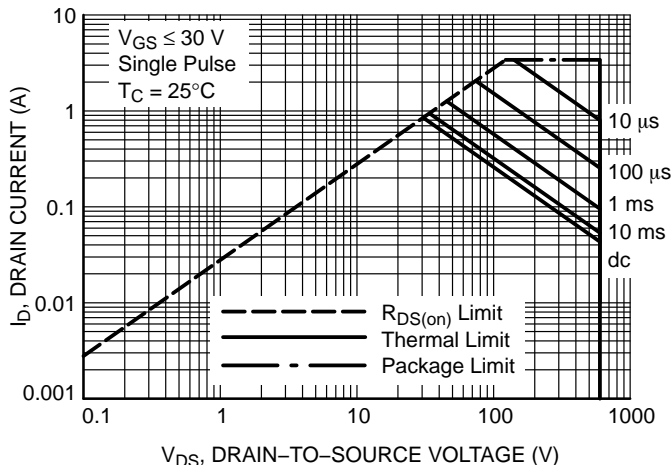
**Figure 11. Resistive Switching Time Variation vs. Gate Resistance**



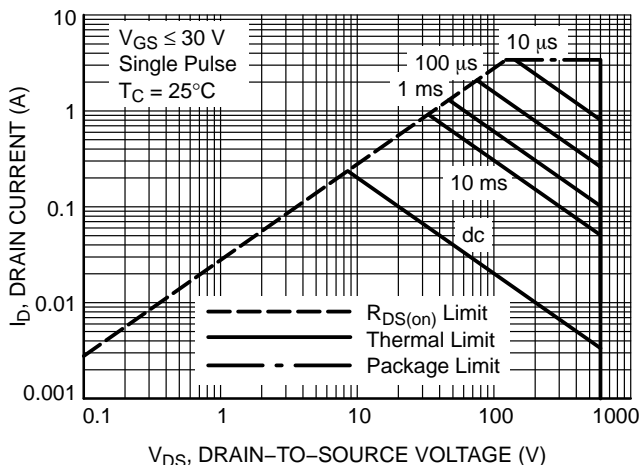
**Figure 12. Diode Forward Voltage vs. Current**

# NDDL01N60Z, NDTL01N60Z

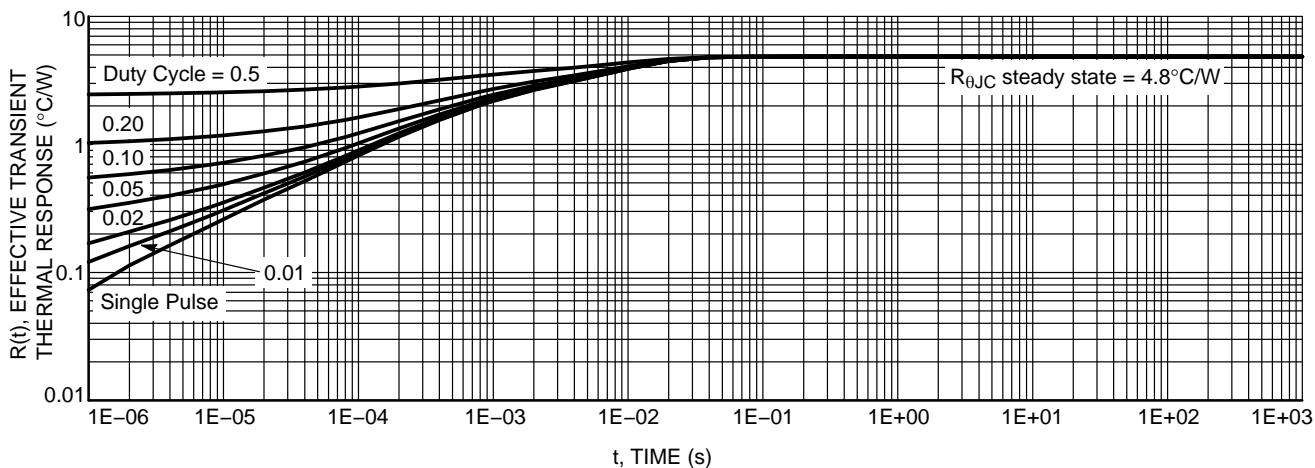
## TYPICAL CHARACTERISTICS



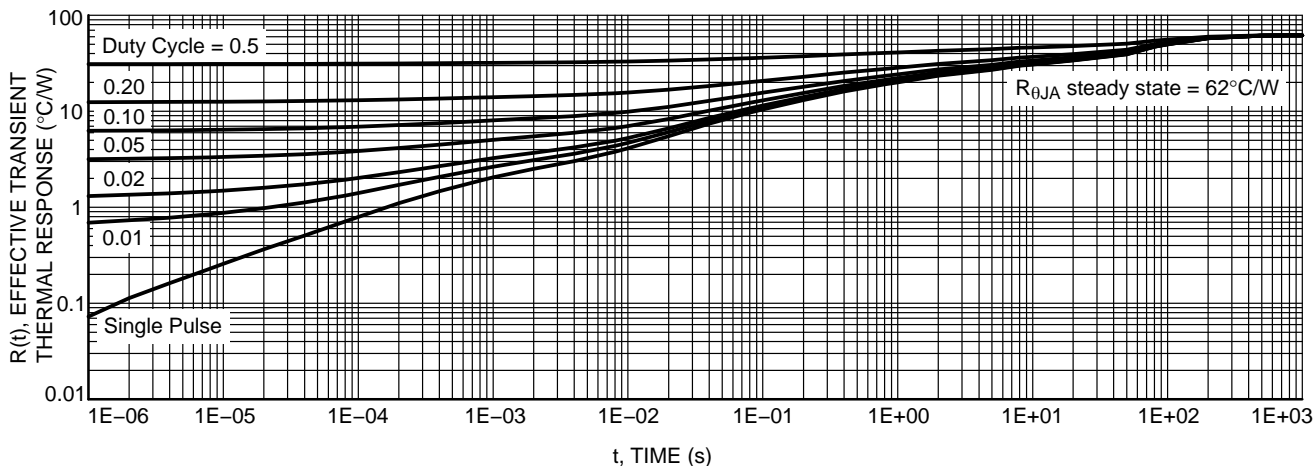
**Figure 13. Maximum Rated Forward Biased Safe Operating Area for NDDL01N60Z**



**Figure 14. Maximum Rated Forward Biased Safe Operating Area for NDTL01N60Z**



**Figure 15. Thermal Impedance (Junction-to-Case) for NDDL01N60Z**



**Figure 16. Thermal Impedance (Junction-to-Ambient) for NDTL01N60Z**

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

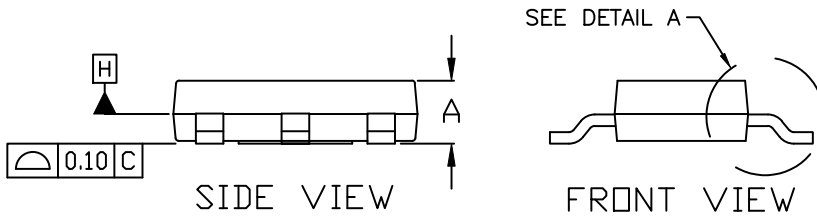
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SCALE 1:1

SOT-223 (TO-261)  
CASE 318E-04  
ISSUE R

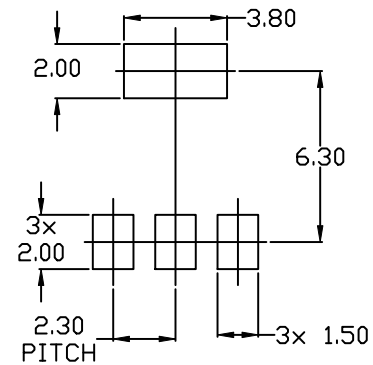
DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
$\theta$	0°	---	10°



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<b>DESCRIPTION:</b>	<b>SOT-223 (TO-261)</b>	<b>PAGE 1 OF 2</b>

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**SOT-223 (TO-261)**  
**CASE 318E-04**  
**ISSUE R**

DATE 02 OCT 2018

- |  |   |   |   |   |
|--|---|---|---|---|
| <b>STYLE 1:</b><br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 2:</b><br>PIN 1. ANODE<br>2. CATHODE<br>3. NC<br>4. CATHODE        | <b>STYLE 3:</b><br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN           | <b>STYLE 4:</b><br>PIN 1. SOURCE<br>2. DRAIN<br>3. GATE<br>4. DRAIN   | <b>STYLE 5:</b><br>PIN 1. DRAIN<br>2. GATE<br>3. SOURCE<br>4. GATE    |
| <b>STYLE 6:</b><br>PIN 1. RETURN<br>2. INPUT<br>3. OUTPUT<br>4. INPUT        | <b>STYLE 7:</b><br>PIN 1. ANODE 1<br>2. CATHODE<br>3. ANODE 2<br>4. CATHODE | <b>STYLE 8:</b><br>CANCELLED  | <b>STYLE 9:</b><br>PIN 1. INPUT<br>2. GROUND<br>3. LOGIC<br>4. GROUND | <b>STYLE 10:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE<br>4. ANODE |
| <b>STYLE 11:</b><br>PIN 1. MT 1<br>2. MT 2<br>3. GATE<br>4. MT 2             | <b>STYLE 12:</b><br>PIN 1. INPUT<br>2. OUTPUT<br>3. NC<br>4. OUTPUT         | <b>STYLE 13:</b><br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR |   |   |

**GENERIC  
 MARKING DIAGRAM\***



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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<b>DESCRIPTION:</b>	<b>SOT-223 (TO-261)</b>	<b>PAGE 2 OF 2</b>

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# MECHANICAL CASE OUTLINE

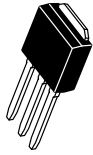
## PACKAGE DIMENSIONS

ON Semiconductor®

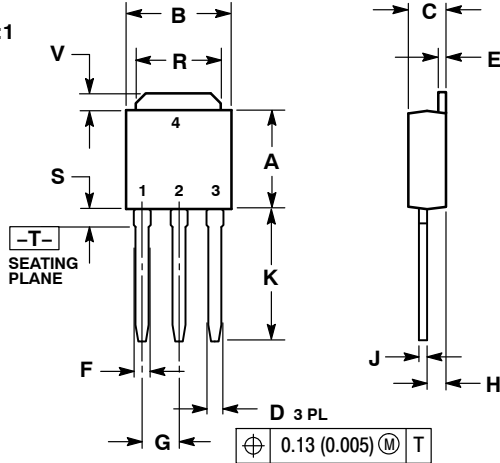


### IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010



SCALE 1:1

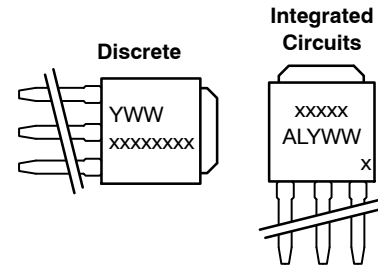


- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- |  |   |  |  |
|--|---|--|--|
| <p>STYLE 1:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 2:<br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p> | <p>STYLE 3:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>      | <p>STYLE 4:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p> |
| <p>STYLE 5:<br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p>         | <p>STYLE 6:<br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>        | <p>STYLE 7:<br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> |  |

### MARKING DIAGRAMS

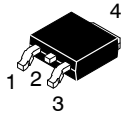


- xxxxxxxx = Device Code  
 A = Assembly Location  
 IL = Wafer Lot  
 Y = Year  
 WW = Work Week

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<b>DESCRIPTION:</b>	<b>IPAK (DPAK INSERTION MOUNT)</b>	<b>PAGE 1 OF 1</b>

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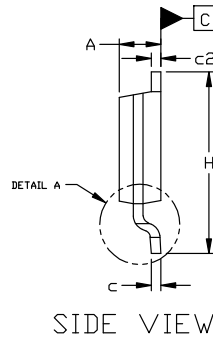
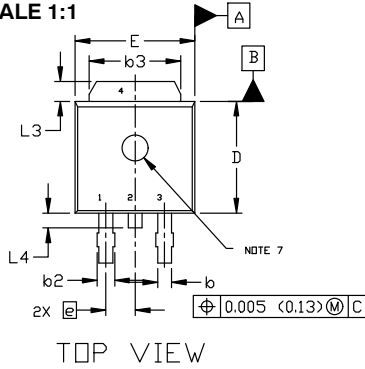
**MECHANICAL CASE OUTLINE  
PACKAGE DIMENSIONS**



**DPAK (SINGLE GAUGE)  
CASE 369C  
ISSUE G**

DATE 31 MAY 2023

SCALE 1:1



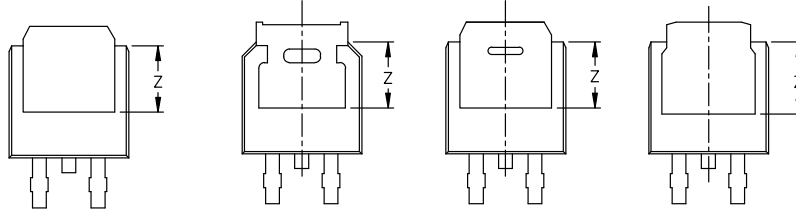
NOTES:

- DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
- OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	----	0.040	---	1.01
Z	0.155	----	3.93	---

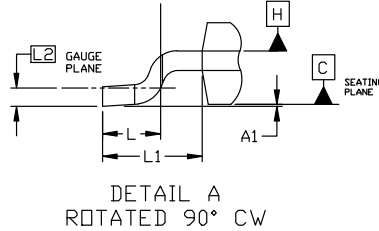
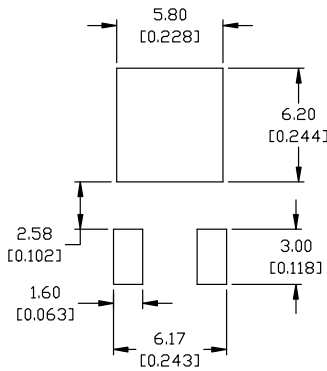
TOP VIEW

SIDE VIEW

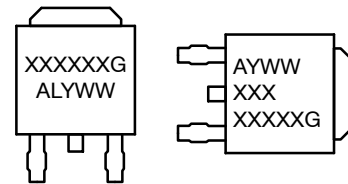


BOTTOM VIEW

BOTTOM VIEW



**GENERIC MARKING DIAGRAM\***



- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

**RECOMMENDED MOUNTING FOOTPRINT\***

\*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

- STYLE 1: PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR
- STYLE 2: PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN
- STYLE 3: PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. CATHODE
- STYLE 4: PIN 1. CATHODE  
2. ANODE  
3. GATE  
4. ANODE
- STYLE 5: PIN 1. GATE  
2. ANODE  
3. CATHODE  
4. ANODE
- STYLE 6: PIN 1. MT1  
2. MT2  
3. GATE  
4. MT2
- STYLE 7: PIN 1. GATE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR
- STYLE 8: PIN 1. N/C  
2. CATHODE  
3. ANODE  
4. CATHODE
- STYLE 9: PIN 1. ANODE  
2. CATHODE  
3. RESISTOR ADJUST  
4. CATHODE
- STYLE 10: PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. ANODE

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DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

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