

NDD02N40, NDT02N40

N-Channel Power MOSFET 400 V, 5.5 Ω

Features

- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	NDD	NDT	Unit
Drain-to-Source Voltage	V _{DSS}	400		V
Gate-to-Source Voltage	V _{GS}	±20		V
Continuous Drain Current R _{θJC} Steady State, T _C = 25°C (Note 1)	I _D	1.7	0.4	A
Continuous Drain Current R _{θJC} Steady State, T _C = 100°C (Note 1)	I _D	1.1	0.25	A
Power Dissipation – R _{θJC} Steady State, T _C = 25°C	P _D	39	2.0	W
Pulsed Drain Current	I _{DM}	6.9	1.6	A
Continuous Source Current (Body Diode)	I _S	1.7	0.4	A
Single Pulse Drain-to-Source Avalanche Energy, I _D = 1 A	EAS	120		mJ
Maximum Temperature for Soldering Leads	T _L	260		°C
Operating Junction and Storage Temperature	T _J , T _{STG}	-55 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Limited by maximum junction temperature
2. I_S = 1.7 A, di/dt ≤ 100 A/μs, V_{DD} ≤ BV_{DSS}, T_J = +150°C

THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	R _{θJC}	3.2	°C/W
Junction-to-Ambient Steady State	R _{θJA}		°C/W
NDD02N40 (Note 4)		39	
NDD02N40-1 (Note 3)		96	
NDT02N40 (Note 4)		62	
NDT02N40 (Note 5)		151	

3. Insertion mounted
4. Surface mounted on FR4 board using 1" sq. pad size (Cu area = 1.127" sq. [2 oz] including traces)
5. Surface-mounted on FR4 board using minimum recommended pad size (Cu area = 0.026" sq. [2 oz]).

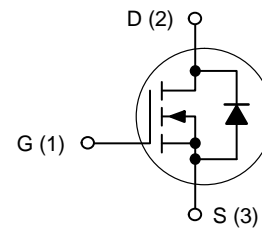


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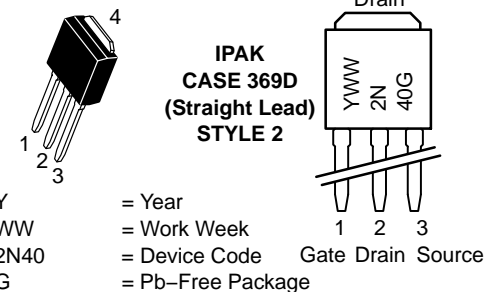
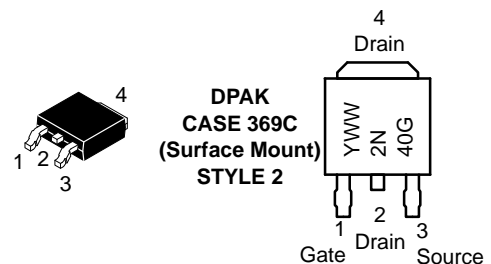
<http://onsemi.com>

V _{(BR)DSS}	R _{DS(ON)} MAX
400 V	5.5 Ω @ 10 V

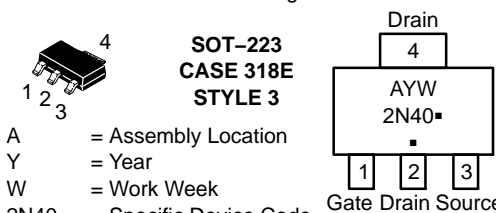
N-Channel MOSFET



MARKING DIAGRAMS



Y = Year
 WW = Work Week
 2N40 = Device Code
 G = Pb-Free Package



A = Assembly Location
 Y = Year
 W = Work Week
 2N40 = Specific Device Code
 ■ = Pb-Free Package

(*Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

NDD02N40, NDT02N40

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 1 mA	400			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	Reference to 25°C, I _D = 1 mA		460		mV/°C
Drain-to-Source Leakage Current	I _{DSS}	V _{DS} = 400 V, V _{GS} = 0 V	T _J = 25°C		1	μA
			T _J = 125°C		50	
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} = ±20 V			±10	μA

ON CHARACTERISTICS (Note 6)

Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 250 μA	0.8	1.6	2	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J	Reference to 25°C, I _D = 50 μA		4.6		mV/°C
Static Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 0.22 A		4.5	5.5	Ω
Forward Transconductance	g _{FS}	V _{DS} = 15 V, I _D = 0.22 A		1.1		S

DYNAMIC CHARACTERISTICS

Input Capacitance (Note 7)	C _{iss}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz		121		pF
Output Capacitance (Note 7)	C _{oss}			16		
Reverse Transfer Capacitance (Note 7)	C _{rss}			3		
Total Gate Charge (Note 7)	Q _g	V _{DS} = 200 V, I _D = 1.7 A, V _{GS} = 10 V		5.5		nC
Gate-to-Source Charge (Note 7)	Q _{gs}			0.8		
Gate-to-Drain ("Miller") Charge (Note 7)	Q _{gd}			1.0		
Plateau Voltage	V _{GP}			3.1		
Gate Resistance	R _g			8.7		Ω

RESISTIVE SWITCHING CHARACTERISTICS (Note 8)

Turn-on Delay Time	t _{d(on)}	V _{DD} = 200 V, I _D = 1.7 A, V _{GS} = 10 V, R _G = 0 Ω		5		ns
Rise Time	t _r			7		
Turn-off Delay Time	t _{d(off)}			14		
Fall Time	t _f			4		

SOURCE-DRAIN DIODE CHARACTERISTICS

Diode Forward Voltage	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V	T _J = 25°C		0.9	1.6	V
			T _J = 100°C		0.8		
Reverse Recovery Time	t _{rr}	V _{GS} = 0 V, V _{DD} = 30 V, I _S = 1.7 A, d _i /d _t = 100 A/μs		146		ns	
Charge Time	t _a			37			
Discharge Time	t _b			109			
Reverse Recovery Charge	Q _{rr}			260			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Pulse Width ≤ 380 μs, Duty Cycle ≤ 2%.

7. Guaranteed by design.

8. Switching characteristics are independent of operating junction temperatures.

NDD02N40, NDT02N40

ORDERING INFORMATION

Device	Package	Shipping†
NDD02N40-1G	IPAK (Pb-Free, Halogen Free)	75 Units / Rail
NDD02N40T4G	DPAK (Pb-Free, Halogen Free)	2500 / Tape & Reel
NDT02N40T1G	SOT-223 (Pb-Free, Halogen Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NDD02N40, NDT02N40

TYPICAL CHARACTERISTICS

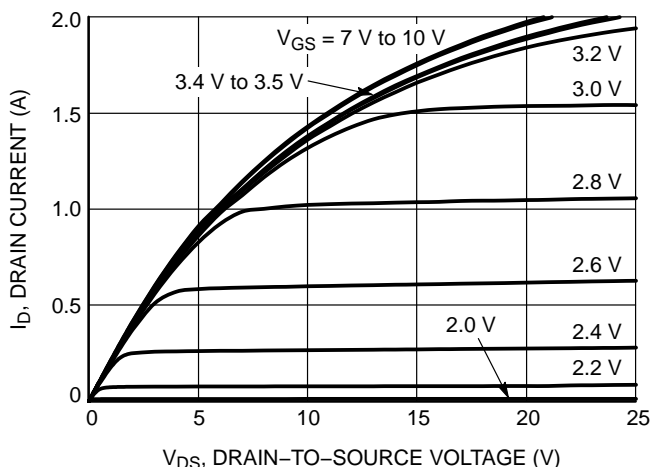


Figure 1. On-Region Characteristics

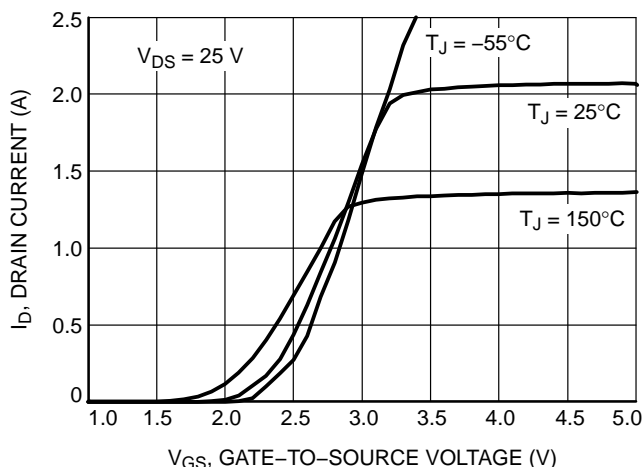


Figure 2. Transfer Characteristics

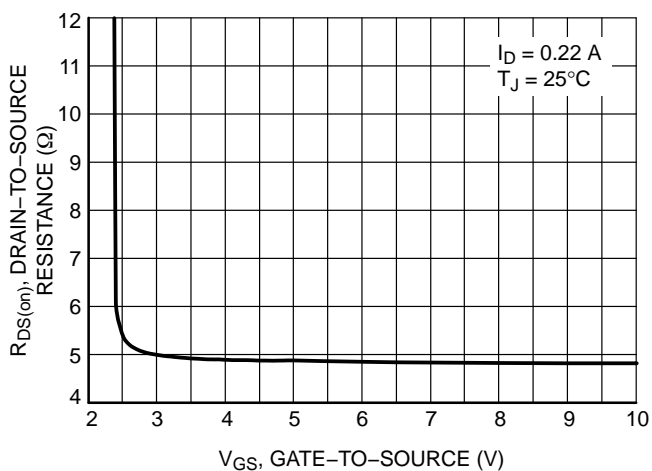


Figure 3. On-Resistance vs. Gate-to-Source Voltage

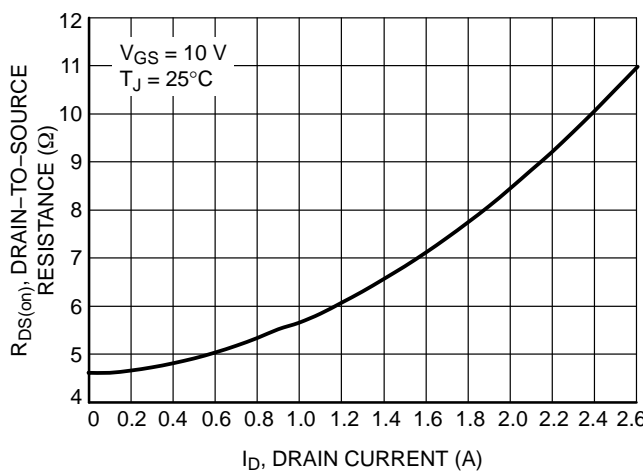


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

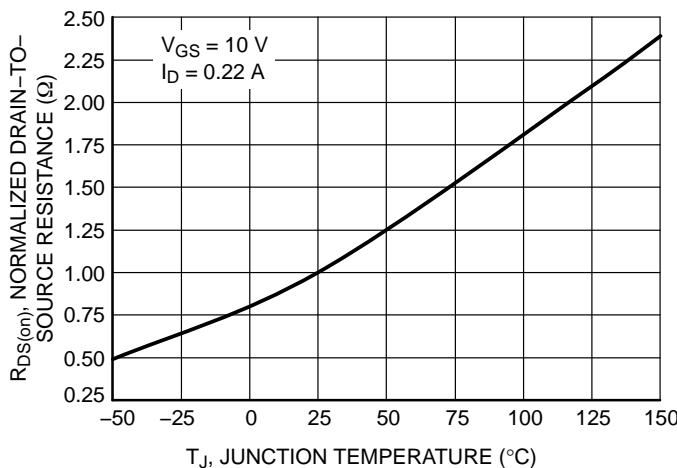


Figure 5. On-Resistance Variation with Temperature

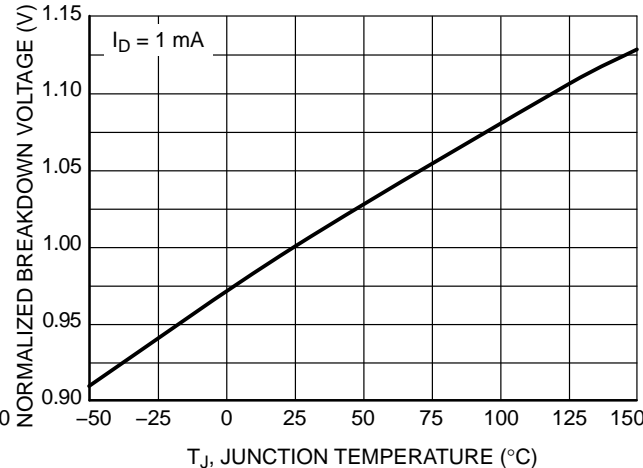


Figure 6. Normalized BVDSS with Temperature

NDD02N40, NDT02N40

TYPICAL CHARACTERISTICS

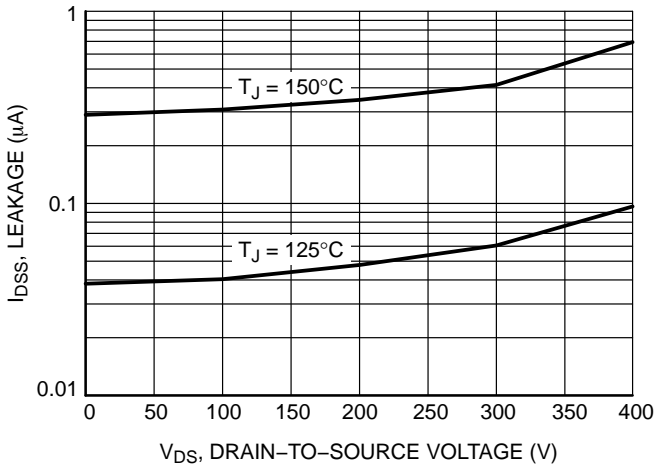


Figure 7. Drain-to-Source Leakage Current vs. Voltage

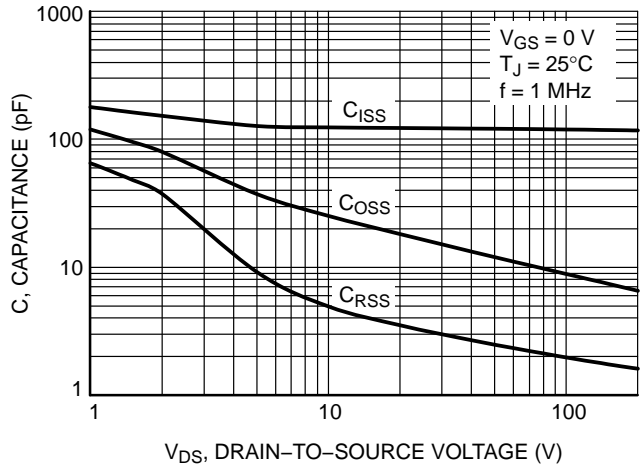


Figure 8. Capacitance Variation

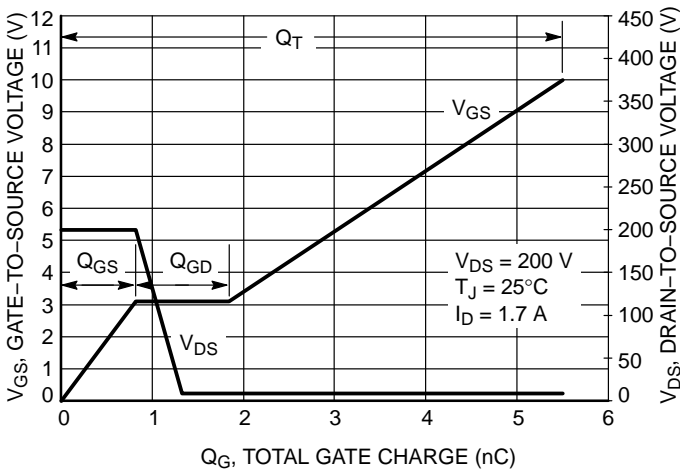


Figure 9. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

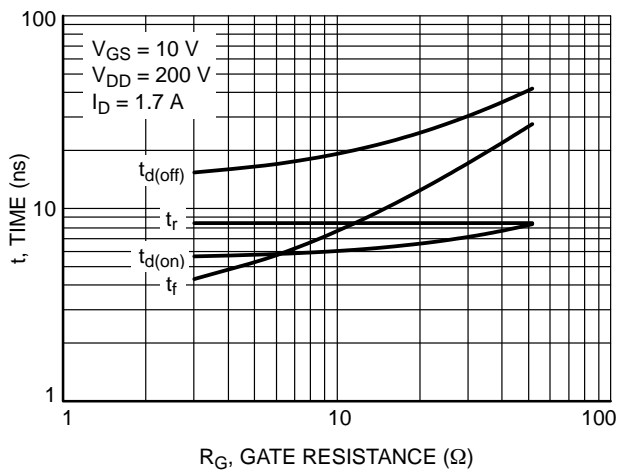


Figure 10. Resistive Switching Time Variation vs. Gate Resistance

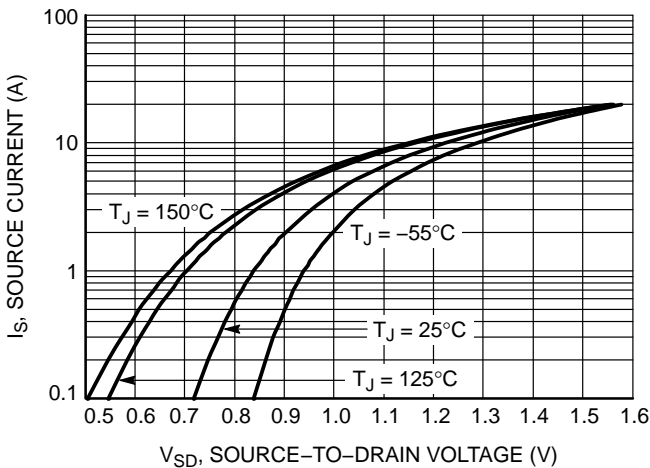


Figure 11. Diode Forward Voltage vs. Current

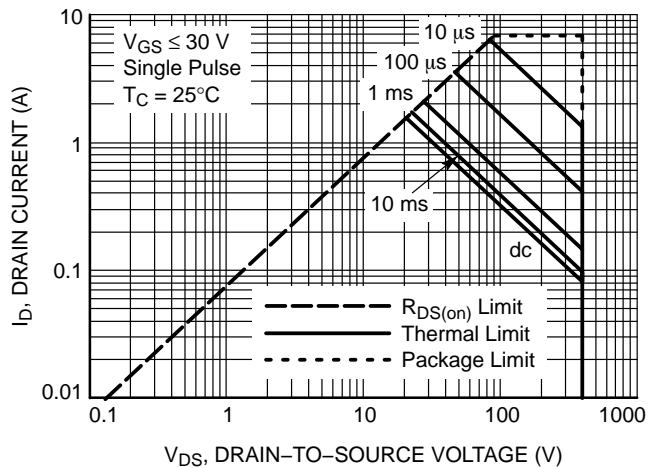


Figure 12. Maximum Rated Forward Biased Safe Operating Area for NDD02N40

NDD02N40, NDT02N40

TYPICAL CHARACTERISTICS

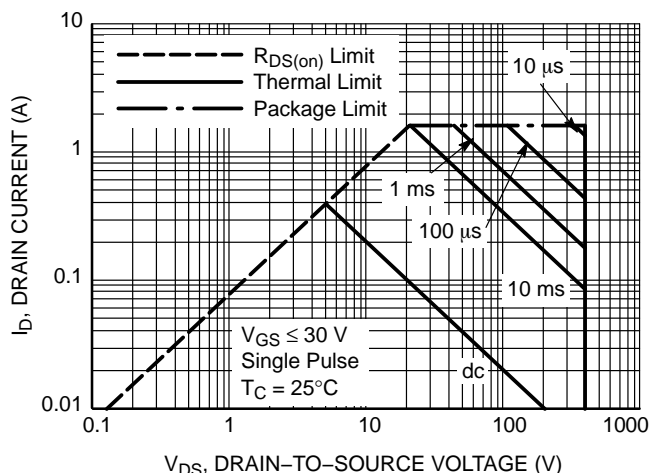


Figure 13. Maximum Rated Forward Biased Safe Operating Area for NDT02N40

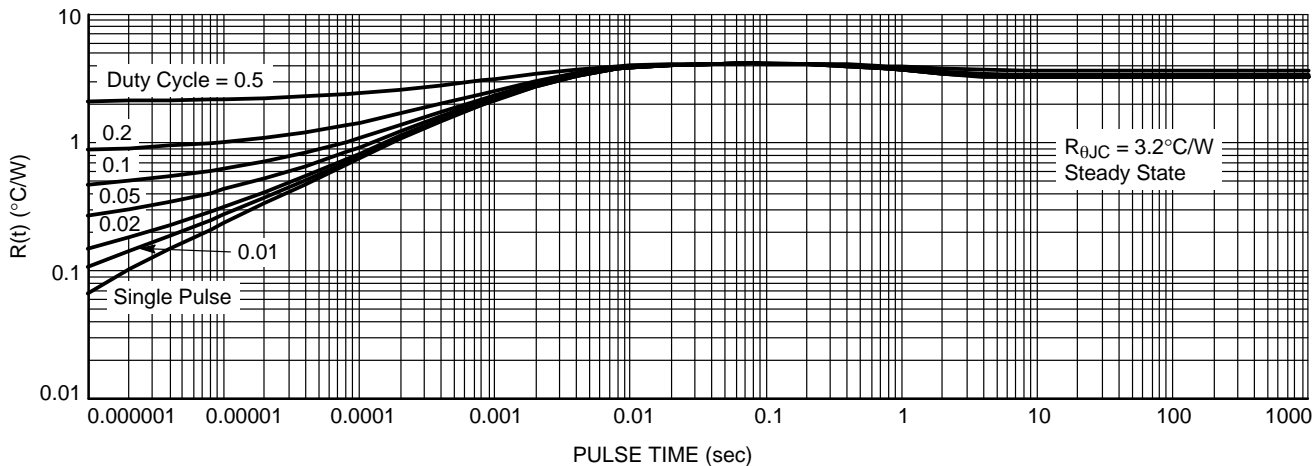


Figure 14. Thermal Impedance (Junction-to-Case) for NDD02N40

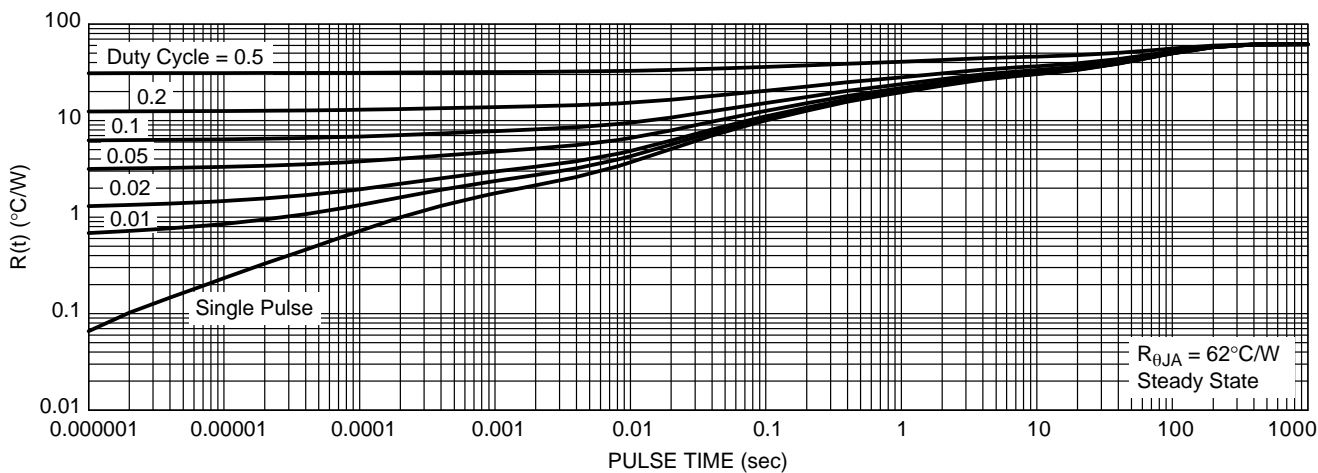


Figure 15. Thermal Impedance (Junction-to-Ambient) for NDD02N40

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

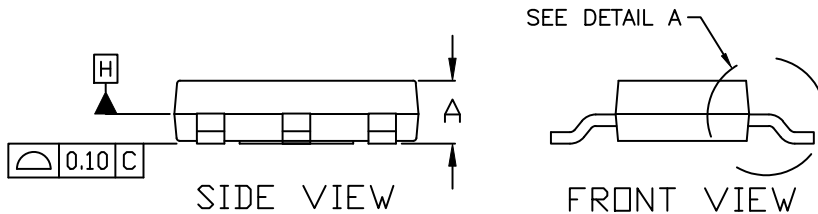
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SCALE 1:1

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

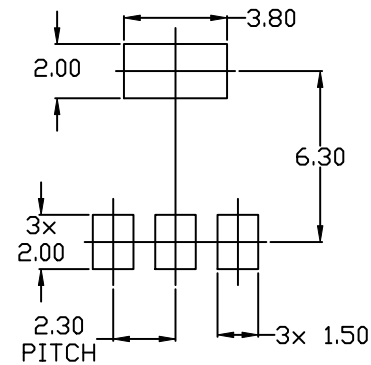
DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



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DESCRIPTION:	SOT-223 (TO-261)	PAGE 1 OF 2

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SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018

- | | | | | |
|--|---|---|---|---|
| STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE | STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN | STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN | STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE |
| STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT | STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE | STYLE 8:
CANCELLED | STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND | STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE |
| STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2 | STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT | STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | | |

**GENERIC
 MARKING DIAGRAM***



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	SOT-223 (TO-261)	PAGE 2 OF 2

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MECHANICAL CASE OUTLINE

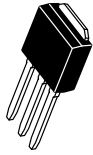
PACKAGE DIMENSIONS

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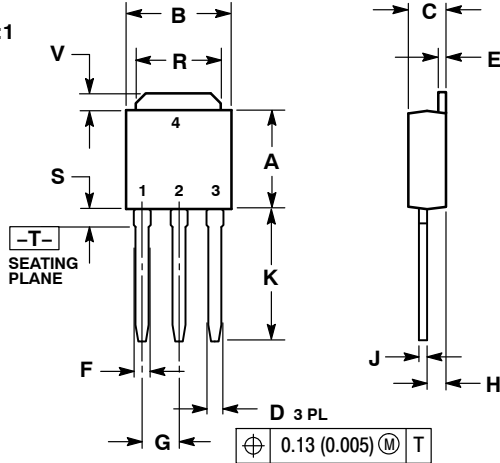


IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010



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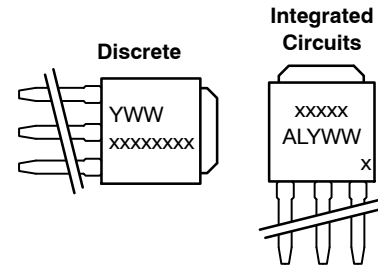


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- | | | | |
|--|---|--|--|
| <p>STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | <p>STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN</p> | <p>STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE</p> | <p>STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE</p> |
| <p>STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE</p> | <p>STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2</p> | <p>STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | |

MARKING DIAGRAMS

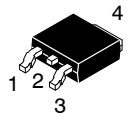


- xxxxxxxxx = Device Code
A = Assembly Location
IL = Wafer Lot
Y = Year
WW = Work Week

DOCUMENT NUMBER:	98AON10528D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	IPAK (DPAK INSERTION MOUNT)	PAGE 1 OF 1

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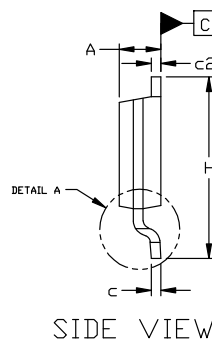
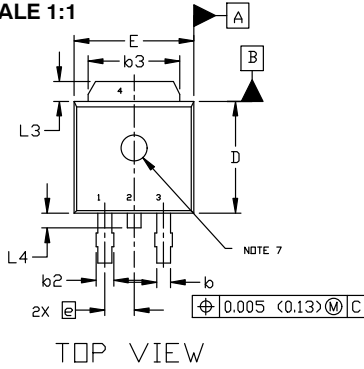
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



DPAK (SINGLE GAUGE) CASE 369C ISSUE G

DATE 31 MAY 2023

SCALE 1:1



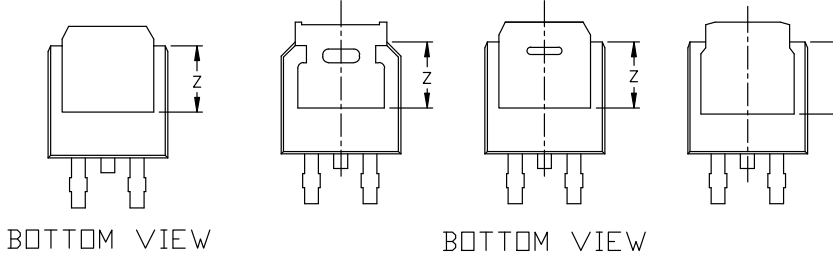
NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

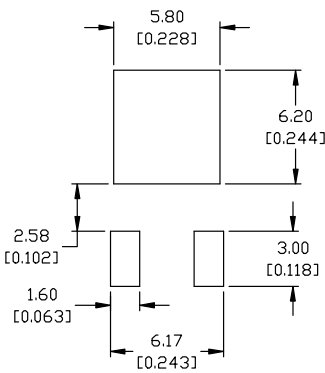
TOP VIEW

SIDE VIEW



BOTTOM VIEW

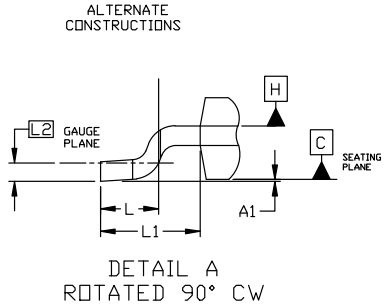
BOTTOM VIEW



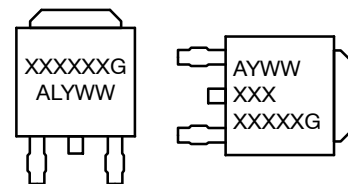
RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

- | | | | | |
|--|--|---|---|--|
| <p>STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | <p>STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN</p> | <p>STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE</p> | <p>STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE</p> | <p>STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE</p> |
| <p>STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2</p> | <p>STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | <p>STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE</p> | <p>STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE</p> | <p>STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE</p> |



GENERIC MARKING DIAGRAM*



- | | |
|--|------------------------|
| <p>IC</p> <p>XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package</p> | <p>Discrete</p> |
|--|------------------------|

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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