Buck Converter - Low Voltage, Dual, Output 2.1 MHz

NCV896530

The NCV896530 dual step−down dc−dc converter is a monolithic integrated circuit dedicated to automotive driver information systems from a downstream voltage rail.

Both channels are externally adjustable from 0.9 V to 3.3 V and can source totally up to 1600 mA. Converters are running at 2.1 MHz switching frequency above the sensitive AM band and operate 180° out of phase to reduce large amounts of current demand on the rail. Synchronous rectification offers improved system efficiency.

The NCV896530 provides additional features expected in automotive power systems such as integrated soft−start, hiccup mode current limit and thermal shutdown protection. The device can also be synchronized to an external clock signal in the range of 2.1 MHz.

The NCV896530 is available in a space saving, 3 x 3 mm 10−pin DFN package.

Features

- Synchronous Rectification for Higher Efficiency
- 2.1 MHz Switching Frequency, 180° Out−of−Phase
- Sources up to 1600 mA Total and 1 A Per Channel
- Adjustable Output Voltage from 0.9 V to 3.3 V
- 2.7 V to 5.5 V Input Voltage Range
- Thermal Limit and Short Circuit Protection
- Auto Synchronizes with an External Clock
- Wettable Flanks – DFN
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This is a Pb−Free Device

Typical Applications

- Audio
- Infotainment
- Vision System
- Instrumentation

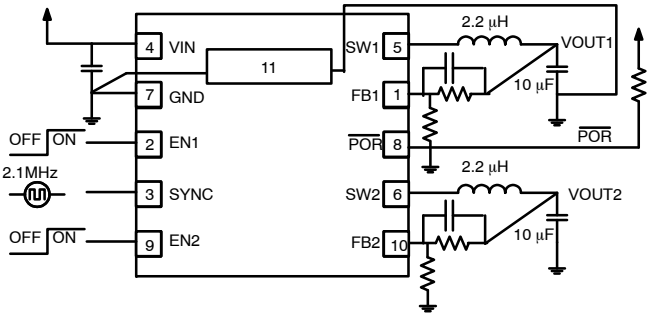


Figure 1. NCV896530 Typical Application

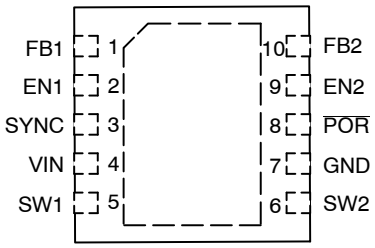
DFN10
CASE 485C

MARKING DIAGRAM

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Device

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 8 of this data sheet.

BLOCK DIAGRAM

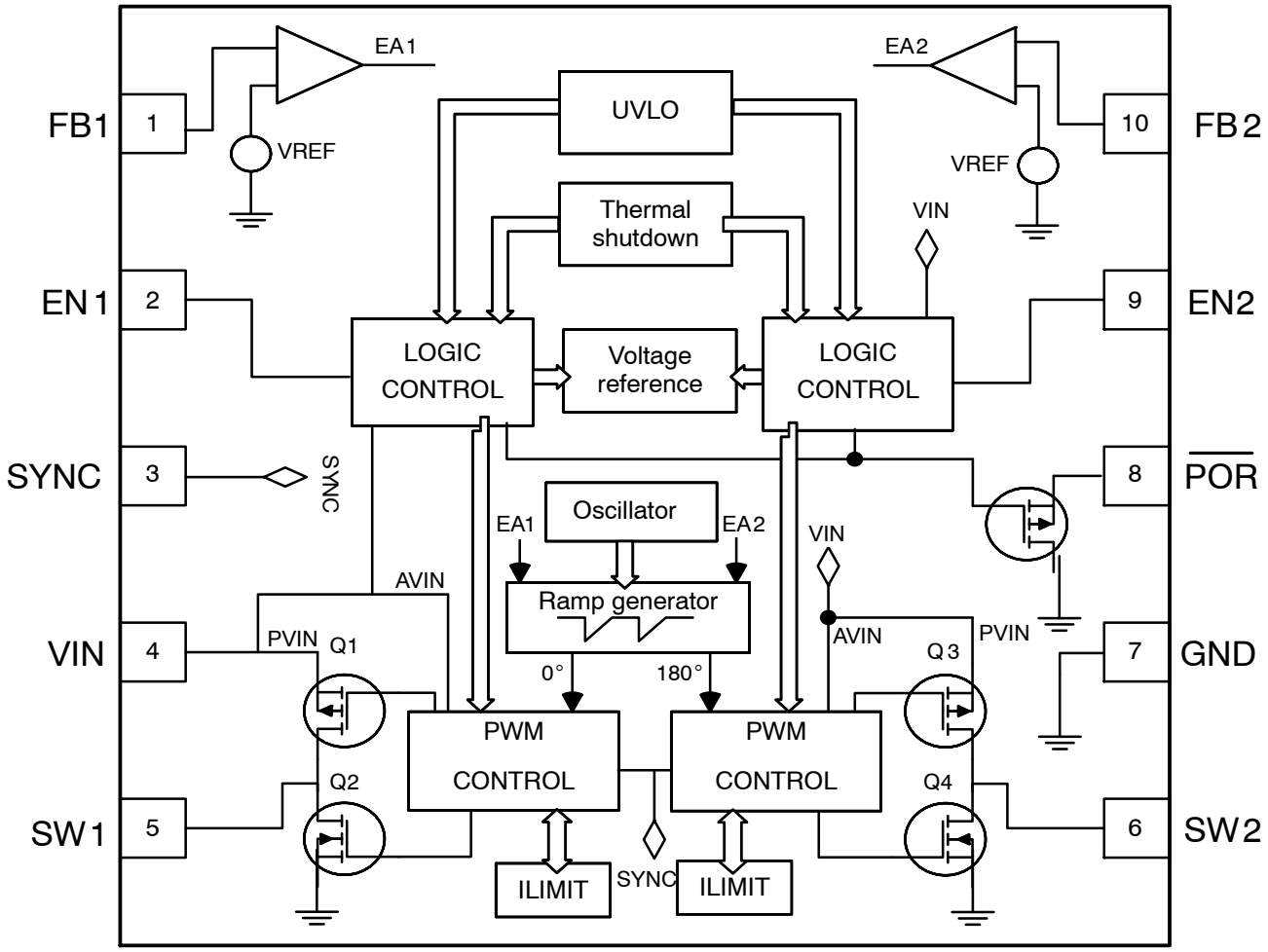


Figure 2. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Type	Description
1	FB1	Analog Input	Feedback voltage from the output 1. This is the input to the error amplifier.
2	EN1	Digital Input	Enable for converter 1. This pin is active HIGH (equal or lower Analog Input voltage) and is turned off by logic LOW. Do not let this pin float.
3	SYNC	Digital Input	Oscillator Synchronization. This pin can be synchronized to an external clock in the range of 2.1 MHz. If not used, the pin must to be connected to ground.
4	VIN	Analog / Power Input	Power supply input for the PFET power stage, analog and digital blocks. The pin must be decoupled to ground by a 10 μF ceramic capacitor.
5	SW1	Analog Output	Connection from power MOSFETs of output 1 to the Inductor.
6	SW2	Analog Output	Connection from power MOSFETs of output 2 to the Inductor.
7	GND	Analog Ground	This pin is the GROUND reference for the analog section of the IC. The pin must be connected to the system ground.
8	POR	Digital Output	Power On Reset. This is an open drain output. This output is shutting down when one of the output voltages are less than 90% (typ) of their nominal values. A pull−up resistor around 500 kΩ should be connected between POR and VIN, VOUT1 or VOUT2 depending on the supplied device.
9	EN2	Digital Input	Enable for converter 2. This pin is active HIGH (equal or lower Analog Input voltage) and is turned off by logic LOW. Do not let this pin float.
10	FB2	Analog Input	Feedback voltage from the output 2. This is the input to the error amplifier.
11	Exposed Pad	Power Ground	This pin is the GROUND reference for the NFET power stage of the IC. The pin must be connected to the system ground and to both input and output capacitors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Minimum Voltage All Pins	V_{min}	−0.3	V
Maximum Voltage All Pins	V_{max}	6.0	V
Maximum Voltage ENx, SYNC, FBx, , SWx, POR	V_{max}	VIN+0.3	V
Thermal Resistance Junction−to−Ambient (3x3 DFN) (Note 1)	$R_{\theta JA}$	40	°C/W
Storage Temperature Range	T_{stg}	−55 to 150	°C
Junction Operating Temperature	T_J	−40 to 150	°C
ESD Withstand Voltage Human Body Model Machine Model	V_{esd}	 2.0 200	 kV V
Moisture Sensitivity Level	MSL	3	per IPC

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted on 1 sq. in. of a 4−layer PCB with 1 oz. copper thickness.

ELECTRICAL CHARACTERISTICS (2.7 V < V_{IN} < 5.5 V, Min and Max values are valid for the temperature range −40°C ≤ T_J ≤ +150°C unless noted otherwise, and are guaranteed by test design or statistical correlation, Typical values are referenced to T_A = +25°C)

Rating	Conditions	Symbol	Min	Typ	Max	Unit
INPUT VOLTAGE						
Quiescent Current	SYNC = GND, V_{FB} = 0 V EN1 = EN2 = 2 V, No Switching	I_Q	–	2.0	3.0	mA
Standby Current	EN1 = EN2 = 0 V	I_{STBMAX}	–	4.0	10	μA
Under Voltage Lockout	V_{IN} falling	V_{UVLO}	2.2	2.4	2.6	V
Under Voltage Hysteresis		V_{UVLOH}	–	100	150	mV
SYNC						
SYNC Threshold Voltage	Logic high	V_{IHSYNC}	1.2	–	–	V
	Logic Low	V_{ILSYNC}			0.4	
SYNC Pin Bias Current	V_{SYNC} = 5 V	I_{ILSYNC}	2		50	μA
External Synchronization		F_{SYNC}	1.8		2.7	MHz
SYNC Pulse Duty Ratio		T_{SYNC}		50		%
EN1, EN2						
ENx Threshold Voltage	Logic high	V_{IHENx}	1.2	–	–	V
	Logic Low	V_{ILENx}			0.4	
ENx Pin Bias Current	V_{ENx} = 5 V	I_{ILENx}	2		50	μA
POWER ON RESET						
Power On Reset Threshold	V_{OUT} falling	V_{PORT}	87%		93%	V
Power On Reset Hysteresis		V_{PORH}	–		3%	V
Sink Current	V_{POR} = 0.4 V	I_{SIPOR}	2			mA
OUTPUT PERFORMANCES						
Feedback Voltage Threshold	FB1, FB2	V_{FB}	–	0.6	–	V
Feedback Voltage Accuracy	T_A = 25C	ΔV_{OUT}		±1	–	%
	−40°C < T_A < 125°C	ΔV_{OUT}	−2	–	+2	
Soft−Start Time	Time from EN to 90% of output voltage	t_{START}	400	–	1000	μs
Switching Frequency	EN1 = EN2 = 1, V_{IN} = 5 V	F_{SW}	1.8	2.1	2.6	MHz
Duty Cycle		D	–	–	100	%
POWER SWITCHES						
High−Side MOSFET On−resistance	$I_{RDS(on)}$ = 600 mA, V_{IN} = 5 V, T_A = 25°C	R_{ONHS}	–	500	820	mΩ
Low−Side MOSFET On−resistance	$I_{RDS(on)}$ = 600 mA, V_{IN} = 5 V, T_A = 25°C	R_{ONLS}	–	450	820	mΩ
High−Side MOSFET Leakage Current	V_{IN} = 5 V, V_{LX} = 0 V, V_{ENx} = 0 V	I_{LEAKHS}	–		5	μA
Low−Side MOSFET Leakage Current	V_{LX} = 5 V, V_{ENx} = 0 V	I_{LEAKLS}	–		5	μA
Minimum On Time		T_{ONMIN}	–		80	ns
PROTECTION						
Current Limit	Peak inductor current, V_{IN} = 5 V, 100% duty cycle	I_{PK}	1.4		2.0	A
Thermal Shutdown Threshold		T_{SD}	150	170	190	°C
Thermal Shutdown Hysteresis		T_{SDH}	5		20	°C
Hiccup Time	% of Soft−Start Time	$t_{hcp,dly}$		60		%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS CURVES

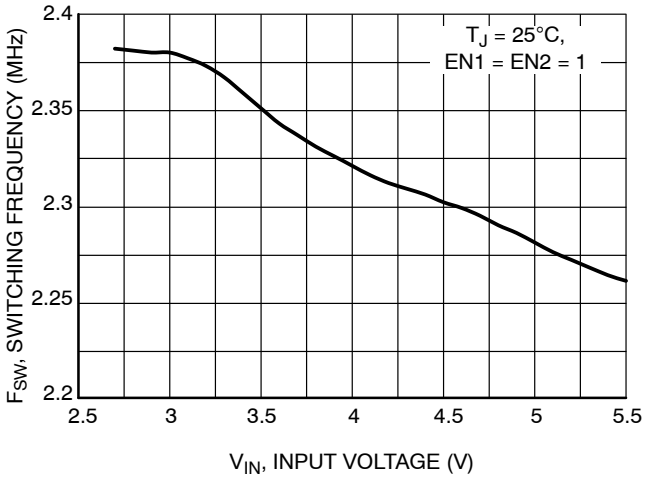


Figure 3. Switching Frequency vs. Input Voltage

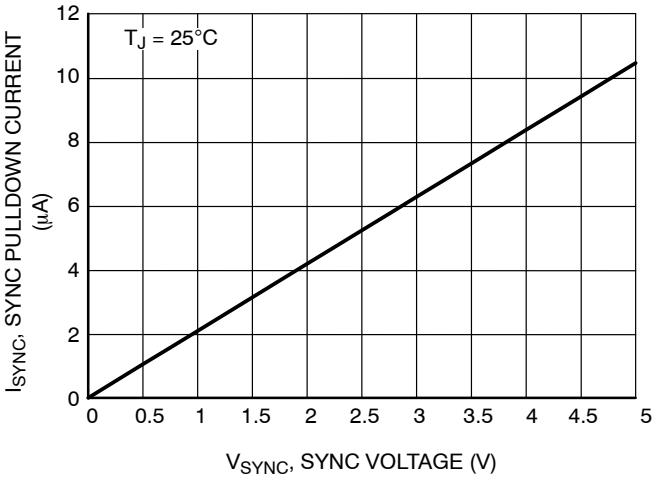


Figure 4. Sync Pulldown Current vs. Sync Voltage

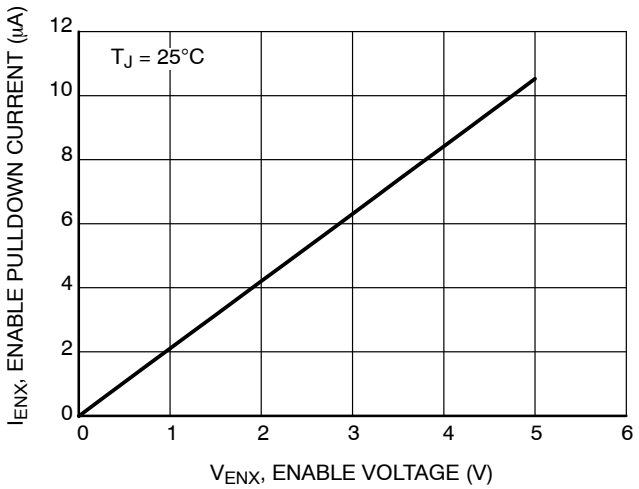


Figure 5. Enable Pulldown Current vs. Enable Voltage

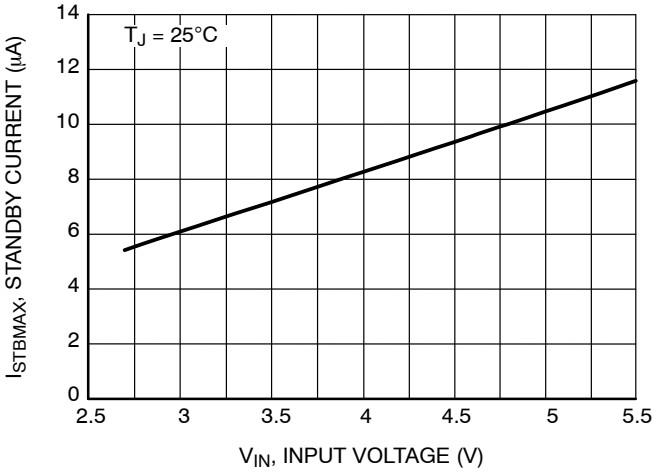


Figure 6. Standby Current vs. Input Voltage

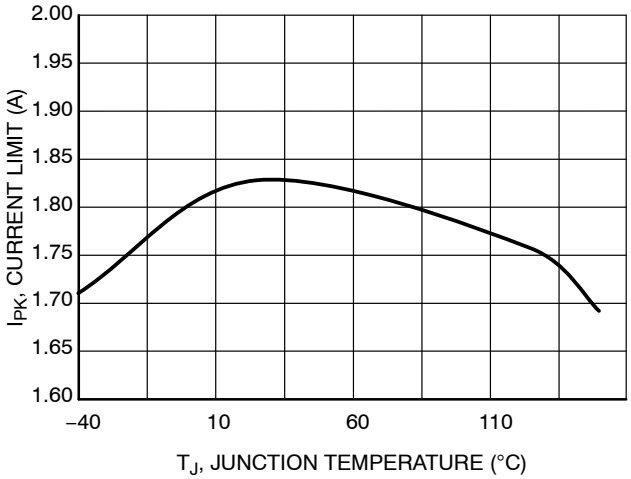


Figure 7. Current Limit vs. Temperature

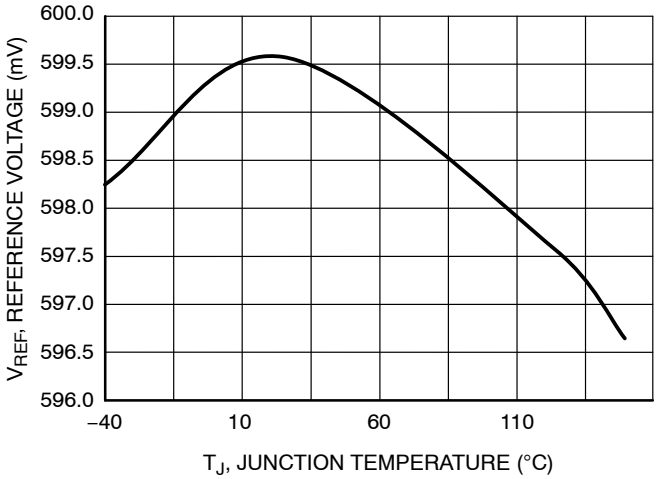


Figure 8. Reference Voltage vs. Temperature

TYPICAL CHARACTERISTICS CURVES

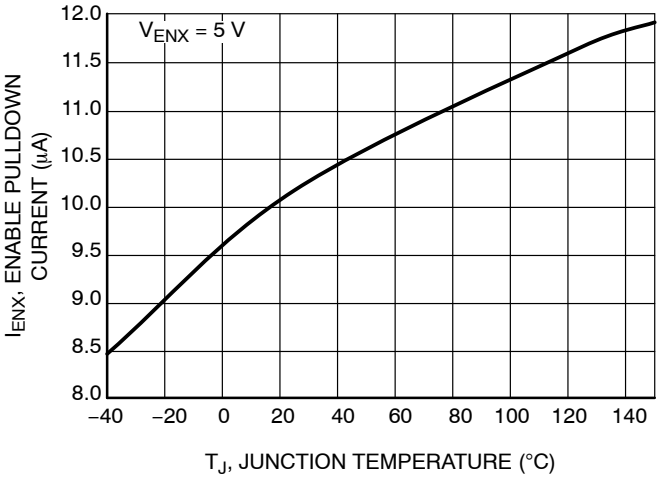


Figure 9. Enable Pulldown Current vs. Temperature

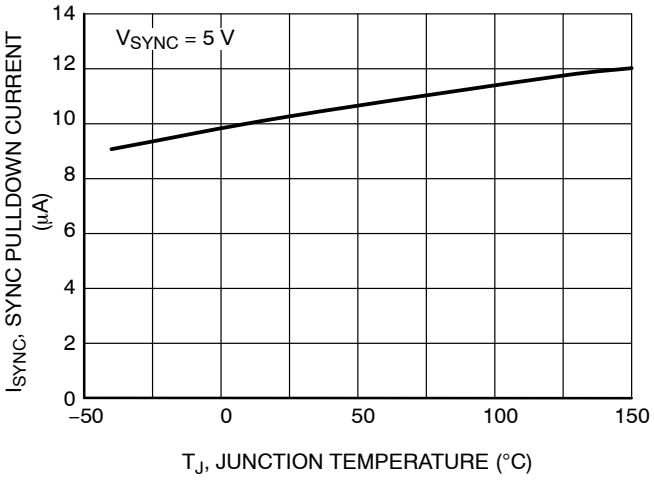


Figure 10. Sync Pulldown Current vs. Temperature

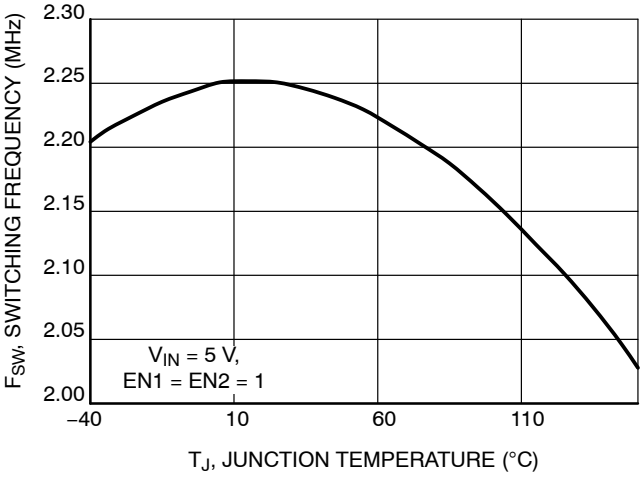


Figure 11. Switching Frequency vs. Temperature

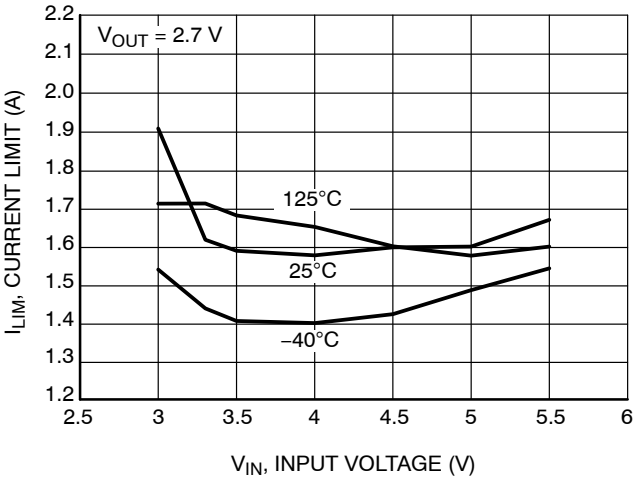


Figure 12. Peak Current Limit vs. Input Voltage

DC/DC OPERATION DESCRIPTION

PWM Operating Mode

The output voltage of the device is regulated by modulating the on−time pulse width of the main switch Q1 at a fixed 2.1 MHz frequency (Figure 13).

The switching of the PMOS Q1 is controlled by a flip−flop driven by the internal oscillator and a comparator that compares the error signal from an error amplifier with the sum of the sensed current signal and compensation ramp.

The driver switches ON and OFF the upper side transistor (Q1) and switches the lower side transistor in either ON state or in current source mode.

At the beginning of each cycle, the main switch Q1 is turned ON by the rising edge of the internal oscillator clock. The inductor current ramps up until the sum of the current sense signal and compensation ramp becomes higher than the error amplifier's voltage. Once this has occurred, the PWM comparator resets the flip−flop, Q1 is turned OFF while the synchronous switch Q2 is turned in its current source mode. Q2 replaces the external Schottky diode to reduce the conduction loss and improve the efficiency. To avoid overall power loss, a certain amount of dead time is introduced to ensure Q1 is completely turned OFF before Q2 is being turned ON.

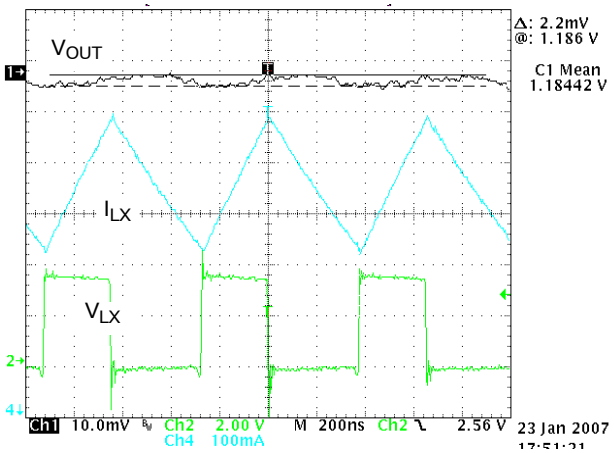


Figure 13. PWM Switching Waveforms

(V_{IN} = 3.6 V, V_{OUT} = 1.2 V, I_{OUT} = 600 mA, Temp = 25°C)

Soft−Start

The NCV896530 uses soft start to limit the inrush current when the device is initially powered up or enabled. Soft start is implemented by gradually increasing the reference voltage until it reaches the full reference voltage. During startup, a pulsed current source charges the internal soft start capacitor to provide gradually increasing reference voltage. When the voltage across the capacitor ramps up to the nominal reference voltage, the pulsed current source will be switched off and the reference voltage will switch to the regular reference voltage.

Over Current Hiccup Protection

When the current through the inductor exceeds the current limit the NCV896530 enters over current hiccup mode. When an over current event is detected the NCV896530 disables the outputs and attempts to re−enable the outputs after the hiccup time. The part remains off for the hiccup time and then goes through the power on reset procedure. If the excessive load has been removed then the output stage re−enables and operates normally; however, if the excessive load is still present the cycle begins again. Internal heat dissipation is kept to a minimum as current will only flow during the reset time of the protection circuitry. The hiccup mode is continuous until the excessive load is removed.

Low Dropout Operation

The NCV896530 offers a low input−to−output voltage difference. The NCV896530 can operate at 100% duty cycle on both channels.

In this mode the PMOS (Q1) remains completely ON. The minimum input voltage to maintain regulation can be calculated as:

$$V_{IN(min)} = V_{OUT(max)} + \left(I_{OUT} \times \left(R_{DS(on)} + R_{INDUCTOR}\right)\right) \quad \text{(eq. 1)}$$

V_{OUT}: Output Voltage
I_{OUT}: Max Output Current
$R_{DS}(ON)$: P−Channel Switch $R_{DS(on)}$
$R_{INDUCTOR}$: Inductor Resistance (DCR)

Power On Reset

The Power On Reset (POR) is pulled low when one of the converter is out of 90% of the regulation. When both outputs are in the range of regulation. If only one channel is active, POR stays low. When the inactive regulator becomes enabled, POR is kept low until the output reaches its voltage range. A pull−up resistor is needed to this open drain output. The resistor may be connected to VIN or to an output voltage of one regulator if the device supplied can not accept VIN on the IO. POR is low when NCV896530 is off. Leave the POR pin unconnected when not used.

Frequency Synchronization

The NCV896530 can be synchronized with an external clock signal by using the SYNC pin (1.8 MHz − 2.4 MHz). During synchronization, the outputs are in phase.

Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. If the junction temperature exceeds T_{SD}, the device shuts down. In this mode all power transistors and control circuits are turned off. The device restarts in soft start after the temperature drops below 130°C min. This feature is provided to prevent catastrophic failures from accidental device overheating.

Switching Frequency

When switcher 2 is enabled and switcher 1 is disabled, the switching frequency is approximately 120 kHz higher than when switcher 1 is enabled and switcher 2 is either enabled or disabled.

Conversion Ratio

The minimum conversion ratio is dictated by switching frequency and the minimum on time. The minimum achievable output is:

$$V_{OUT} = 0.2 \times V_{IN}$$

Maximum Output Capacitance

The maximum output capacitance is determined by the amount the capacitor can be charged during soft start and the effect on the control loop. If more than 100 μF is used on an output small signal analysis should be done to make sure that sufficient phase margin is maintained. The maximum allowable due to soft start current limit is given by the following equation:

$$C_{max} = \frac{I_{OUT,startup}\, t_{start}}{V_{OUT}} \qquad \text{(eq. 2)}$$

C_{max}: Maximum output capacitance (F)
$I_{OUT,startup}$: Output current during soft start (A)
t_{start}: Soft-start time (s)
V_{out}: Regulated output voltage (V)

DEVICE ORDERING INFORMATION

Device	Status	Part Marking	Package	Shipping†
NCV896530MWATXG	Recommended	NCV89 6530A	DFN10 (Pb−Free)	3000 / Tape & Reel
NCV896530MWTXG	Not for new designs	NCV89 6530	DFN10 (Pb−Free)	3000 / Tape & Reel

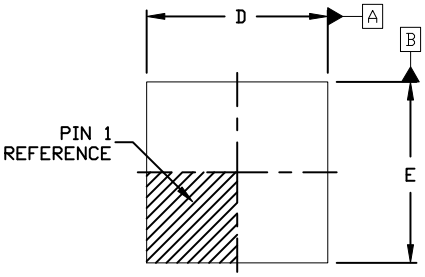
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

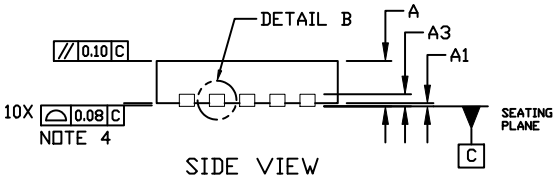
DFN10, 3x3, 0.5P
CASE 485C
ISSUE F

DATE 16 DEC 2021

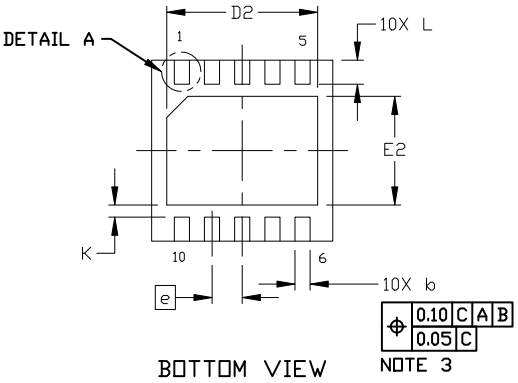
SCALE 2:1



TOP VIEW

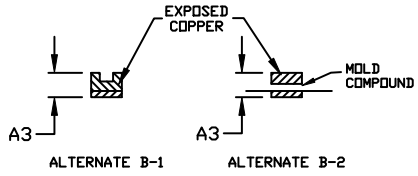


SIDE VIEW

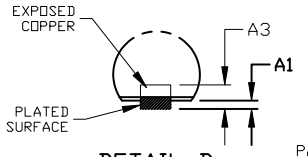


BOTTOM VIEW

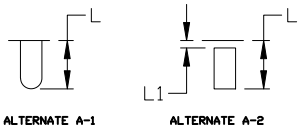
NOTES:
1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASH MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL A AND DETAIL B ALTERNATE CONSTRUCTIONS ARE NOT APPLICABLE. WETTABLE FLANK CONSTRUCTION IS DETAIL B AS SHOWN ON SIDE VIEW OF PACKAGE.



DETAIL B
ALTERNATE CONSTRUCTION

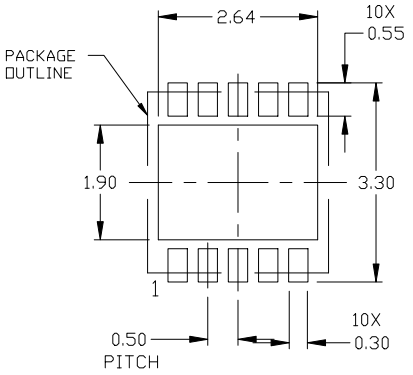


DETAIL B
WETTABLE FLANK
CONSTRUCTION



DETAIL A
ALTERNATE CONSTRUCTION

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3		0.20 REF	
b	0.18	0.23	0.30
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.70	1.80	1.90
e		0.50 BSC	
K		0.20 REF	
L	0.30	0.40	0.50
L1	---	---	0.03



RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON03161D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**DFN10, 3X3 MM, 0.5 MM PITCH**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales