NCP81255

Single-Phase Voltage Regulator with Intel Proprietary Interface for Computing Applications

The NCP81255 is a high-performance, low-bias current, single-phase regulator with integrated power MOSFETs intended to support a wide range of computing applications. The device is able to deliver up to 14 A TDC output current on an adjustable output with Intel proprietary interface interface. Operating in high switching frequency up to 1.2 MHz allows employing small size inductor and capacitors. The controller makes use of ON Semiconductor's patented high performance RPM operation. RPM control maximizes transient response while allowing for smooth transitions between discontinuous-frequency-scaling operation and continuous-mode full-power operation. The NCP81255 has an ultra-low offset current monitor amplifier with programmable offset compensation for high-accuracy current monitoring.

Features

- Auto DCM Operation in High Current Power States
- High Performance RPM Control System
- IMVP8 Intel proprietary interface Support
- Ultra Low Offset IOUT Monitor
- Dynamic VID Feed-Forward
- Programmable Droop Gain
- Zero Droop Capable
- Supports IMVP8 Intel proprietary interface Addresses
- PSYS Input Monitor
- Thermal Monitor
- UltraSonic Operation
- Digitally Controlled Operating Frequency
- QFN40 5 mm × 5 mm Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- IMVP8 Rail1, Rail3, and Rail4

ON Semiconductor®

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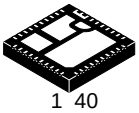

QFN40
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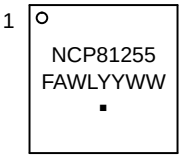
MARKING DIAGRAM



NCP81255	= Specific Device Code
F	= Wafer Fab
A	= Assembly Location
WL	= Lot ID
YY	= Year
WW	= Work Week
▪	= Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP81255MNTXG	QFN40 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

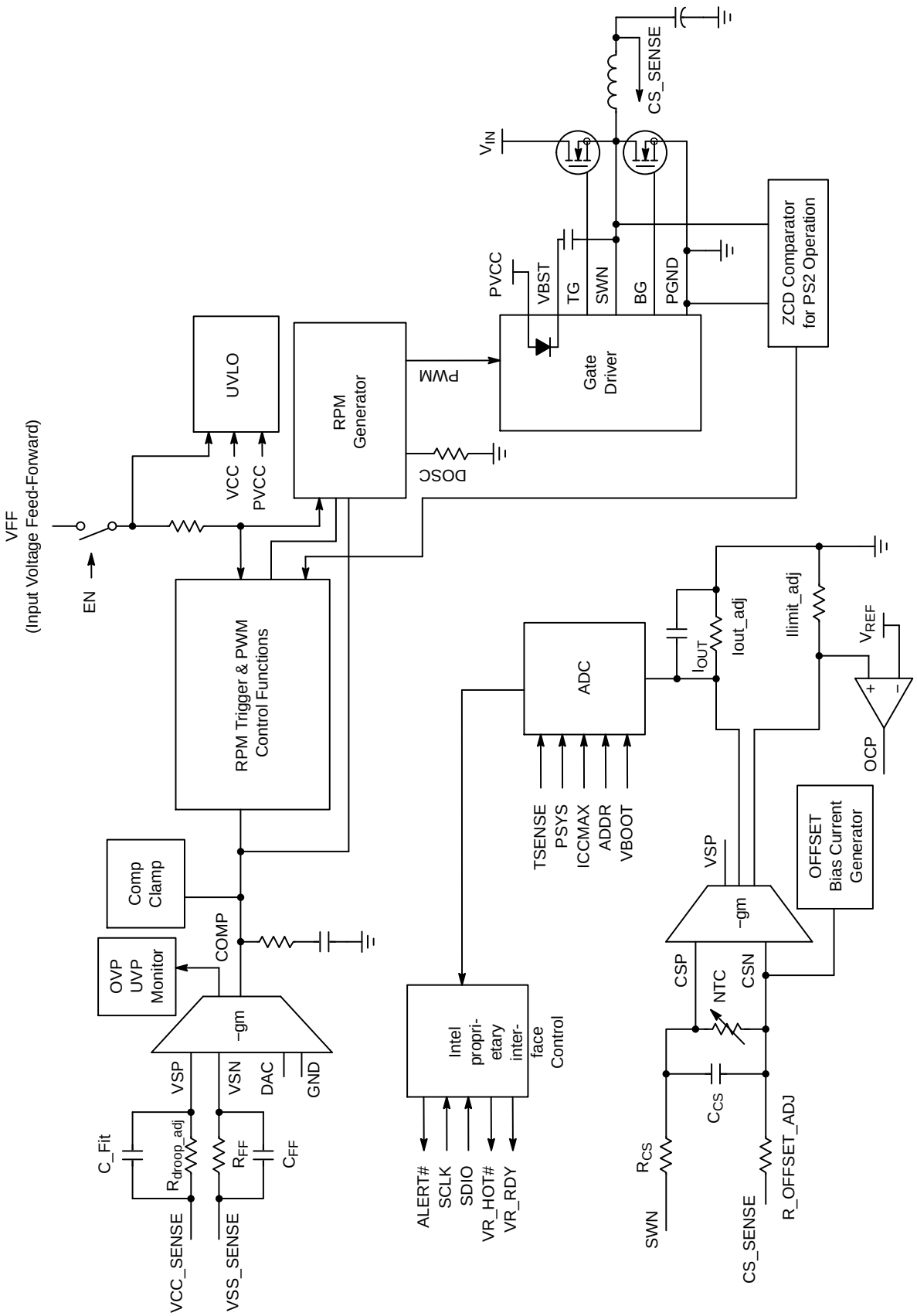


Figure 1. Block Diagram

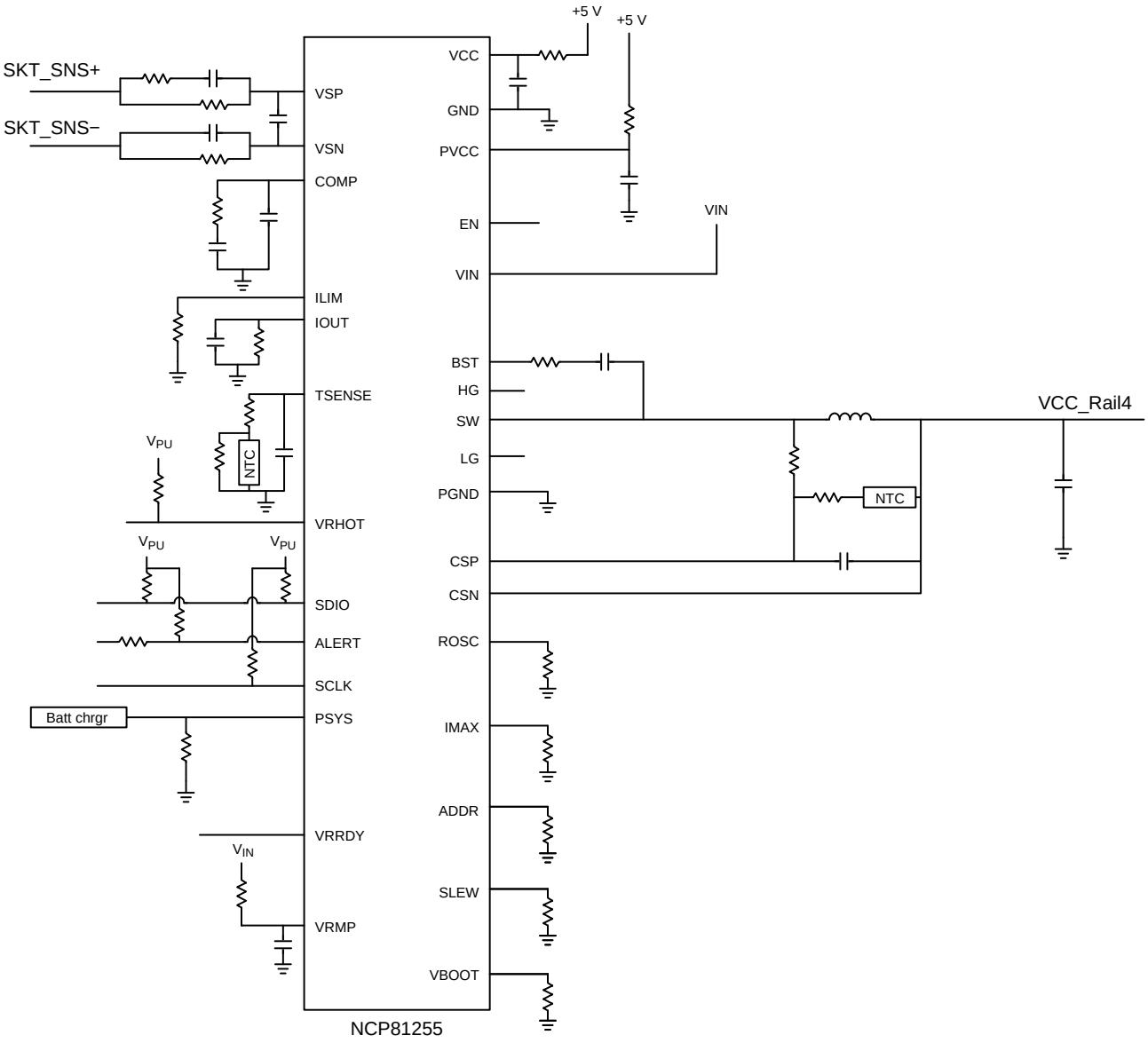


Figure 2. Simplified Application Schematic

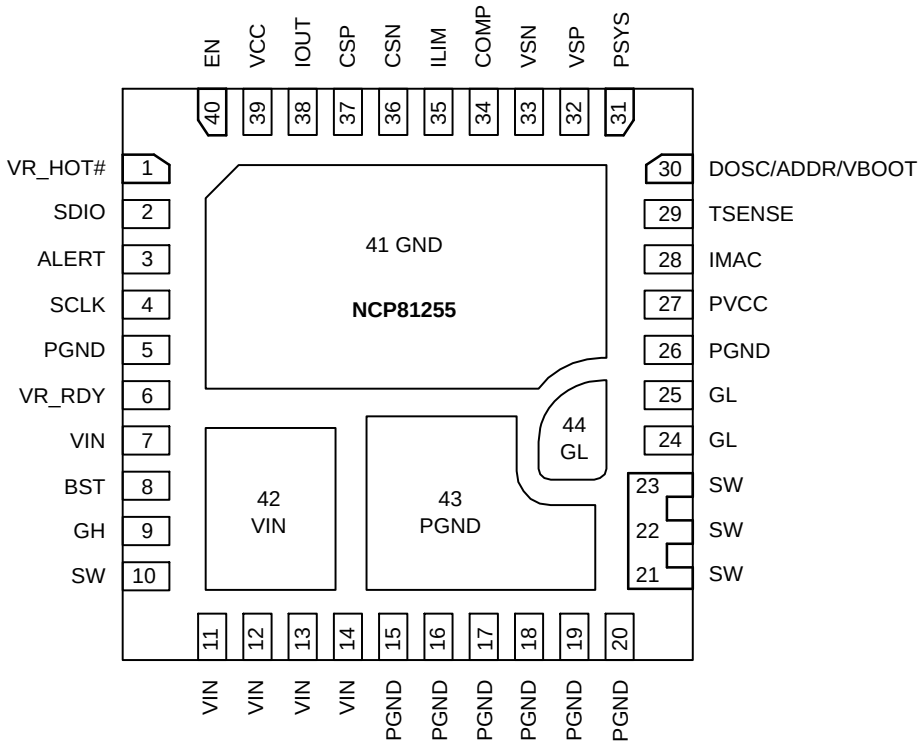


Figure 3. Pin Configuration

Table 1. NCP81255 PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	VR_HOT#	Thermal Logic Output for Over-Temperature Condition on either TSENSE
2	SDIO	Serial VID Data Interface
3	ALERT#	Serial VID ALERT#
4	SCLK	Serial VID Clock
5	PGND	Power Ground. Power Supply Ground Pins, Connected to Source of Internal LS FET
6	VR_RDY	VR_RDY Indicates the Controller is Ready to Accept Intel proprietary interface Commands
7	VIN	Input Voltage for HS FET Drain. 22 μF or More Ceramic Caps must Bypass this Input to Power Ground. Place Close to Pins
8	BST	Provides Bootstrap Voltage for the HS Gate Driver. A Cap is Required from this Pin to SW
9	GH	Gate of HS FET
10	SW	Switching Node. Provides a Return Path for the Integrated HS Driver. Internally Connected to the Source of the HS FET
11	VIN	Input Voltage for HS FET Drain. 22 μF or More Ceramic Caps must Bypass this Input to Power Ground. Place Close to Pins
12	VIN	Input Voltage for HS FET Drain. 22 μF or More Ceramic Caps must Bypass this Input to Power Ground. Place Close to Pins
13	VIN	Input Voltage for HS FET Drain. 22 μF or More Ceramic Caps must Bypass this Input to Power Ground. Place Close to Pins
14	VIN	Input Voltage for HS FET Drain. 22 μF or More Ceramic Caps must Bypass this Input to Power Ground. Place Close to Pins
15	PGND	Power Ground. Power Supply Ground Pins, Connected to Source of Internal LS FET
16	PGND	Power Ground. Power Supply Ground Pins, Connected to Source of Internal LS FET
17	PGND	Power Ground. Power Supply Ground Pins, Connected to Source of Internal LS FET
18	PGND	Power Ground. Power Supply Ground Pins, Connected to Source of Internal LS FET

Table 1. NCP81255 PIN DESCRIPTIONS (continued)

Pin No.	Symbol	Description
19	PGND	Power Ground. Power Supply Ground Pins, Connected to Source of Internal LS FET
20	PGND	Power Ground. Power Supply Ground Pins, Connected to Source of Internal LS FET
21	SW	Switch Node. Pins to be Connected to an External Inductor. These Pins are Interconnection between Internal HS and LS FETs
22	SW	Switch Node. Pins to be Connected to an External Inductor. These Pins are Interconnection between Internal HS and LS FETs
23	SW	Switch Node. Pins to be Connected to an External Inductor. These Pins are Interconnection between Internal HS and LS FETs
24	GL	Gate of LS FET
25	GL	Gate of LS FET
26	PGND	Power Ground. Power Supply Ground Pins, Connected to Source of Internal LS FET
27	PVCC	Voltage Supply of Gate Drivers. A 4.7 μF or Larger Ceramic Capacitor Bypasses this Input to GND, Placed as Close to the Pin as Possible
28	IMAX	ICCMAX Register Program
29	TSENSE	External Temperature Sense Network is Connected to this Pin
30	DOSC/ADDR/ VBOOT	Programming for F_{SW}, Intel proprietary interface Address, and V_{BOOT}. A Resistor to GND Programs these Values during Start-up, per Look-up Table
31	PSYS	System Power Signal Input. A Resistor to Ground Scales this Signal
32	VSP	Differential Output Voltage Sense Positive
33	VSN	Differential Output Voltage Sense Negative
34	COMP	Compensation
35	ILIM	Current-Limit Program
36	CSN	Differential Current Sense Negative
37	CSP	Differential Current Sense Positive
38	IOUT	IOUT Gain Program
39	VCC	Power Supply Input Pin of Control Circuits. A 1 μF or Larger Ceramic Capacitor Bypasses this Input to Ground, Placed Close to the Controller
40	EN	Enable
41	GND	Flag. Analog Ground. Ground of Internal Control Circuits
42	VIN	Flag. Input Voltage for HS FET Drain. 22 μF or More Ceramic Caps must Bypass this Input to Power Ground. Place Close to Pins
43	PGND	Flag. Power Ground. Power Supply Ground Pins, Connected to Source of Internal LS FET.
44	GL	Flag. Gate of LS FET

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Power Supply Voltage to PGND	V_{VIN}	−	30	V
Switch Node to PGND	V_{SW}	−0.3	30	V
Analog Supply Voltage to GND	V_{CC}, V_{CCP}	−0.3	6.5	V
BST to PGND	BST_PGND	−0.3	33 38 (< 50 ns)	V
BST to SW	BST_SW	−0.3	6.5	V
GH to SW	GH	−0.3 −2 (< 200 ns)	BST + 0.3	V
GL to GND	GL	−0.3 −2 (< 200 ns)	V_{CCP} + 0.3	V
VSN to GND	VSN	−0.3	0.3	V
IOUT	IOUT	−0.3	2.5	V
PGND to GND	PGND	−0.3	0.3	V
Other Pins		−0.3	V_{CC} + 0.3	V
Latch Up Current: (Note 1) All Pins, Except Digital Pins Digital Pins	I_{LU}	 −100 −10	 100 10	mA
Operating Junction Temperature Range	T_J	−40	125	°C
Operating Ambient Temperature Range	T_A	−40	100	°C
Storage Temperature Range	T_{STG}	−40	150	°C
Thermal Resistance Junction to Board (Note 2)	$R_{\theta JB}$	8.2		°C/W
Thermal Resistance Junction to Ambient (Note 2)	$R_{\theta JA}$	21.8		°C/W
Power Dissipation at T_A = 25°C (Note 3)	P_D	4.59		W
Moisture Sensitivity Level (Note 4)	MSL	3		−
ESD Human Body Model	HBM	2,000		V
ESD Machine Model	MM	200		V
ESD Charged Device Model	CDM	1,000		V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Latch up Current per JEDEC standard: JESD78 Class II.
2. The thermal resistance values are dependent on the internal losses split between devices and the PCB heat dissipation. This data is based on a typical operation condition with a 4-layer FR−4 PCB board, which as two, 1-ounce copper internal power and ground planes and 2-ounce copper traces on top and bottom layers with approximately 80% copper coverage. No airflow and no heat sink applied (reference EIA/JEDEC 51.7). It also does not account for other heat sources that may be present on the PCB next to the device in question (such as inductors, resistors, etc.)
3. The maximum power dissipation (PD) is dependent on input voltage, output voltage, output current, external components selected, and PCB layout. The reference data is obtained based on T_{JMAX} = 125°C and $R_{\theta JA}$ = 21.8°C/W.
4. Moisture Sensitivity Level (MSL): 3 per IPC/JEDEC Standard: J−STD−020D.1.

Table 3. ELECTRICAL CHARACTERISTICS
(Unless otherwise stated: −40°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Unit
BIAS SUPPLY					
VCC Quiescent Current	EN = High	−	10	12	mA
	EN = Low	−	20	40	μA
	PS3	−	−	10	mA
	PS4	−	−	200	μA
VCC UVLO Threshold	VCC Rising	−	−	4.5	V
	VCC Falling	4	−	−	V
VCC UVLO Hysteresis		−	275	−	mV
VIN UVLO Threshold	VIN Rising	−	−	4.25	V
	VIN Falling	3	−	−	V
VIN UVLO Hysteresis		−	680	−	mV
ENABLE INPUT					
Enable High Input Leakage Current	Enable = 0	−1.0	0	1.0	μA
Upper Threshold	V_{UPPER}	0.8	−	−	V
Lower Threshold	V_{LOWER}	−	−	0.3	V
Enable Hysteresis		−	300	−	mV
Enable Delay Time	Measure Time from Enable Transitioning HI to VR_RDY High	−	−	2.5	ms
DAC SLEW RATE					
Soft Start Slew Rate		−	1/2 SR Fast	−	mv/μs
Slew Rate Slow		−	1/2 SR Fast	−	mv/μs
Slew Rate Fast		−	30	−	mv/μs
OSCILLATOR					
Switching Frequency Range		600	−	1,200	KHz
Switching Frequency Accuracy	600 KHz < F_{SW} < 1.2 MHz	−10	−	10	%
ADC					
Voltage Range		0	−	2	V
Total Unadjusted Error (TUE)		−1	−	+1	%
Differential Non-Linearity (DNL)	8-Bit	−	−	1	LSB
Power Supply Sensitivity		−	±1	−	%
Conversion Time		−	6	−	μs
Round Robin		−	55	−	μs
VR_HOT#					
Output Low Voltage		−	−	0.3	V
Output Leakage Current	High Impedance State	−1.0	−	1.0	μA
TSENSE					
Alert# Assert Threshold		−	491	−	mV
Alert# De-Assert Threshold		−	513	−	mV
VRHOT Assert Threshold		−	472	−	mV
VRHOT Rising Threshold		−	494	−	mV
TSENSE Bias Current		116	120	124	μA

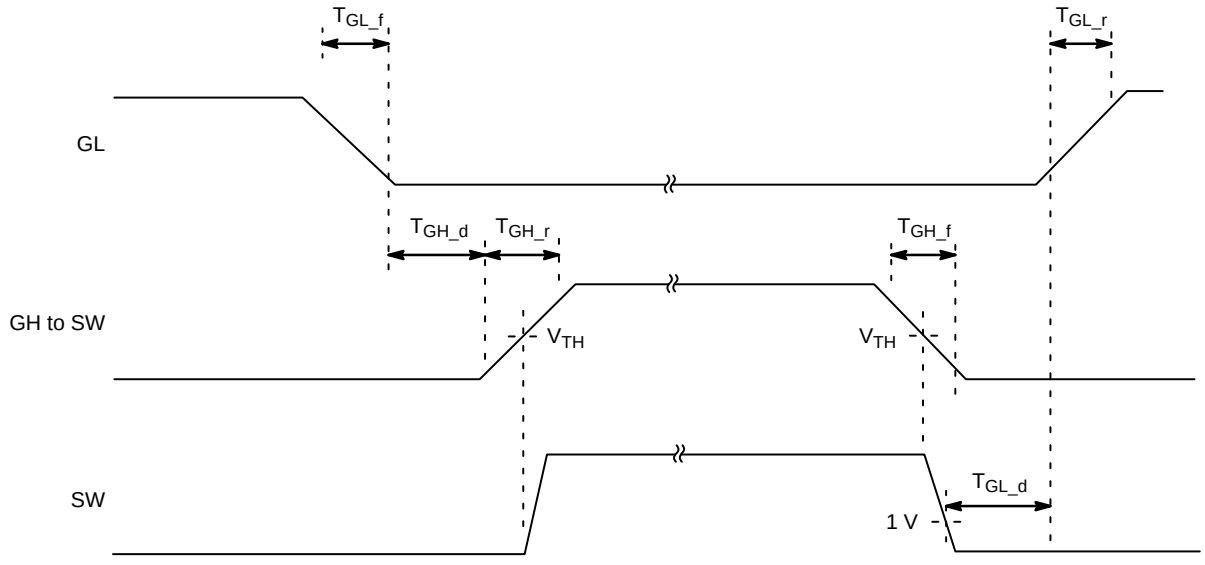
Table 3. ELECTRICAL CHARACTERISTICS (continued)
(Unless otherwise stated: −40°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Unit
VR_RDY_OUTPUT					
Output Low Saturation Voltage	I_{VR_RDY} = 4 mA,	−	−	0.3	V
Rise Time	External Pull-Up of 1 kΩ to 3.3 V, C_{TOT} = 45 pF, ΔVo = 10% to 90%	−	−	150	ns
Fall Time	External Pull-Up of 1 kΩ to 3.3 V, C_{TOT} = 45 pF, ΔVo = 90% to 10%	−	−	150	ns
Output Voltage at Power-Up	VRRDY Pulled Up to 5 V via 2 kΩ	−	−	1.2	V
Output Leakage Current When High	VRRDY = 5.0 V	−1.0	−	1.0	μA
VRRDY Delay (Falling)	From OCP	−	0	−	μs
VRRDY Delay (Falling)	From OVP	−	0.3	−	μs
DIFFERENTIAL VOLTAGE SENSE AMPLIFIER					
Input Bias Current		−1	−	1	μA
VSP Input Voltage Range		−0.3	−	3.0	V
VSN Input Voltage Range		−0.3	−	0.3	V
gm	VSP = 1.2 V	1.33	1.6	1.86	mS
Open loop Gain	Load = 1 nF in Series with 1 kΩ in Parallel with 10 pF to Ground	70	73	−	dB
Source Current	Input Differential −200 mV	−	280	−	μA
Sink Current	Input Differential 200 mV	−	280	−	μA
−3dB Bandwidth	Load = 1 nF in Series with 1 kΩ in Parallel with 10 pF to Ground	−	15	−	MHz
IOUT					
Analog Gain Accuracy		−3	−	+3	%
gm		0.95	1.0	1.05	mS
IOUT Output Accuracy		−140	−	140	nA
ADC Voltage Range		0	−	2.0	V
ADC Differential Nonlinearity (DNL)	Highest 8-Bits	−	−	1	LSB
OUTPUT OVER VOLTAGE & UNDER VOLTAGE PROTECTION (OVP & UVP)					
Over Voltage Threshold	VSP−VSN−VID Setting	360	−	440	mV
Over Voltage Max Capability		−	2	−	V
Over Voltage Delay	VSP Rising to PWMx Low	−	400	−	ns
Over Voltage VR_RDY Delay	VSP Rising to VR_RDY Low	−	400	−	ns
Under Voltage Threshold	VSP−VSN Falling	225	290	375	mV
Under-Voltage Hysteresis	VSP−VSN Falling/Rising	−	25	−	mV
Under-Voltage Blanking Delay	VSP−VSN Falling to VR_RDY Falling	−	5	−	μs
DROOP					
gm		0.95	1.0	1.05	mS
Offset Accuracy		−1	−	1	μA
Common Mode Rejection	CS1 Input Referred from 0.5 V to 1.2 V	−	80	−	dB
OVERCURRENT PROTECTION					
ILIMIT Threshold		1.275	1.3	1.325	V
ILIMIT Delay		−	500	−	ns
ILIMIT Gain	I_{ILIMIT}/(CSP−CSN), CSP−CSN = 20 mV	−	1.0	−	mS
CSP-CSN ZCD COMPARATOR					
Offset Accuracy		−1.85	−	1.85	mV

Table 3. ELECTRICAL CHARACTERISTICS (continued)
(Unless otherwise stated: −40°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Unit
SWN ZCD COMPARATOR					
Offset Accuracy		−1.5	−	1.5	mV
HIGH-SIDE MOSFET					
Drain-to-Source On Resistance	V_{GS} = 4.5 V, I_D = 10 A, R_{ON_H}	−	8.0	−	mΩ
LOW-SIDE MOSFET					
Drain-to-Source On Resistance	V_{GS} = 4.5 V, I_D = 10 A, R_{ON_L}	−	4.0	−	mΩ
HIGH-SIDE GATE DRIVE					
Pull-High Drive On Resistance	$V_{BST} - V_{SW}$ = 5 V, R_{DRV_HH}	−	1.2	2.5	Ω
Pull-Low Drive On Resistance	$V_{BST} - V_{SW}$ = 5 V, R_{DRV_HL}	−	0.8	2.0	Ω
GH Propagation Delay Time	From GL Falling to GH Rising, T_{GH_d}	15	23	30	ns
GH Rise Time	TGH_R	−	9	15	ns
GH Fall Time	TGH_F	4	9	15	ns
GH Pull-Down Resistance	$V_{BST} - V_{SW}$ = 0 V	−	292	−	kΩ
LOW-SIDE GATE DRIVE					
Pull-High Drive On Resistance	$V_{CCP} - V_{PGND}$ = 5 V, R_{DRV_LH}	−	0.9	2.5	Ω
Pull-Low Drive On Resistance	$V_{CCP} - V_{PGND}$ = 5 V, R_{DRV_LL}	−	0.4	1.25	Ω
GL Propagation Delay Time	From GH Falling to GL Rising, T_{GL_d}	−	11	30	ns
GL Rise Time	TGL_R	6	9	15	ns
GL Fall Time	TGL_F	−	11	15	ns
SW TO PGND RESISTANCE					
SW to PGND Pull-Down Resistance	R_{SW} (Note 1)	−	2	−	kΩ
BOOTSTRAP RECTIFIER SWITCH					
Output Low Resistance	EN = L or EN = H and DRVL = H, R_{on_BST}	5	13	21	Ω

1. Guaranteed by design, not tested in production.
2. T_J = 25°C



NOTE: Timing is referenced to the 10% and the 90% points, unless otherwise stated.

Figure 4. Driver Timing Diagram

Table 4. STATE TRUTH TABLE

State	VR_RDY Pin	Error AMP Comp Pin	OVP & UVP	Method of Reset
POR 0 < VCC < UVLO	N/A	N/A	N/A	
Disabled EN < Threshold UVLO > Threshold	Low	Low	Disabled	
Start-Up Delay & Calibration EN > Threshold UVLO > Threshold	Low	Low	Disabled	
Soft Start EN > Threshold UVLO > Threshold	Low	Operational	Active/No Latch	
Normal Operation EN > Threshold UVLO > Threshold	High	Operational	Active/Latching	N/A
Over Voltage	Low	N/A	DAC + 150 mV	
Over Current	Low	Operational	Last DAC Code	
Vout = 0 V	Low: if Reg34h: bit 0 = 0; High: if Reg34h: bit 0 = 1;	Clamped at 0.9 V	Disabled	

GENERAL

The NCP81255 is a single phase IMVP8 Intel proprietary interface controller with a built in gate driver. The controller makes use of a digitally enhanced high performance current mode RPM control method that provides excellent transient response while minimizing transient aliasing. The average operating frequency is digitally stabilized to remove frequency drift under all continuous mode operating conditions. At light load the NCP81255 automatically transitions into DCM operation to save power.

Serial VID Interface (Intel proprietary interface)

For Intel proprietary interface communication details please contact Intel®, Inc.

Switching Frequency, Intel proprietary interface Address, and Boot Voltage Programming

F_{SW}, address, and VBOOT are during power up on a single pin. A 10 μA current is sourced from the pin and the resulting voltage is measured. This is compared with the thresholds and the corresponding values for F_{SW}, VBOOT, and Intel proprietary interface address are configured. These values are programmed on power up and cannot be changed after the initial power up sequence is complete.

Table 5. SWITCHING FREQUENCY

	Resistor	F_{SW}	Address	VBOOT
1	10 kΩ	1.2 MHz	0	0 V
2	13 kΩ	1.1 MHz	0	0 V
3	16 kΩ	1.0 MHz	0	0 V
4	19.2 kΩ	900 kHz	0	0 V
5	22.5 kΩ	800 kHz	0	0 V
6	26 kΩ	700 kHz	0	0 V
7	29.6 kΩ	600 kHz	0	0 V
8	33.5 kΩ	1.2 MHz	1	0 V
9	37.4 kΩ	1.1 MHz	1	0 V
10	41.5 kΩ	1.0 MHz	1	0 V
11	45.8 kΩ	900 kHz	1	0 V
12	50.2 kΩ	800 kHz	1	0 V
13	54.8 kΩ	700 kHz	1	0 V
14	59.5 kΩ	600 kHz	1	0 V
15	64.5 kΩ	1.2 MHz	2	1.05 V
16	69.6 kΩ	1.1 MHz	2	1.05 V
17	75 kΩ	1.0 MHz	2	1.05 V
18	80.6 kΩ	900 kHz	2	1.05 V
19	86.5 kΩ	800 kHz	2	1.05 V
20	92.6 kΩ	700 kHz	2	1.05 V
21	99 kΩ	600 kHz	2	1.05 V
22	105.5 kΩ	1.2 MHz	3	0 V
23	112.5 kΩ	1.1 MHz	3	0 V
24	119.6 kΩ	1.0 MHz	3	0 V
25	127 kΩ	900 kHz	3	0 V
26	134.8 kΩ	800 kHz	3	0 V
27	143 kΩ	700 kHz	3	0 V
28	151.4 kΩ	600 kHz	3	0 V
29	160.3 kΩ	700kHz	0	1.05 V
30	169.5 kΩ	700kHz	1	1.05 V
31	180 kΩ	700 kHz	2	0 V
32	210 kΩ	700 kHz	3	1.05 V

Remote Sense Error Amplifier

A high performance, high input impedance, true differential transconductance amplifier is provided to accurately sense the regulator output voltage and provide high bandwidth transient performance. The VSP and VSN inputs should be connected to the regulator's output voltage sense points through filter networks describe in the Droop Compensation and DAC Feed-Forward Compensation sections. The remote sense error amplifier outputs a current proportional to the difference between the output voltage and the DAC voltage:

$$I_{COMP} = gm \cdot \left(V_{DAC} - \left(V_{VSP} - V_{VSN}\right)\right) \qquad \text{(eq. 1)}$$

This current is applied to a standard Type II compensation network.

Single-Phase Rail Voltage Compensation

The Remote Sense Amplifier outputs a current that is applied to a Type II compensation network formed by external tuning components CLF, RZ and CHF

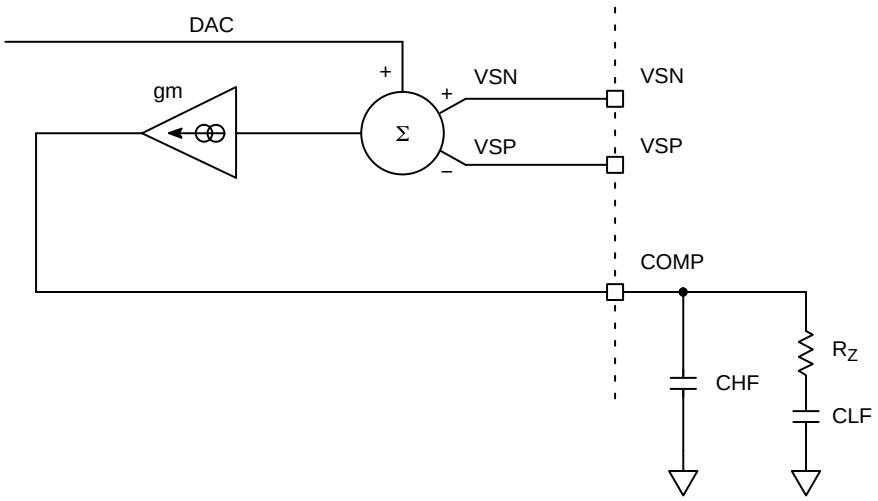


Figure 5.

Differential Current Feedback Amplifier

The NCP81255 controller has a low offset, differential amplifier to sense output inductor current. An external low-pass filter can be used to superimpose a reconstruction of the AC inductor current onto the DC current signal sensed across the inductor. The low-pass filter time constant should match the inductor L/DCR time constant by setting the filter pole frequency equal to the zero of the output inductor. This makes the filter AC output mimic the product of AC inductor current and DCR, with the same gain as the filter DC output. It is best to perform fine tuning of the filter pole during transient testing.

$$F_Z = \frac{DCR\ @\ 25^{\circ}C}{2 \cdot \pi \cdot L} \qquad \text{(eq. 2)}$$

$$F_P = \frac{1}{2 \cdot \pi \cdot \left(\frac{R_{PHSP} \cdot (R_{TH} + R_{CSSP})}{R_{PHSP} + R_{TH} + R_{CSSP}} \right) \cdot C_{CSSP}} \qquad \text{(eq. 3)}$$

Forming the low-pass filter with an NTC thermistor (R_{TH}) placed near the output inductor, compensates both the DC gain and the filter time constant for the inductor DCR change with temperature. The values of R_{PHSP} and R_{CSSP} are set based on the effect of temperature on both the thermistor and inductor. The CSP and CSN pins are high impedance inputs, but it is recommended that the low-pass filter resistance not exceed 10 kΩ in order to avoid offset due to leakage current. It is also recommended that the voltage sense element (inductor DCR) be no less than 0.5 mΩ for sufficient current accuracy. Recommended values for the external filter components are:

R_{PHSP} = 7.68 kΩ
R_{CSSP} = 14.3 kΩ
R_{TH} = 100 kΩ, Beta = 4300

$$C_{CSSP} = \frac{L_{PHASE}}{\frac{R_{PHSP} \cdot (R_{TH} + R_{CSSP})}{R_{PHSP} + R_{TH} + R_{CSSP}} \cdot DCR} \qquad \text{(eq. 4)}$$

Using 2 parallel capacitors in the low-pass filter allows fine tuning of the pole frequency using commonly available capacitor values.

The DC gain equation for the current sense amplifier output is:

$$V_{CURR} = \frac{R_{TH} + R_{CSSP}}{R_{PHSP} + R_{TH} + R_{CSSP}} \cdot I_{OUT} \cdot DCR \qquad \text{(eq. 5)}$$

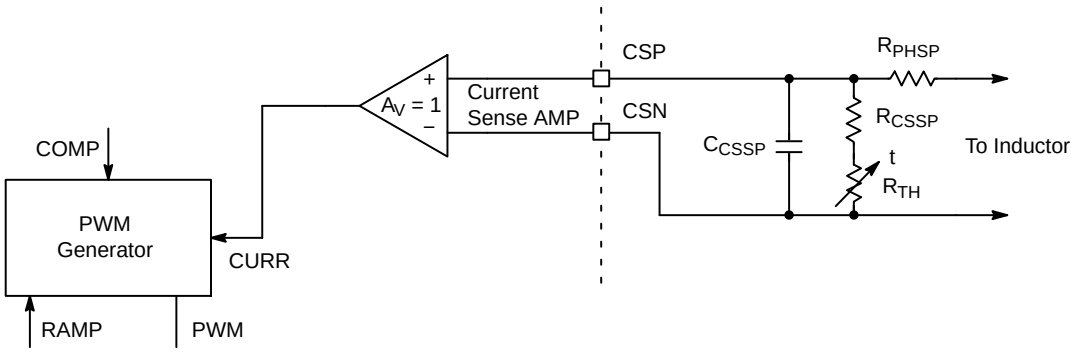


Figure 6.

The amplifier output signal is combined with the COMP and RAMP signals at the PWM comparator inputs to produce the Ramp Pulse Modulation (RPM) PWM signal.

PSYS

The PSYS pin is an analog input to the NCP81255. It is a system input power monitor that facilitates the monitoring of the total platform system power. For more details about PSYS please contact Intel, Inc.

Load-line Programming (DROOP)

An output load-line is a power supply characteristic wherein the regulated (DC) output voltage decreases by a voltage V_{DROOP}, proportional to load current. This characteristic can reduce the output capacitance required to maintain output voltage within limits during load transients faster than those to which the regulation loop can respond.

In the NCP81255, a load-line is produced by adding a signal proportional to output load current (V_{DROOP}) to the output voltage feedback signal – thereby satisfying the voltage regulator at an output voltage reduced proportional to load current. V_{DROOP} is developed across a resistance between the VSP pin and the output voltage sense point.

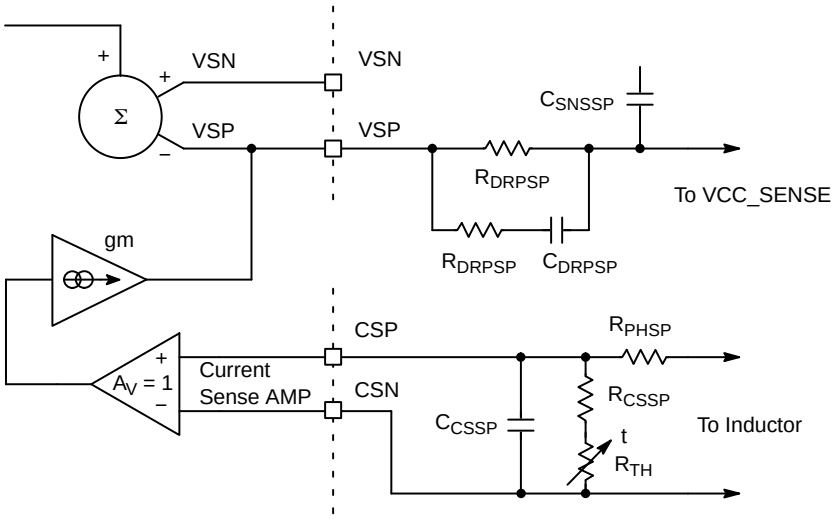


Figure 7.

$$V_{DROOP} = R_{DRPSP} \cdot gm \cdot \frac{R_{TH} + R_{CSSP}}{R_{PHSP} + R_{TH} + R_{CSSP}} \cdot I_{OUT} \cdot DCR \qquad \text{(eq. 6)}$$

The loadl-ine is programmed by choosing R_{DRPSP} such that the ratio of voltage produced across R_{DRPSP} to output current is equal to the desired load-line.

$$R_{DRPSP} = \frac{\text{Loadline}}{gm \cdot DCR} \cdot \frac{R_{PHSP} + R_{TH} + R_{CSSP}}{R_{TH} + R_{CSSP}} \qquad \text{(eq. 7)}$$

I_{CC} Max

A resistor to ground on the IMAX pin programs these registers at the time the part is enabled. 10 μA is sourced from these pins to generate a voltage on the program resistor. The resistor value should be no less than 10 kΩ.

$$ICC\_MAX_{21h} = \frac{R \cdot 10\ \mu A \cdot 255\ A}{2\ V} \qquad \text{(eq. 8)}$$

Programming IOUT

The IOUT pin sources a current in proportion to the ILIMIT sink current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICC_MAX generates a 2 V signal on IOUT. A pull-up resistor from 5 V VCC can be used to offset the IOUT signal positive if needed.

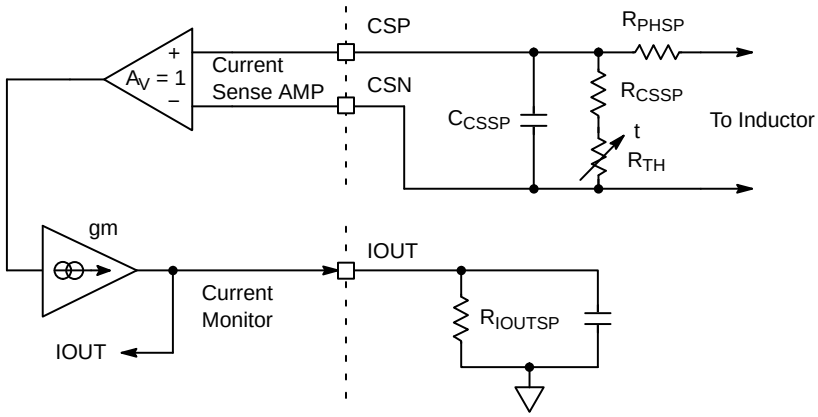


Figure 8.

$$R_{IOUTSP} = \frac{2\ V}{gm \cdot \frac{R_{TH} + R_{CSSP}}{R_{PHSP} + R_{TH} + R_{CSSP}} \cdot IccMax \cdot DCR} \qquad \text{(eq. 9)}$$

Programming the DAC Feed-Forward Filter

The NCP81255 outputs a pulse of current from the VSN pin upon each increment of the internal DAC following a DVID UP command. A parallel RC network inserted into the path from VSN to the output voltage return sense point, VSS_SENSE, causes these current pulses to temporarily decrease the voltage between VSP and VSN. This causes the output voltage during DVID to be regulated slightly higher, in order to compensate for the response of the Droop function to the inductor current flowing into the charging output capacitors. RFFSP sets the gain of the DAC feed-forward and CFFSP provides the time constant to cancel the time constant of the system per the following equations. C_{OUT} is the total output capacitance of the system.

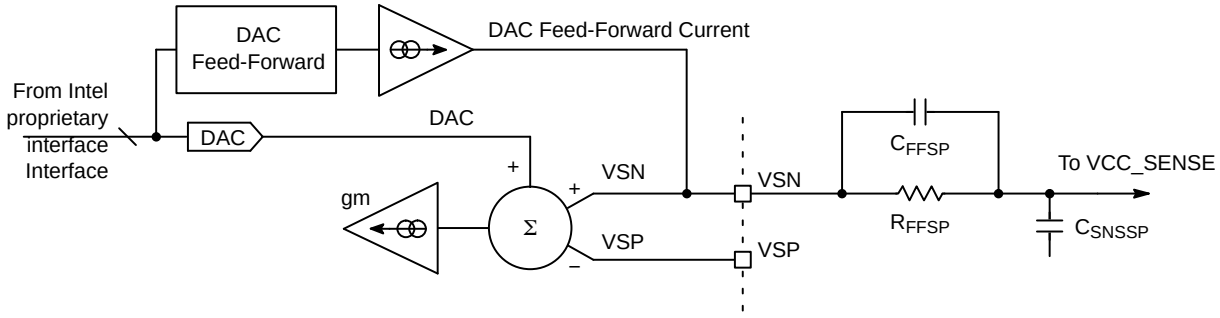


Figure 9.

$$R_{FFSP} = \frac{Loadline \cdot C_{OUT}}{1.35 \cdot 10^{-9}}\ (\Omega) \qquad C_{FFSP} = \frac{200}{R_{FFSP}}\ (nF) \qquad \text{(eq. 10)}$$

Programming the Current Limit

The current limit threshold is programmed with a resistor (R_{ILIM}) from the ILIM pin to ground. The current limit latches the single-phase rail off immediately if the ILIM pin voltage exceeds the ILIM Threshold. Set the value of the current limit resistor based on the equation shown below. A capacitor can be placed in parallel with the programming resistor to slightly delay activation of the latch if some tolerance of short over-current events is desired.

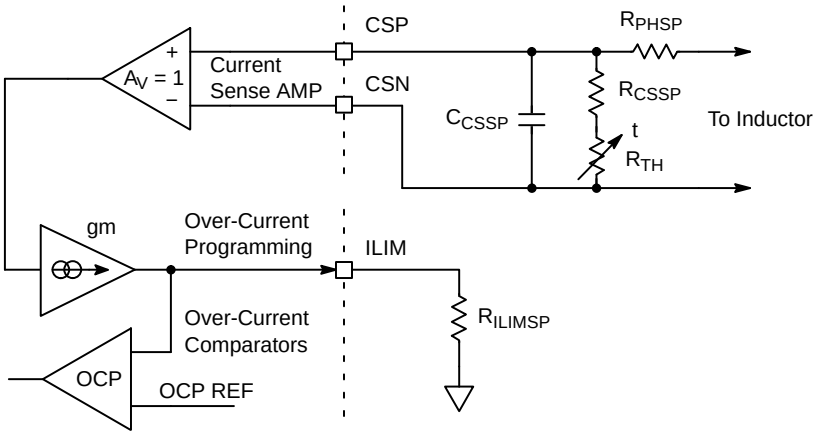


Figure 10.

$$R_{ILIMSP} = \frac{1.3\ V}{gm \cdot \frac{R_{TH} + R_{CSSP}}{R_{PHSP} + R_{TH} + R_{CSSP}} \cdot I_{OUT_{LIMIT}} \cdot DCR} \quad \text{(eq. 11)}$$

TSENSE

A temperature sense input is provided. A precision current is sourced out the TSENSE pin to generate voltage on the temperature sense network. The voltage on the temperature sense input is sampled by the internal A/D converter. A 100k NTC similar to the VISHAY ERT−J1VS104JA should be used. See the specification table for the thermal sensing voltage thresholds and source current.

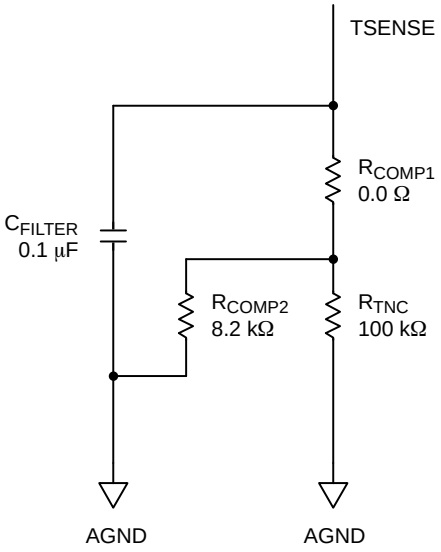


Figure 11.

Ultrasonic Mode

The switching frequency of a rail in DCM will decrease at very light loads. Ultrasonic Mode forces the switching frequency to stay above the audible range.

Input Under-Voltage Protection

The controller is protected against under-voltage on the VCC, VCCP, and VFF pins.

Under-Voltage Protection

Under-voltage protection will shut off the output similar to OCP to protect against short circuits. The threshold is specified in the parametric spec tables and is not adjustable.

Over-Current Protection (OCP)

A programmable current limit is programmed with a resistor between the ILIM pin and ground. to this resistor is compared to the ILIM Threshold Voltage (V_{CL}). If the ILIM pin voltage exceeds the lower Threshold Voltage, an internal latch-off timer starts. When the timer expires, the controller shuts down if the fault is not removed. If the voltage at the ILIM pin exceeds the higher Threshold Voltage, the controller shuts down immediately. To recover from an OCP fault, the EN pin or V_{CC} voltage must be cycled low.

Layout Notes

The NCP81255 has differential voltage and current monitoring. This improves signal integrity and reduces noise issues related to layout for easy design use. To insure proper function there are some general rules to follow. Always place the inductor current sense RC filters as close to the CSN and CSP pins on the controller as possible. Place the VCC decoupling caps as close as possible to the controller VCC pin.

Electrical Layout Considerations

Good electrical layout is a key to make sure proper operation, high efficiency, and noise reduction. Electrical layout guidelines are:

- *Power Paths:* Use wide and short traces for power paths (such as VIN, VOUT, SW, and PGND) to reduce parasitic inductance and high-frequency loop area. It is also good for efficiency improvement.
- *Power Supply Decoupling:* The device should be well decoupled by input capacitors and input loop area should be a small as possible to reduce parasitic inductance, input voltage spike, and noise emission. Usually, a small low-ESL MLCC is placed very close to VIN and PGND pins.
- *VCC Decoupling:* Place decoupling caps as close as possible to the controller VCC and VCCP pins. The filter resistor at VCC pin should be not higher than 2.2 Ω to prevent large voltage drop.
- *Switching Node:* SW node should be a copper pour, but compact because it is also a noise source.
- *Bootstrap:* The bootstrap cap and an optional resistor need to be very close and directly connected between BST and SW pins. No need to externally connect pin 10 to SW node because it has been internally connected to other SW pins.
- *Ground:* It would be good to have separated ground planes for PGND and GND and connect the two planes at one point. Directly connect GND pin to the exposed panda then connect to GND ground plane through vias.
- *Voltage Sense:* Use Kelvin sense pair and arrange a “quiet” path for the differential output voltage sense.
- *Current sense:* Careful layout for current sensing is critical for jitter minimization, accurate current limiting, and IOUT reporting. The temperature compensating thermistor should be placed as close as possible to the inductor. The wiring path should be kept as short as possible and well away from the switch node.
- *Intel proprietary interface Bus:* The Serial VID bus is a high-speed data bus and the bus routing should be done to limit noise coupling from the switching node. The signals should be routed with the Alert# line in between the Intel proprietary interface clock and Intel proprietary interface data lines. The Intel proprietary interface lines must be ground referenced and each line’s width and spacing should be such that they have nominal 50 Ω impedance with the board stack-up.

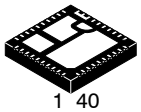
Thermal Layout Considerations

Good thermal layout helps high power dissipation from a small package with reduced temperature rise. Thermal layout guidelines are:

- The exposed pads must be well soldered on the board.
- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- More free vias are welcome to be around IC and underneath the exposed pads to connect the inner ground layers to reduce thermal impedance.
- Use large area copper pour to help thermal conduction and radiation.
- Do not put the inductor to be too close to the IC, thus the heat sources are distributed.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



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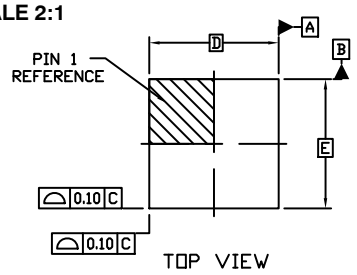
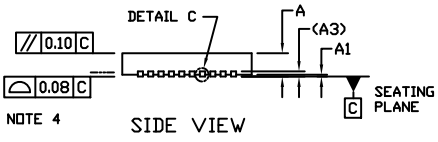
SCALE 2:1

QFN40 5x5, 0.4P
CASE 485DY
ISSUE A

DATE 26 APR 2016



TOP VIEW

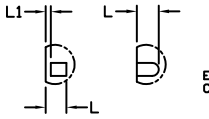


NOTE 4

SIDE VIEW

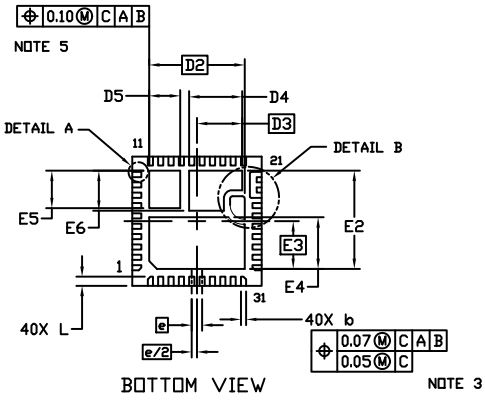
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO ALL OF THE EXPOSED PADS IN BOTH THE X AND Y AXIS.

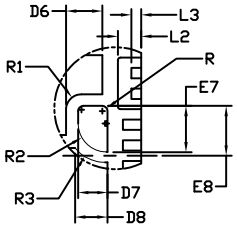


DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

DETAIL C
ALTERNATE CONSTRUCTION



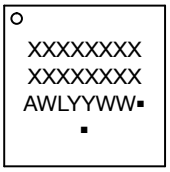
BOTTOM VIEW



DETAIL B

DIM	MILLIMETERS MIN.	MAX.
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.15	0.25
D	5.00 BSC	
D2	3.70 BSC	
D3	1.75 BSC	
D4	2.00	2.10
D5	1.15	1.25
D6	0.65	0.75
D7	0.57 REF	
D8	0.63 REF	
E	5.00 BSC	
E2	3.75	3.85
E3	1.85 BSC	
E4	1.95	2.05
E5	1.40	1.50
E6	1.50	1.60
E7	0.89 REF	
E8	0.96 REF	
e	0.40 BSC	
L	0.25	0.45
L1	---	0.15
L2	0.35	0.55
L3	0.10	0.30
R	R0.10 REF	
R1	R0.30 REF	
R2	R0.55 REF	
R3	R0.75 REF	

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT AND VIEWS ON PAGE 2

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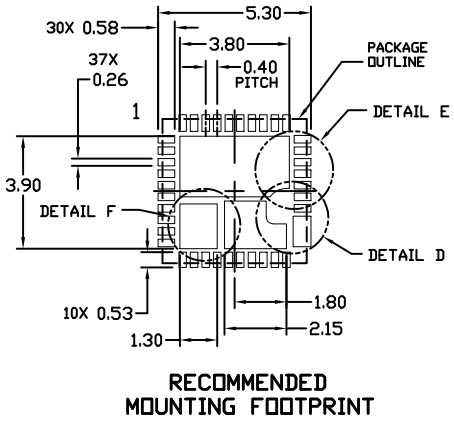
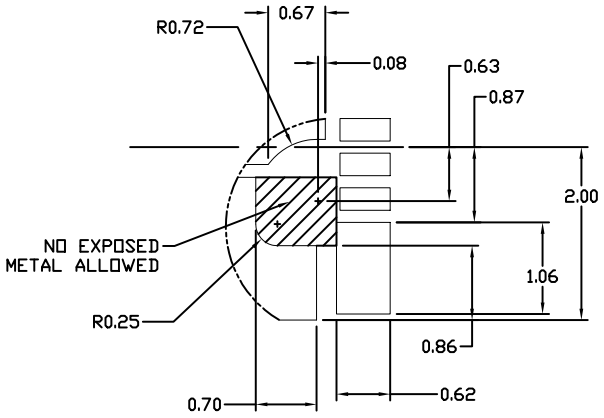
QFN40 5x5, 0.4P
CASE 485DY
ISSUE A

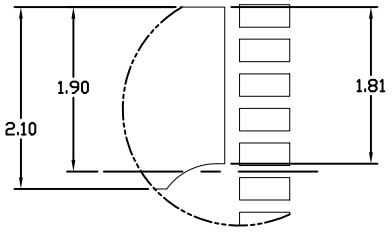
DATE 26 APR 2016



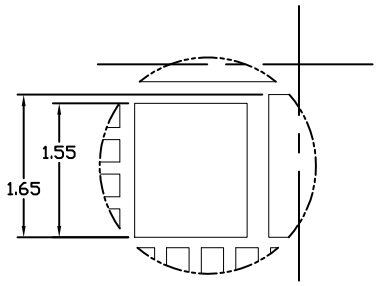
RECOMMENDED
MOUNTING FOOTPRINT



DETAIL D



DETAIL E



DETAIL F

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