

# Linear Regulator - Dual-Rail, Very Low-Dropout, Programmable Soft-Start 1.5 A NCP59748

The NCP59748 is dual-rail very low dropout voltage regulator, capable of providing an output current in excess of 1.5 A with a dropout voltage of 60 mV typ. at full load current. The devices are stable with ceramic and any other type of output capacitor  $\geq 2.2 \mu\text{F}$ . This series contains adjustable output voltage version with output voltage down to 0.8 V. Internal protection features consist of built-in thermal shutdown and output current limiting protection. User-programmable Soft-Start and Power-Good pins are available on both QFN and DFN versions.

The NCP59748 is offered in DFN10 3x3 and QFN20 5x5 packages.

## Features

- Output Current in Excess of 1.5 A
- $V_{IN}$  Range: 0.8 V to 5.5 V
- $V_{BIAS}$  Range: 2.7 V to 5.5 V
- Output Voltage Range: 0.8 V to 3.6 V
- Dropout Voltage: 60 mV at 1.5 A
- Programmable Soft-Start
- Open Drain Power Good Output
- Fast Transient Response
- Stable with Any Type of Output Capacitor  $\geq 2.2 \mu\text{F}$
- Current Limit and Thermal Shutdown Protection
- These are Pb-Free Devices

## Applications

- Consumer and Industrial Equipment Point of Load Regulation
- FPGA, DSP and Logic Power Supplies
- Switching Power Supply Post Regulation

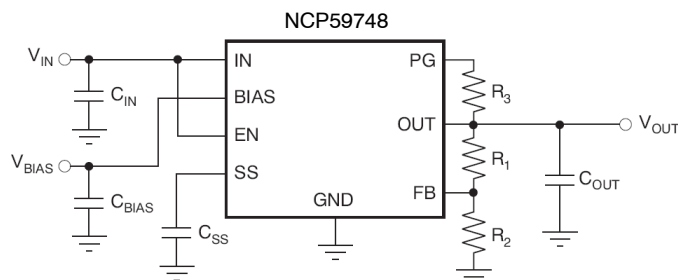
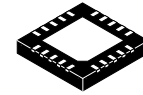


Figure 1. Typical Application Schematic

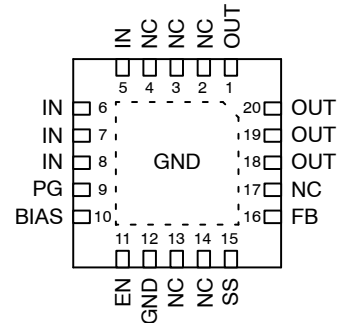


QFN20  
CASE 485DB

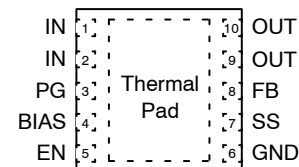


DFN10  
CASE 485C

## PIN CONNECTIONS

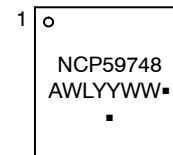


QFN20-5x5-0.65P

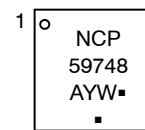


DFN10-3x3-0.5P

## MARKING DIAGRAMS



QFN20



DFN10

- A = Assembly Location
- WL = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

## ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 4 of this data sheet.



**Table 2. ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit
Input Voltage Range	$V_{IN}$	-0.3 to +6	V
Input Voltage Range	$V_{BIAS}$	-0.3 to +6	V
Enable Voltage Range	$V_{EN}$	-0.3 to +6	V
Power-Good Voltage Range	$V_{PG}$	-0.3 to +6	V
PG Sink Current	$I_{PG}$	0 to +1.5	mA
SS Pin Voltage Range	$V_{SS}$	-0.3 to +6	V
Feedback Pin Voltage Range	$V_{FB}$	-0.3 to +6	V
Output Voltage Range	$V_{OUT}$	$-0.3 \text{ to } (V_{IN} + 0.3) \leq 6$	V
Maximum Output Current	$I_{OUT}$	Internally Limited	
Output Short Circuit Duration		Indefinite	
Continuous Total Power Dissipation	$P_D$	See Thermal Characteristics Table and Formula	
Maximum Junction Temperature	$T_{JMAX}$	+150	°C
Storage Junction Temperature Range	$T_{STG}$	-55 to +150	°C
ESD Capability, Human Body Model (Note 2)	ESD <sub>HBM</sub>	2000	V
ESD Capability, Machine Model (Note 2)	ESD <sub>MM</sub>	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:  
 ESD Human Body Model tested per EIA/JESD22-A114  
 ESD Machine Model tested per EIA/JESD22-A115  
 Latch-up Current Maximum Rating tested per JEDEC standard: JESD78.

**Table 3. THERMAL CHARACTERISTICS**

Rating	Symbol	Value	Unit
Thermal Characteristics, QFN20, 5x5, 0.65P package			
Thermal Resistance, Junction-to-Ambient (Note 5)	$R_{\theta JA}$	30.5	°C/W
Thermal Resistance, Junction-to-Case (bottom) (Note 6)	$R_{\theta JC}$	4.1	°C/W
Thermal Characteristics, DFN10, 3x3, 0.5P package			
Thermal Resistance, Junction-to-Ambient (Note 5)	$R_{\theta JA}$	41.5	°C/W
Thermal Resistance, Junction-to-Case (bottom) (Note 6)	$R_{\theta JC}$	6.6	°C/W

3. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
4. Thermal data are derived by thermal simulations based on methodology specified in the JEDEC JESD51 series standards. The following assumptions are used in the simulations:  
 This data was generated with only a single device at the center of a high-K (2s2p) board with 3 in x 3 in copper area which follows the JEDEC51.7 guidelines.  
 - QFN20: The exposed pad is connected to the PCB ground layer through a 4x4 thermal via array. Vias are 0.3 mm diameter, plated. Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.  
 - DFN10: The exposed pad is connected to the PCB ground layer through a 3x2 thermal via array. Vias are 0.3 mm diameter, plated. Each of top and bottom copper layers are assumed to have thermal conductivity representing 20% copper coverage.
5. The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a high-K board, following the JEDEC51.7 guidelines with assumptions as above, in an environment described in JESD51-2a.
6. The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the IC exposed pad. Test description can be found in the ANSI SEMI standard G30-88.

**Table 4. RECOMMENDED OPERATING CONDITIONS** (Note 7)

Rating	Symbol	Min	Max	Unit
Input Voltage	$V_{IN}$	$V_{OUT} + V_{DO}$	5.5	V
Bias Voltage	$V_{BIAS}$	2.7	5.5	V
Junction Temperature	$T_J$	-40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

# NCP59748

**Table 5. ELECTRICAL CHARACTERISTICS** (At  $V_{EN} = 1.1\text{ V}$ ,  $V_{IN} = V_{OUT} + 0.3\text{ V}$ ,  $C_{BIAS} = 0.1\ \mu\text{F}$ ,  $C_{SS} = 1\ \text{nF}$ ,  $C_{IN} = C_{OUT} = 10\ \mu\text{F}$ ,  $I_{OUT} = 50\ \text{mA}$ ,  $V_{BIAS} = 5.0\ \text{V}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_J = +25^\circ\text{C}$ .)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{IN}$	Input Voltage Range		$V_{OUT} + V_{DO}$	–	5.5	V
$V_{BIAS}$	Bias Pin Voltage Range		2.7	–	5.5	V
UVLO	Undervoltage Lock-out	$V_{BIAS}$ Rising Hysteresis	– –	1.6 0.4	– –	V
$V_{REF}$	Internal Reference (Adj.)	$T_J = +25^\circ\text{C}$	0.796	0.8	0.804	V
$V_{OUT}$	Output Voltage Range	$V_{IN} = 5\ \text{V}$ , $I_{OUT} = 1.5\ \text{A}$	$V_{REF}$	–	3.6	V
	Accuracy (Note 1)	$2.97\ \text{V} < V_{BIAS} < 5.5\ \text{V}$ , $50\ \text{mA} < I_{OUT} < 1.5\ \text{A}$	–2	$\pm 0.5$	+2	%
$V_{OUT}/V_{IN}$	Line Regulation	$V_{OUT}(\text{NOM}) + 0.3 < V_{IN} < 5.5\ \text{V}$	–	0.03	–	%/V
$V_{OUT}/I_{OUT}$	Load Regulation	$50\ \text{mA} < I_{OUT} < 1.5\ \text{A}$	–	0.09	–	%/A
$V_{DO}$	$V_{IN}$ Dropout Voltage (Note 2)	$I_{OUT} = 1.5\ \text{A}$ , $V_{BIAS} - V_{OUT}(\text{NOM}) \geq 3.25\ \text{V}$ (Note 3)	–	60	165	mV
	$V_{BIAS}$ Dropout Voltage (Note 2)	$I_{OUT} = 1.5\ \text{A}$ , $V_{IN} = V_{BIAS}$	–	1.31	1.6	V
$I_{CL}$	Current Limit	$V_{OUT} = 80\% \times V_{OUT}(\text{NOM})$	2.0	–	5.5	A
$I_{BIAS}$	Bias Pin Current		–	1	2	mA
$I_{SHDN}$	Shutdown Supply Current ( $I_{GND}$ )	$V_{EN} \leq 0.4\ \text{V}$	–	1	50	$\mu\text{A}$
$I_{FB}$	Feedback Pin Current		–1	0.15	1	$\mu\text{A}$
PSRR	Power-Supply Rejection ( $V_{IN}$ to $V_{OUT}$ )	1 kHz, $I_{OUT} = 1.5\ \text{A}$ , $V_{IN} = 1.8\ \text{V}$ , $V_{OUT} = 1.5\ \text{V}$	–	60	–	dB
		300 kHz, $I_{OUT} = 1.5\ \text{A}$ , $V_{IN} = 1.8\ \text{V}$ , $V_{OUT} = 1.5\ \text{V}$	–	30	–	
	Power-Supply Rejection ( $V_{BIAS}$ to $V_{OUT}$ )	1 kHz, $I_{OUT} = 1.5\ \text{A}$ , $V_{IN} = 1.8\ \text{V}$ , $V_{OUT} = 1.5\ \text{V}$	–	50	–	dB
		300 kHz, $I_{OUT} = 1.5\ \text{A}$ , $V_{IN} = 1.8\ \text{V}$ , $V_{OUT} = 1.5\ \text{V}$	–	30	–	
Noise	Output Noise Voltage	100 Hz to 100 kHz, $I_{OUT} = 1.5\ \text{A}$	–	$25 \times V_{OUT}$	–	$\mu\text{V}_{\text{rms}}$
$t_{\text{STRT}}$	Minimum Startup Time	$R_{\text{LOAD}}$ for $I_{OUT} = 1.0\ \text{A}$ , $C_{SS} = \text{open}$	–	200	–	$\mu\text{s}$
$I_{\text{SS}}$	Soft-Start Charging Current	$V_{SS} = 0.4\ \text{V}$	–	0.44	–	$\mu\text{A}$
$V_{\text{EN, HI}}$	Enable Input High Level		1.1	–	5.5	V
$V_{\text{EN, LO}}$	Enable Input Low Level		0	–	0.4	V
$V_{\text{EN, HYS}}$	Enable Pin Hysteresis		–	50	–	mV
$V_{\text{EN, DG}}$	Enable Pin Deglitch Time		–	20	–	$\mu\text{s}$
$I_{\text{EN}}$	Enable Pin Current	$V_{\text{EN}} = 5\ \text{V}$	–	0.1	1	$\mu\text{A}$
$V_{\text{IT}}$	PG Trip Threshold	$V_{\text{OUT}}$ Decreasing	85	90	94	% $V_{\text{OUT}}$
$V_{\text{HYS}}$	PG Trip Hysteresis		–	3	–	% $V_{\text{OUT}}$
$V_{\text{PG, LO}}$	PG Output Low Voltage	$I_{\text{PG}} = 1\ \text{mA}$ (Sinking), $V_{\text{OUT}} < V_{\text{IT}}$	–	–	0.3	V
$I_{\text{PG, LKG}}$	PG Leakage Current	$V_{\text{PG}} = 5.25\ \text{V}$ , $V_{\text{OUT}} > V_{\text{IT}}$	–	0.1	1	$\mu\text{A}$
TSD	Thermal Shutdown Temperature	Shutdown, Temperature Increasing	–	+165	–	$^\circ\text{C}$
		Reset, Temperature Decreasing	–	+140	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Adjustable devices tested at  $V_{REF}$ ; external resistor tolerance is not taken into account.
- Dropout is defined as the voltage from the input to  $V_{OUT}$  when  $V_{OUT}$  is 3% below nominal.
- 3.25 V is a test condition of this device and can be adjusted by referring to Figure 8.

**Table 6. ORDERING INFORMATION**

Device	Output Current	Output Voltage	Junction Temperature Range	Package	Shipping <sup>†</sup>
NCP59748MN1ADJTBG	1.5 A	ADJ	$-40^\circ\text{C}$ to $+125^\circ\text{C}$	DFN10	3000 / Tape & Reel
NCP59748MN2ADJTBG	1.5 A	ADJ	$-40^\circ\text{C}$ to $+125^\circ\text{C}$	QFN20	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

At  $T_J = +25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$ ,  $V_{BIAS} = 5\text{ V}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  
 $C_{IN} = 1\ \mu\text{F}$ ,  $C_{BIAS} = 4.7\ \mu\text{F}$ , and  $C_{OUT} = 10\ \mu\text{F}$ , unless otherwise noted.

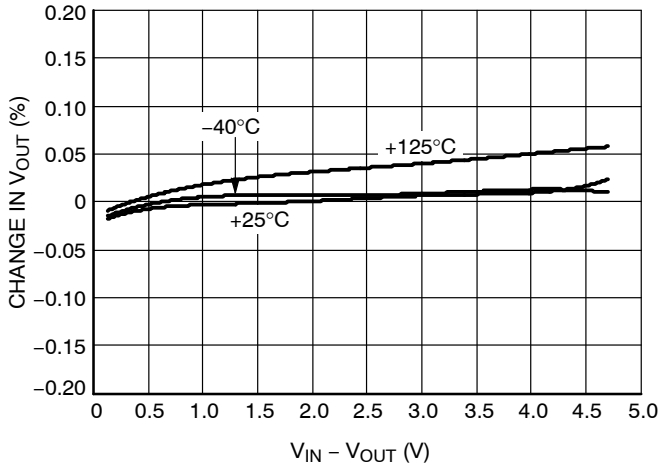


Figure 3.  $V_{IN}$  Line Regulation

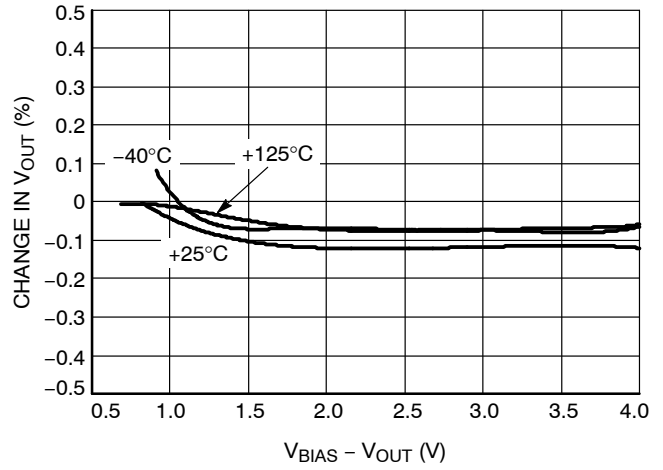


Figure 4.  $V_{BIAS}$  Line Regulation

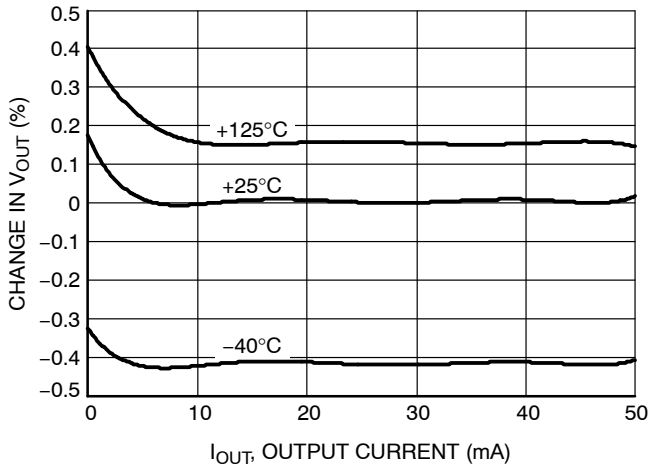


Figure 5. Load Regulation

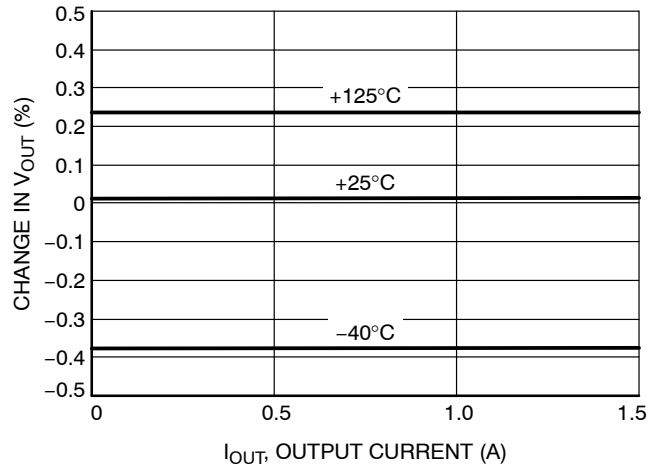


Figure 6. Load Regulation

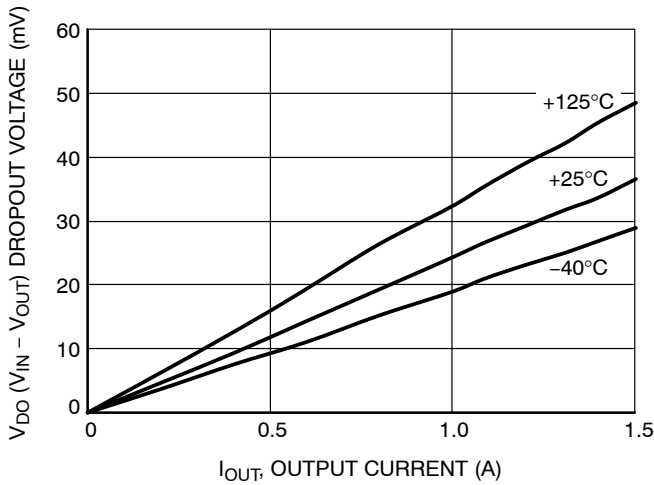


Figure 7.  $V_{IN}$  Dropout Voltage vs.  $I_{OUT}$  and Temperature  $T_J$

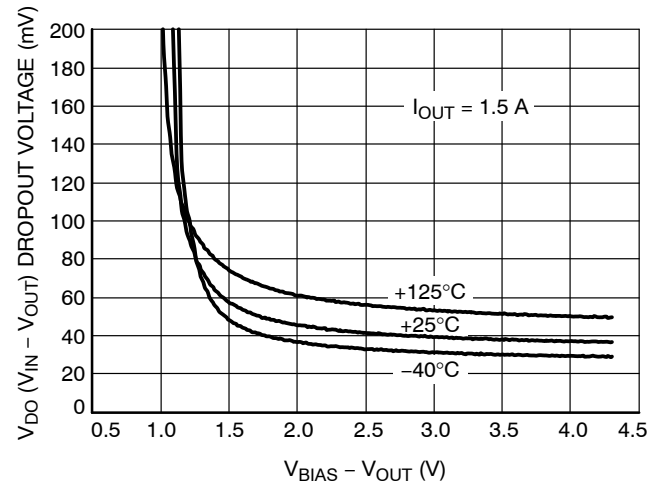


Figure 8.  $V_{IN}$  Dropout Voltage vs.  $(V_{BIAS} - V_{OUT})$  and Temperature  $T_J$

TYPICAL CHARACTERISTICS

At  $T_J = +25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$ ,  $V_{BIAS} = 5\text{ V}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  
 $C_{IN} = 1\ \mu\text{F}$ ,  $C_{BIAS} = 4.7\ \mu\text{F}$ , and  $C_{OUT} = 10\ \mu\text{F}$ , unless otherwise noted.

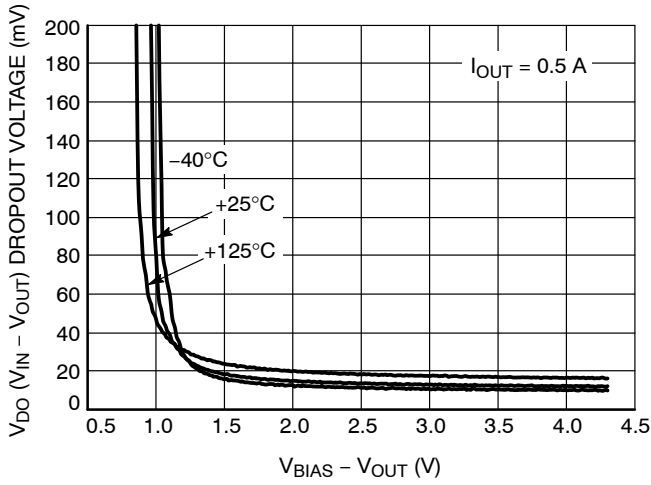


Figure 9.  $V_{IN}$  Dropout Voltage vs.  $(V_{BIAS} - V_{OUT})$  and Temperature  $T_J$

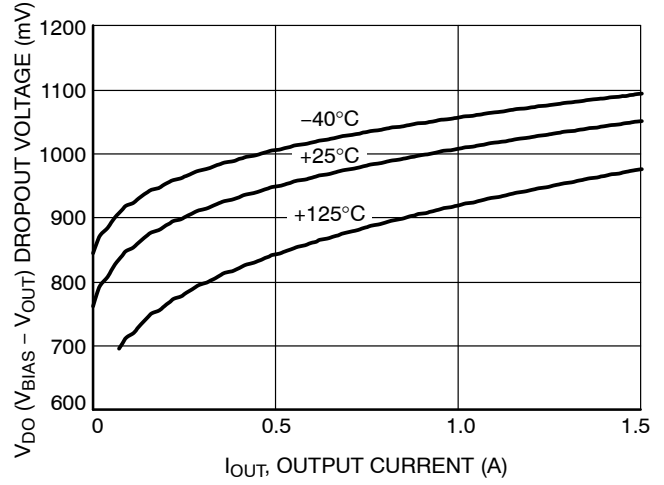


Figure 10.  $V_{BIAS}$  Dropout Voltage vs.  $I_{OUT}$  and Temperature  $T_J$

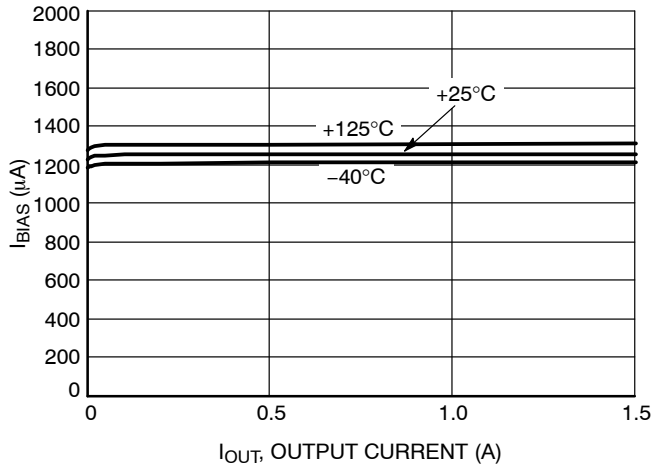


Figure 11. BIAS Pin Current vs.  $I_{OUT}$  and Temperature  $T_J$

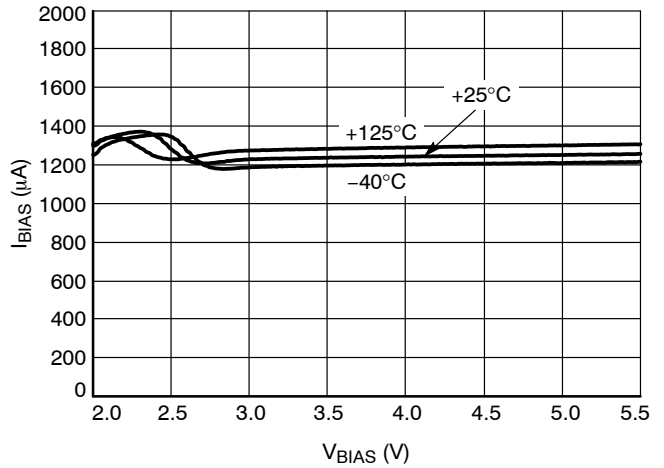


Figure 12. BIAS Pin Current vs.  $V_{BIAS}$  and Temperature  $T_J$

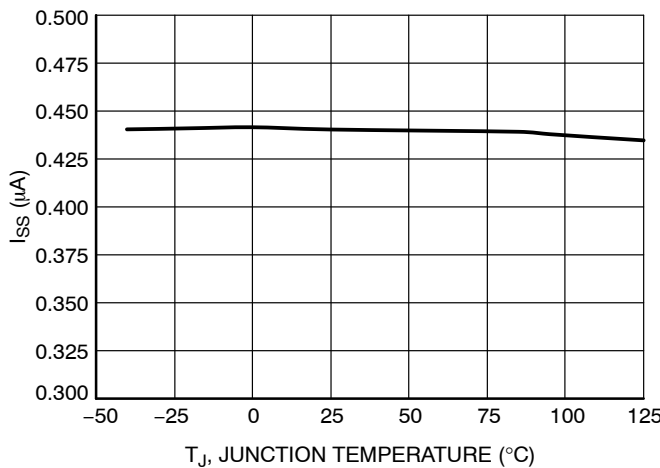


Figure 13. Soft Start Charging Current  $I_{SS}$  vs. Temperature  $T_J$

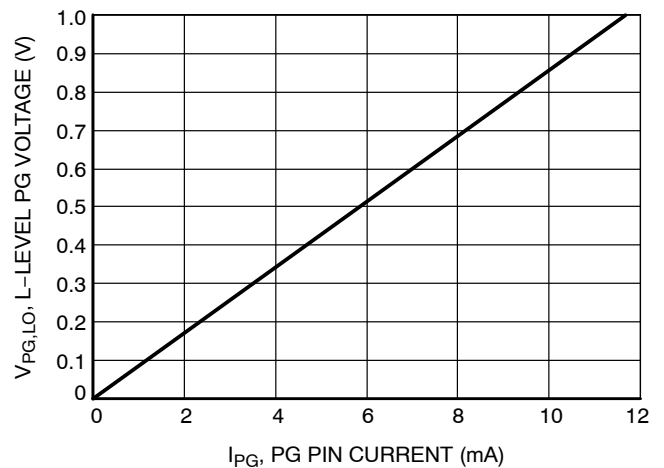


Figure 14. L-level PG Voltage vs. Current

TYPICAL CHARACTERISTICS

At  $T_J = +25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$ ,  $V_{BIAS} = 5\text{ V}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  
 $C_{IN} = 1\ \mu\text{F}$ ,  $C_{BIAS} = 4.7\ \mu\text{F}$ , and  $C_{OUT} = 10\ \mu\text{F}$ , unless otherwise noted.

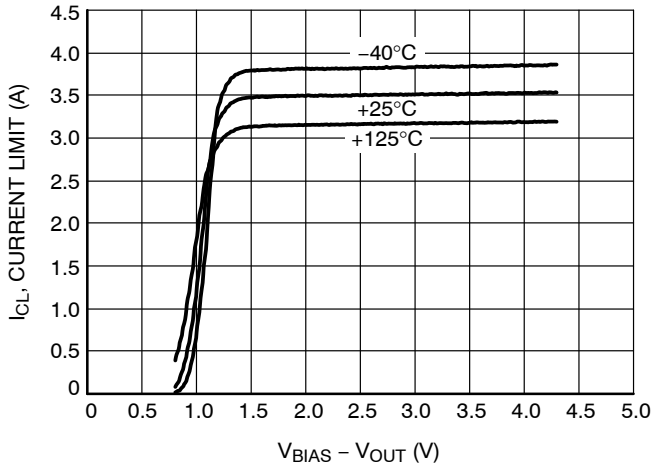


Figure 15. Current Limit vs. ( $V_{BIAS} - V_{OUT}$ )

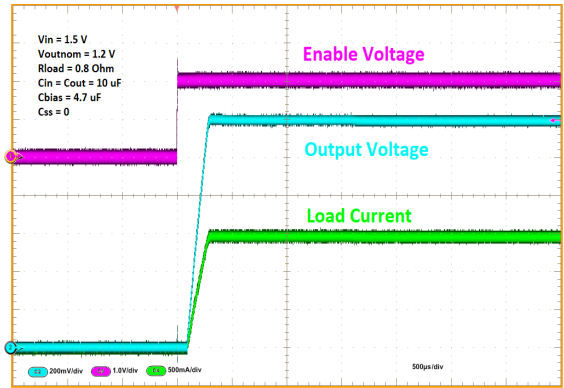


Figure 16. Start by Enable @  $C_{SS} = 0\text{ nF}$

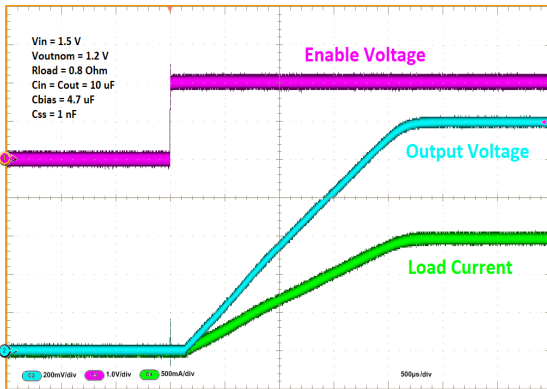


Figure 17. Start by Enable @  $C_{SS} = 1\text{ nF}$

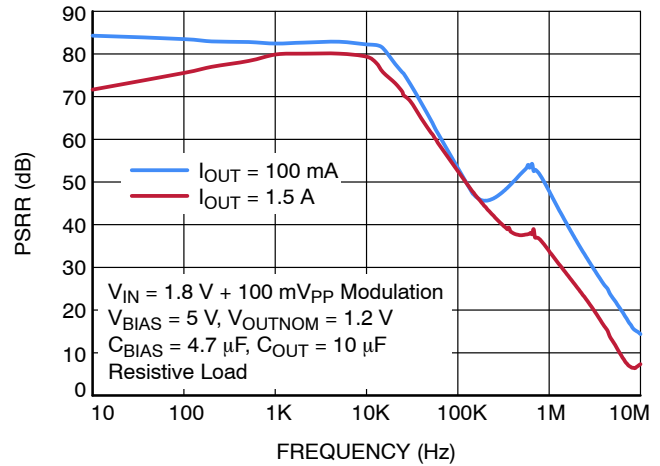


Figure 18.  $V_{IN}$  PSRR

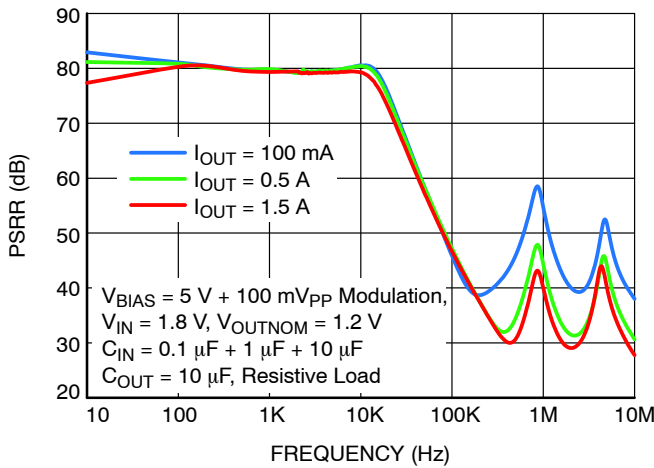


Figure 19.  $V_{BIAS}$  PSRR

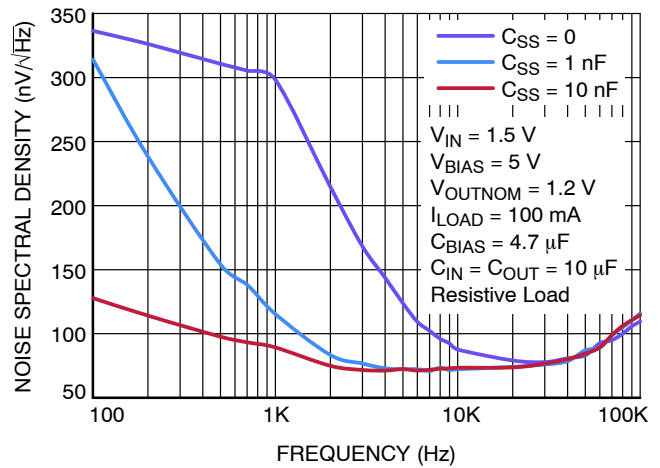


Figure 20. Noise Density vs.  $C_{SS}$

APPLICATIONS INFORMATION

The NCP59748 dual-rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from  $V_{IN}$  voltage. All the low current internal control circuitry is powered from the  $V_{BIAS}$  voltage.

The use of an NMOS pass transistor offers several advantages in applications. Unlike a PMOS topology devices, the output capacitor has reduced impact on loop stability.  $V_{in}$  to  $V_{out}$  operating voltage difference can be very low compared with standard PMOS regulators in very low  $V_{in}$  applications.

The NCP59748 offers programmable smooth monotonic start-up. The controlled voltage rising limits the inrush current what is advantageous in applications with large capacitive loads. The Voltage Controlled Soft-Start timing is programmable by external  $C_{SS}$  capacitor value.

The Enable (EN) input is equipped with internal hysteresis and deglitch filter.

Open Drain type Power Good (PG) output is available for  $V_{out}$  monitoring and sequencing of other devices.

NCP58748 is a Adjustable linear regulator. The required Output voltage can be adjusted by two external resistors. Typical application schematics is shown in Figure 21.

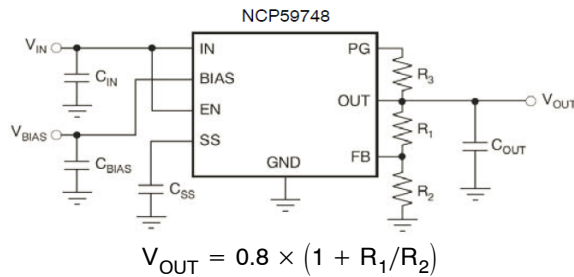


Figure 21. Typical Application Schematics

Dropout Voltage

Because of two power supply inputs  $V_{IN}$  and  $V_{BIAS}$  and one  $V_{OUT}$  regulator output, there are two Dropout voltages specified.

The first, the  $V_{IN}$  Dropout voltage is the voltage difference ( $V_{IN} - V_{OUT}$ ) when  $V_{OUT}$  starts to decrease by percents specified in the Electrical Characteristics table.  $V_{BIAS}$  is high enough, specific value is published in the Electrical Characteristics table.

The second,  $V_{BIAS}$  dropout voltage is the voltage difference ( $V_{BIAS} - V_{OUT}$ ) when  $V_{IN}$  and  $V_{BIAS}$  pins are joined together and  $V_{OUT}$  starts to decrease.

Input and Output Capacitors

The device is designed to be stable for all available types and values of output capacitors  $\geq 2.2 \mu F$ . The device is also stable with multiple capacitors in parallel, which can be of any type or value.

In applications where no low input supplies impedance available (PCB inductance in  $V_{IN}$  and/or  $V_{BIAS}$  inputs as example), the recommended  $C_{IN}$  and  $C_{BIAS}$  value is  $1 \mu F$  or

greater. Ceramic or other low ESR capacitors are recommended. For the best performance all the capacitors should be connected to the NCP59748 respective pins directly in the device PCB copper layer, not through vias having not negligible impedance.

Enable Operation

The enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet. If the enable function is not to be used then the pin should be connected to  $V_{IN}$  or  $V_{BIAS}$ .

The NCP59748 device is equipped with Output Active Discharge transistor that is pulling the output to GND through an  $1.2 k\Omega$  (typ.) resistor when the device is disabled.

To get the full functionality of Soft-Start, it is recommended to turn on the  $V_{IN}$  and  $V_{BIAS}$  supply voltages first and activate the Enable pin no sooner than  $V_{IN}$  and  $V_{BIAS}$  are on their nominal levels.

Output Noise

When the NCP59748 device reaches the end of the Soft-Start cycle, the Soft Start capacitor is switched to serve as a Noise filtering capacitor.

Output Voltage Adjust

The output voltage can be adjusted from 0.8 V to 3.6 V using resistors divider between the output and the FB input. Recommended resistor values for frequently used voltages can be found in the Table 7.

Programmable Soft-Start

The Soft-Start ramp time depends on the Soft-Start charging current  $I_{SS}$ , Soft-Start capacitor value  $C_{SS}$  and internal reference voltage  $V_{REF}$ .

The Soft-Start time can be calculated using following equations:

$$t_{SS} = C_{SS} \times (V_{REF} / I_{SS}) [s, F, V, A]$$

or in more practical units

$$t_{SS} = C_{SS} \times 0.8V / 0.44 = C_{SS} \times 1.82$$

where

$t_{SS}$  = Soft-Start time in milliseconds

$C_{SS}$  = Soft-Start capacitor value in nano Farads

Capacitor values for frequently used Soft-Start times can be found in the Table 8.

The maximal recommended value of  $C_{SS}$  capacitor is 15 nF. For higher  $C_{SS}$  values the capacitor full discharging before new Soft-Start cycle is not guaranteed.

Power Good

Power-Good (PG) is an open-drain, active-high output that indicates the status of  $V_{OUT}$ . When  $V_{OUT}$  exceeds the PG trip threshold, the PG pin goes into a high-impedance state. When  $V_{OUT}$  is below this threshold the pin is driven to a low-impedance state. A pull-up resistor from  $10 k\Omega$  to



1 MΩ should be connected from this pin to a supply up to 5.5 V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left floating if output monitoring is not necessary.

**Current Limitation**

The internal Current Limitation circuitry allows the device to supply the full nominal current and surges but protects the device against Current Overload or Short. The response time of this protection is in the range of microseconds.

**Thermal Protection**

Internal thermal shutdown (TSD) circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When TSD activated, the regulator output turns off. When cooling down under the low temperature threshold, device output is activated again. This TSD feature is provided to prevent failures from accidental overheating.

**Table 8. CAPACITOR VALUES FOR PROGRAMMING THE SOFT-START TIME**

Soft-Start Time	C <sub>SS</sub>
0.2 ms	Open
0.5 ms	270 pF
1 ms	560 pF
5 ms	2.7 nF
10 ms	5.6 nF
18 ms	10 nF

**Table 7. RESISTOR VALUES FOR PROGRAMMING THE OUTPUT VOLTAGE**

V <sub>OUT</sub> (V)	R <sub>1</sub> (kΩ)	R <sub>2</sub> (kΩ)
0.8	Short	Open
0.9	0.619	4.99
1.0	1.13	4.53
1.05	1.37	4.33
1.1	1.87	4.99
1.2	2.49	4.99
1.5	4.12	4.75
1.8	3.57	2.87
2.5	3.57	1.69
3.3	3.57	1.15

NOTE:  $V_{OUT} = 0.8 \times (1 + R_1/R_2)$   
Resistors in the table are standard 1% types

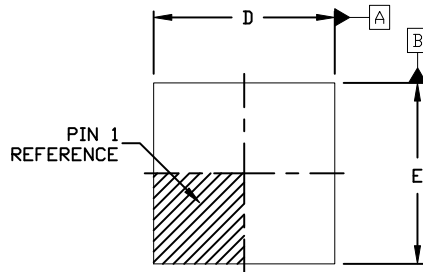
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



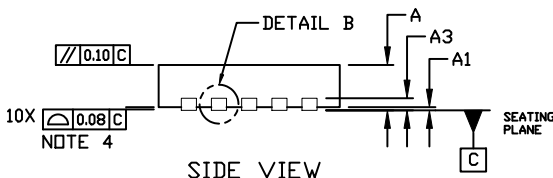
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## DFN10, 3x3, 0.5P CASE 485C ISSUE F

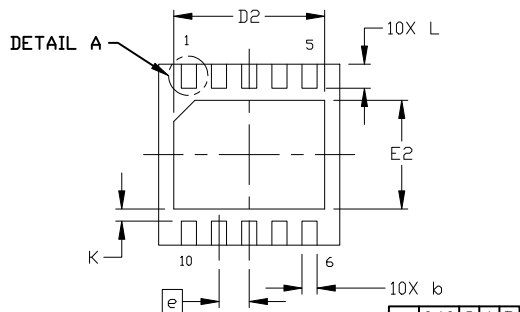
DATE 16 DEC 2021



TOP VIEW

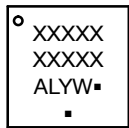


SIDE VIEW



BOTTOM VIEW

### GENERIC MARKING DIAGRAM\*



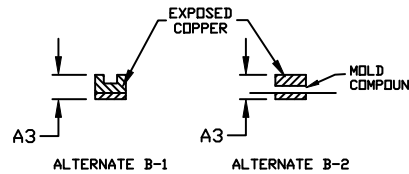
- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

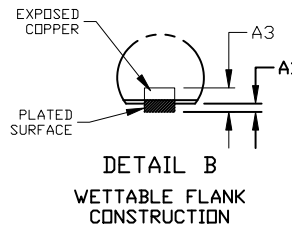
### NOTES:

1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASH MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL A AND DETAIL B ALTERNATE CONSTRUCTIONS ARE NOT APPLICABLE. WETTABLE FLANK CONSTRUCTION IS DETAIL B AS SHOWN ON SIDE VIEW OF PACKAGE.

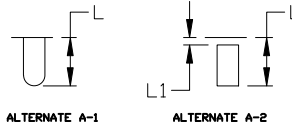


DETAIL B

ALTERNATE CONSTRUCTION



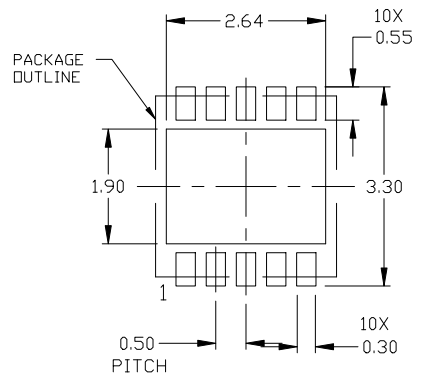
DETAIL B  
WETTABLE FLANK  
CONSTRUCTION



DETAIL A

ALTERNATE CONSTRUCTION

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3	0.20 REF		
b	0.18	0.23	0.30
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.70	1.80	1.90
e	0.50 BSC		
K	0.20 REF		
L	0.30	0.40	0.50
L1	---	---	0.03



### RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

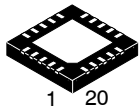
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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

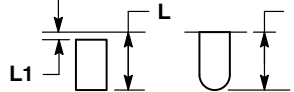
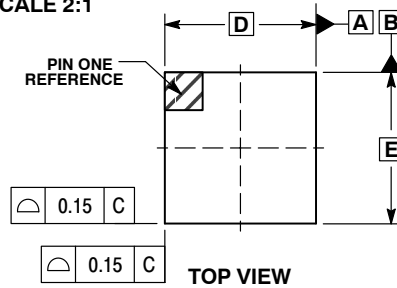
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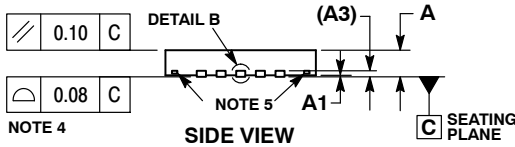
**QFN20 5x5, 0.65P**  
CASE 485DB  
ISSUE O

DATE 02 APR 2013

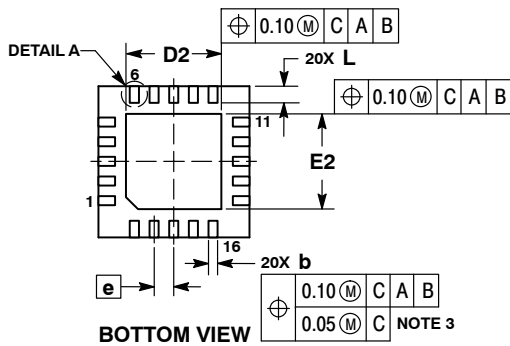
SCALE 2:1



**DETAIL A**  
ALTERNATE TERMINAL  
CONSTRUCTIONS



**DETAIL B**  
ALTERNATE  
CONSTRUCTION

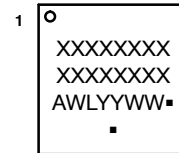


**NOTES:**

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. OPTIONAL FEATURES.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	----	0.05
A3	0.20	REF
b	0.25	0.35
D	5.00	BSC
D2	3.05	3.25
E	5.00	BSC
E2	3.05	3.25
e	0.65	BSC
L	0.45	0.65
L1	----	0.15

**GENERIC MARKING DIAGRAM\***

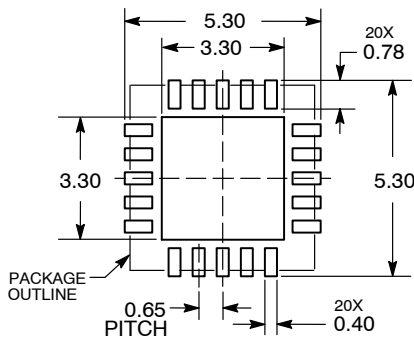


- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**RECOMMENDED SOLDERING FOOTPRINT\***



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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