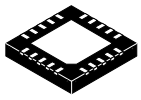
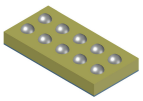
Linear Regulator - Dual-Rail, Very Low-Dropout, Programmable Soft-Start

3.0 A

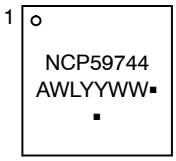
NCP59744


QFN20
CASE 485DB

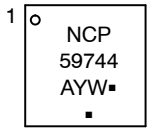

DFN10
CASE 485C


WLCSP10
CASE 567ZC

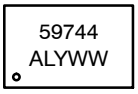
MARKING DIAGRAMS



QFN20



DFN10



WLCSP10

A = Assembly Location
WL = Wafer Lot
YY, Y = Year
WW, W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 13 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 13.

The NCP59744 is dual−rail very low dropout voltage regulator that is capable of providing an output current in excess of 3.0 A with a dropout voltage of 75 mV typ. at full load current. The devices are stable with ceramic and other low ESR output capacitors. This series contains adjustable output voltage version with output voltage down to 0.8 V. Internal protection features consist of built−in thermal shutdown and output current limiting protection. User−programmable Soft−Start and Power Good pins are available. The NCP59744 is offered in DFN10 3x3, QFN20 5x5 and WLCSP10 packages.

Features

- Output Current in Excess of 3.0 A
- 0.25% Typical Accuracy Over Line and Load
- V_{IN} Range: 0.8 V to 5.5 V
- V_{BIAS} Range: 2.2 V to 5.5 V
- Output Voltage Range: 0.8 V to 3.6 V
- Dropout Voltage: 75 mV at 3 A
- Programmable Soft Start
- Open Drain Power Good Output
- Excellent Transient Response
- Current Limit and Thermal Shutdown Protection
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Telecom and Industrial Equipment Point of Load Regulation
- FPGA, DSP and Logic Power Supplies
- Switching Power Supply Post Regulation
- Applications with Specific Start−up Time or Sequencing Requirements

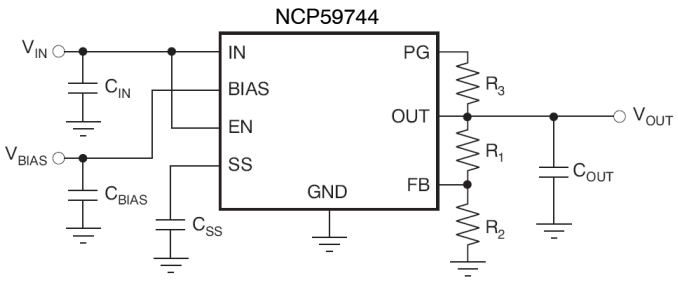
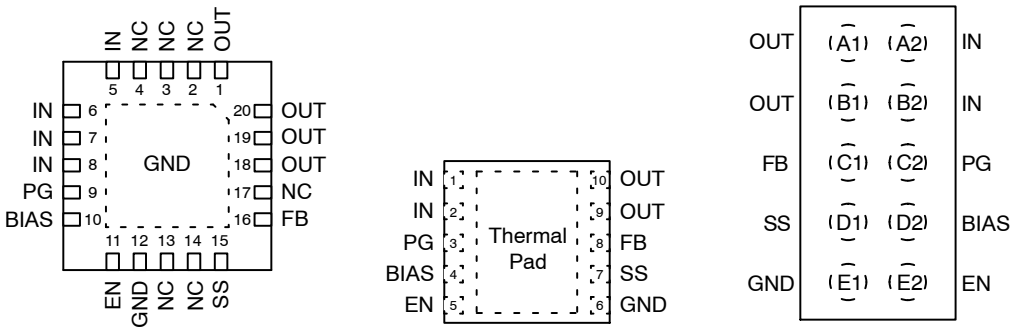


Figure 1. Typical Application Schematic



QFN20−5×5−0.65P
(Top View)

DFN10−3×3−0.5P
(Top View)

WLCSP10
(Top View)

Figure 2. Pin Connections

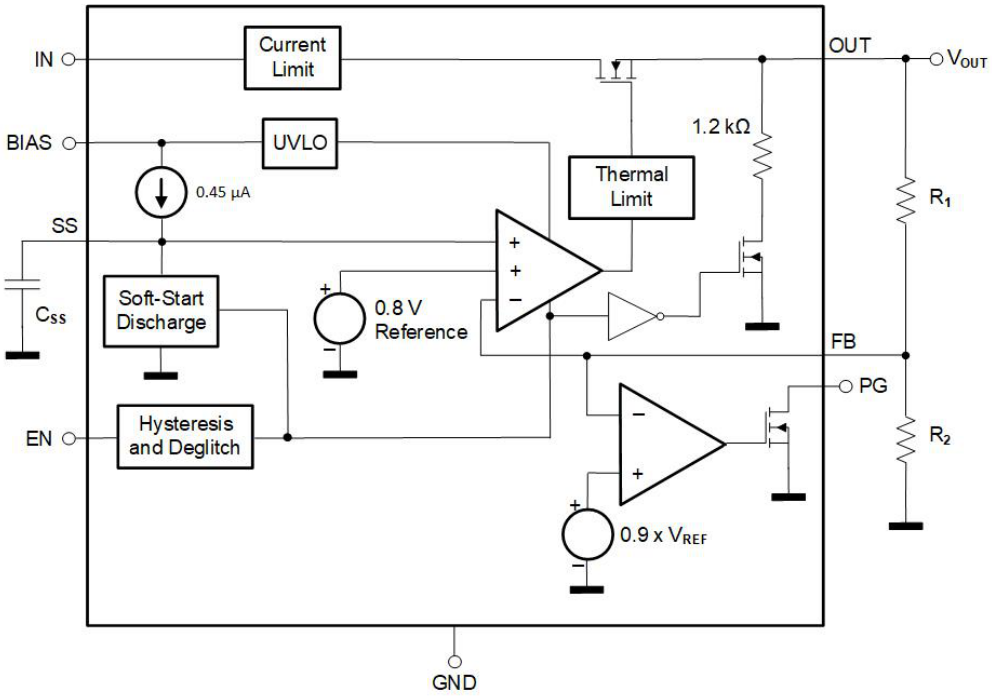


Figure 3. Simplified Schematic Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Name	DFN10	QFN20	WLCSP10	Description
IN	1, 2	5–8	A2, B2	Unregulated input to the device.
EN	5	11	E2	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left floating.
SS	7	15	D1	Soft−Start pin. A capacitor connected on this pin to ground sets the start−up time. If this pin is left floating, the regulator output soft−start ramp time is typically 200 μs.
BIAS	4	10	D2	Bias input voltage for error amplifier, reference, and internal control circuits.
PG	3	9	C2	Power−Good (PG) is an open−drain, active−high output that indicates the status of V_{OUT}. When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high−impedance state. When V_{OUT} is below this threshold the pin is driven to a low−impedance state. A pull−up resistor from 10 kΩ to 1 MΩ should be connected from this pin to a supply up to 5.5 V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left floating if output monitoring is not necessary.
FB	8	16	C1	This pin is the feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
OUT	9, 10	1, 18–20	A1, B1	Regulated output voltage. It is recommended that the output capacitor ≥ 2.2 μF.
NC	N/A	2–4, 13, 14, 17	N/A	No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top−side plane.
GND	6	12	E1	Ground
PAD/TAB				Should be soldered to the ground plane for increased thermal performance

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Input Voltage Range	V_{IN}	−0.3 to +6	V
Input Voltage Range	V_{BIAS}	−0.3 to +6	V
Enable Voltage Range	V_{EN}	−0.3 to +6	V
Power−Good Voltage Range	V_{PG}	−0.3 to +6	V
PG Sink Current	I_{PG}	0 to +1.5	mA
SS Pin Voltage Range	V_{SS}	−0.3 to +6	V
Feedback Pin Voltage Range	V_{FB}	−0.3 to +6	V
Output Voltage Range	V_{OUT}	−0.3 to $(V_{IN} + 0.3) \le 6$	V
Maximum Output Current	I_{OUT}	Internally Limited	
Output Short Circuit Duration		Indefinite	
Continuous Total Power Dissipation	P_D	See Thermal Characteristics Table and Formula	
Maximum Junction Temperature	T_{JMAX}	+150	°C
Storage Junction Temperature Range	T_{STG}	−55 to +150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114
   ESD Machine Model tested per EIA/JESD22−A115
   Latch−up Current Maximum Rating tested per JEDEC standard: JESD78.

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, DFN10, 3x3, 0.5P package			
Thermal Resistance, Junction−to−Ambient (Note 5)	$R_{\theta JA}$	41.5	°C/W
Thermal Resistance, Junction−to−Case (bottom) (Note 7)	$R_{\theta JC}$	6.6	°C/W
Thermal Characteristics, QFN20, 5x5, 0.65P package			
Thermal Resistance, Junction−to−Ambient (Note 5)	$R_{\theta JA}$	35.4	°C/W
Thermal Resistance, Junction−to−Board (Note 6)	$R_{\theta JB}$	14.7	°C/W
Thermal Resistance, Junction−to−Case (bottom) (Note 7)	$R_{\theta JC}$	3.9	°C/W
Thermal Characteristics, WLCSP10 package			
Thermal Resistance, Junction−to−Ambient (Note 5)	$R_{\theta JA}$	72	°C/W
Thermal Characterization Parameter, Junction−to−Case (top)	Ψ_{JT}	0.9	°C/W

3. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
4. Thermal data are derived by thermal simulations based on methodology specified in the JEDEC JESD51 series standards. The following assumptions are used in the simulations:
   − These data were generated with only a single device at the center of a high−K (2s2p) board with 3 in x 3 in copper area which follows the JEDEC51.7 guidelines. Top and Bottom layer 2 oz. copper, inner planes 1 oz. copper.
   − DFN10: The exposed pad is connected to the PCB ground inner layer through a 3x2 thermal via array. Vias are 0.3 mm diameter, plated. Each of top and bottom copper layers are assumed to have thermal conductivity representing 20% copper coverage.
   − QFN20: The exposed pad is connected to the PCB ground inner layer through a 4x4 thermal via array. Vias are 0.3 mm diameter, plated. Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.
5. The junction−to−ambient thermal resistance under natural convection is obtained in a simulation on a high−K board, following the JEDEC51.7 guidelines with assumptions as above, in an environment described in JESD51−2a.
6. The junction−to−board thermal resistance is simulated in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51−8.
7. The junction−to−case (bottom) thermal resistance is obtained by simulating a cold plate test on the IC exposed pad. Test description can be found in the ANSI SEMI standard G30−88.

Table 4. RECOMMENDED OPERATING CONDITIONS (Note 8)

Rating	Symbol	Min	Max	Unit
Input Voltage	V_{IN}	$V_{OUT} + V_{DO}$	5.5	V
Bias Voltage	V_{BIAS}	2.2	5.5	V
Junction Temperature	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

8. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

Table 5. ELECTRICAL CHARACTERISTICS – NCP59744FCTCADJT2G – WLCSP10
(At V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = C_{IN} = 0.1 μF, C_{OUT} = 10 μF, I_{OUT} = 50 mA, V_{BIAS} = 5.0 V, T_J = −40°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage range		V_{OUT} +V_{DO}		5.5	V
V_{BIAS}	Bias pin voltage range		2.2		5.5	V
UVLO	Undervoltage Lock−out	V_{BIAS} Rising Hysteresis	1.2 –	1.6 0.4	1.9 –	V
V_{REF}	Internal reference (Adj.)	T_J = +25°C	0.796	0.8	0.804	V
V_{OUT}	Output voltage range	V_{IN} = 5 V, I_{OUT} = 1.5 A, V_{BIAS} = 5 V	V_{REF}		3.6	V
	Accuracy (Note 9)	2.97 V ≤ V_{BIAS} ≤ 5.25 V, V_{OUT} + 1.62 V ≤ V_{BIAS} 50 mA ≤ I_{OUT} ≤ 3.0 A	−1.0	±0.25	+1.0	%
V_{OUT}/V_{IN}	Line regulation	$V_{OUT(NOM)}$ + 0.3 ≤ V_{IN} ≤ 5.5 V		0.0006		%/V
V_{OUT}/I_{OUT}	Load regulation	0 mA ≤ I_{OUT} ≤ 50 mA		0.005		%/mA
		50 mA ≤ I_{OUT} ≤ 3.0 A		0.01		%/A
V_{DO}	V_{IN} dropout voltage (Note 10)	I_{OUT} = 3.0 A, V_{BIAS} − $V_{OUT(NOM)}$ ≥ 1.62 V		75	140	mV
	V_{BIAS} dropout voltage (Note 10)	I_{OUT} = 3.0 A, V_{IN} = V_{BIAS}		1.13	1.5	V
I_{CL}	Current limit	V_{OUT} = 80% x $V_{OUT(NOM)}$	3.8	4.6	7	A
I_{BIAS}	Bias pin current	0 mA ≤ I_{OUT} ≤ 3.0 A		1.3	2	mA
I_{SHDN}	Shutdown supply current	V_{EN} ≤ 0.4 V		1	15	μA
I_{FB}	Feedback pin current	0 mA ≤ I_{OUT} ≤ 3.0 A	−250	95	250	nA
PSRR	Power−supply rejection (V_{IN} to V_{OUT})	1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		72		dB
		1 MHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		50		
	Power−supply rejection (V_{BIAS} to V_{OUT})	1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		80		dB
		1 MHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		48		
Noise	Output noise voltage	100 Hz to 100 kHz, I_{OUT} = 3 A C_{ss} = 1.0 nF		18 x V_{OUT}		μVrms
V_{TRAN}	%V_{OUT} droop during load transient	I_{OUT} = 50 mA to 3.0 A at 1 A/μs, C_{OUT} = 10 μF, V_{OUT} = 3.3 V		±1.5		%V_{OUT}
t_{STRT}	Minimum startup time	I_{OUT} = 1.5 A, C_{SS} = open		200		μs
I_{SS}	Soft−start charging current	V_{SS} = 0.4 V		0.45		μA
$V_{EN, HI}$	Enable input high level		1.1		5.5	V
$V_{EN, LO}$	Enable input low level		0		0.4	V
$V_{EN,HYS}$	Enable pin hysteresis			100		mV
$V_{EN,DG}$	Enable pin deglitch time			20		μs
I_{EN}	Enable pin current	V_{EN} = 5 V		0.3	1	μA
V_{IT}	PG trip threshold	V_{OUT} decreasing	86.5	90	93.5	%V_{OUT}
V_{HYS}	PG trip hysteresis			3		%V_{OUT}
$V_{PG, LO}$	PG output low voltage	I_{PG} = 1 mA (sinking), V_{OUT} < V_{IT}			0.3	V
$I_{PG, LKG}$	PG leakage current	V_{PG} = 5.25 V, V_{OUT} > V_{IT}		0.03	1	μA
TSD	Thermal shutdown temperature	Shutdown, temperature increasing Reset, temperature decreasing		+165 +140		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
9. Adjustable devices tested at 0.8 V; external resistor tolerance is not taken into account.
10. Dropout is defined as the voltage from the input to V_{OUT} when V_{OUT} is 2% below nominal.

Table 6. ELECTRICAL CHARACTERISTICS – NCP59744MN1ADJTBG – DFN10
(At V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = C_{IN} = 0.1 μF, C_{OUT} = 10 μF, I_{OUT} = 50 mA, V_{BIAS} = 5.0 V, T_J = −40°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage range		V_{OUT} +V_{DO}		5.5	V
V_{BIAS}	Bias pin voltage range		2.2		5.5	V
UVLO	Undervoltage Lock−out	V_{BIAS} Rising Hysteresis	1.2 –	1.6 0.4	1.9 –	V
V_{REF}	Internal reference (Adj.)	T_J = +25°C	0.796	0.8	0.804	V
V_{OUT}	Output voltage range	V_{IN} = 5 V, I_{OUT} = 1.5 A, V_{BIAS} = 5 V	V_{REF}		3.6	V
	Accuracy (Note 11)	2.97 V ≤ V_{BIAS} ≤ 5.25 V, V_{OUT} + 1.62 V ≤ V_{BIAS} 50 mA ≤ I_{OUT} ≤ 3.0 A	−1.0	±0.25	+1.0	%
V_{OUT}/V_{IN}	Line regulation	$V_{OUT(NOM)}$ + 0.3 ≤ V_{IN} ≤ 5.5 V		0.0006		%/V
V_{OUT}/I_{OUT}	Load regulation	0 mA ≤ I_{OUT} ≤ 50 mA		0.005		%/mA
		50 mA ≤ I_{OUT} ≤ 3.0 A		0.01		%/A
V_{DO}	V_{IN} dropout voltage (Note 12)	I_{OUT} = 3.0 A, V_{BIAS} − $V_{OUT(NOM)}$ ≥ 1.62 V		95	160	mV
	V_{BIAS} dropout voltage (Note 12)	I_{OUT} = 3.0 A, V_{IN} = V_{BIAS}		1.13	1.5	V
I_{CL}	Current limit	V_{OUT} = 80% x $V_{OUT(NOM)}$	3.8	4.6	7	A
I_{BIAS}	Bias pin current	0 mA ≤ I_{OUT} ≤ 3.0 A		1.3	2	mA
I_{SHDN}	Shutdown supply current	V_{EN} ≤ 0.4 V		1	15	μA
I_{FB}	Feedback pin current	0 mA ≤ I_{OUT} ≤ 3.0 A	−250	95	250	nA
PSRR	Power−supply rejection (V_{IN} to V_{OUT})	1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		72		dB
		1 MHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		50		
	Power−supply rejection (V_{BIAS} to V_{OUT})	1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		80		dB
		1 MHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		48		
Noise	Output noise voltage	100 Hz to 100 kHz, I_{OUT} = 3 A C_{ss} = 1.0 nF		18 x V_{OUT}		μVrms
V_{TRAN}	%V_{OUT} droop during load transient	I_{OUT} = 50 mA to 3.0 A at 1 A/μs, C_{OUT} = 10 μF, V_{OUT} = 3.3 V		±1.5		%V_{OUT}
t_{STRT}	Minimum startup time	I_{OUT} = 1.5 A, C_{SS} = open		200		μs
I_{SS}	Soft−start charging current	V_{SS} = 0.4 V		0.45		μA
$V_{EN, HI}$	Enable input high level		1.1		5.5	V
$V_{EN, LO}$	Enable input low level		0		0.4	V
$V_{EN,HYS}$	Enable pin hysteresis			100		mV
$V_{EN,DG}$	Enable pin deglitch time			20		μs
I_{EN}	Enable pin current	V_{EN} = 5 V		0.3	1	μA
V_{IT}	PG trip threshold	V_{OUT} decreasing	86.5	90	93.5	%V_{OUT}
V_{HYS}	PG trip hysteresis			3		%V_{OUT}
$V_{PG, LO}$	PG output low voltage	I_{PG} = 1 mA (sinking), V_{OUT} < V_{IT}			0.3	V
$I_{PG, LKG}$	PG leakage current	V_{PG} = 5.25 V, V_{OUT} > V_{IT}		0.03	1	μA
TSD	Thermal shutdown temperature	Shutdown, temperature increasing Reset, temperature decreasing		+165 +140		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
11. Adjustable devices tested at 0.8 V; external resistor tolerance is not taken into account.
12. Dropout is defined as the voltage from the input to V_{OUT} when V_{OUT} is 2% below nominal.

Table 7. ELECTRICAL CHARACTERISTICS – NCP59744MN2ADJTBG – QFN20
(At V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = C_{IN} = 0.1 μF, C_{OUT} = 10 μF, I_{OUT} = 50 mA, V_{BIAS} = 5.0 V, T_J = −40°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage range		V_{OUT} +V_{DO}		5.5	V
V_{BIAS}	Bias pin voltage range		2.2		5.5	V
UVLO	Undervoltage Lock−out	V_{BIAS} Rising Hysteresis	1.2 –	1.6 0.4	1.9 –	V
V_{REF}	Internal reference (Adj.)	T_J = +25°C	0.796	0.8	0.804	V
V_{OUT}	Output voltage range	V_{IN} = 5 V, I_{OUT} = 1.5 A, V_{BIAS} = 5 V	V_{REF}		3.6	V
	Accuracy (Note 13)	2.97 V ≤ V_{BIAS} ≤ 5.25 V, V_{OUT} + 1.62 V ≤ V_{BIAS} 50 mA ≤ I_{OUT} ≤ 3.0 A	−1.0	±0.25	+1.0	%
V_{OUT}/V_{IN}	Line regulation	$V_{OUT(NOM)}$ + 0.3 ≤ V_{IN} ≤ 5.5 V		0.0006		%/V
V_{OUT}/I_{OUT}	Load regulation	0 mA ≤ I_{OUT} ≤ 50 mA		0.005		%/mA
		50 mA ≤ I_{OUT} ≤ 3.0 A		0.01		%/A
V_{DO}	V_{IN} dropout voltage (Note 14)	I_{OUT} = 3.0 A, V_{BIAS} − $V_{OUT(NOM)}$ ≥ 1.62 V		115	195	mV
	V_{BIAS} dropout voltage (Note 14)	I_{OUT} = 3.0 A, V_{IN} = V_{BIAS}		1.13	1.5	V
I_{CL}	Current limit	V_{OUT} = 80% x $V_{OUT(NOM)}$	3.8	4.6	6	A
I_{BIAS}	Bias pin current	0 mA ≤ I_{OUT} ≤ 3.0 A		1.3	2	mA
I_{SHDN}	Shutdown supply current	V_{EN} ≤ 0.4 V		1	10	μA
I_{FB}	Feedback pin current	0 mA ≤ I_{OUT} ≤ 3.0 A	−250	95	250	nA
PSRR	Power−supply rejection (V_{IN} to V_{OUT})	1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		72		dB
		1 MHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		50		
	Power−supply rejection (V_{BIAS} to V_{OUT})	1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		80		dB
		1 MHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		48		
Noise	Output noise voltage	100 Hz to 100 kHz, I_{OUT} = 3 A C_{ss} = 1.0 nF		18 x V_{OUT}		μVrms
V_{TRAN}	%V_{OUT} droop during load transient	I_{OUT} = 50 mA to 3.0 A at 1 A/μs, C_{OUT} = 10 μF, V_{OUT} = 3.3 V		±1.5		%V_{OUT}
t_{STRT}	Minimum startup time	I_{OUT} = 1.5 A, C_{SS} = open		200		μs
I_{SS}	Soft−start charging current	V_{SS} = 0.4 V		0.45		μA
$V_{EN, HI}$	Enable input high level		1.1		5.5	V
$V_{EN, LO}$	Enable input low level		0		0.4	V
$V_{EN,HYS}$	Enable pin hysteresis			100		mV
$V_{EN,DG}$	Enable pin deglitch time			20		μs
I_{EN}	Enable pin current	V_{EN} = 5 V		0.3	1	μA
V_{IT}	PG trip threshold	V_{OUT} decreasing	86.5	90	93.5	%V_{OUT}
V_{HYS}	PG trip hysteresis			3		%V_{OUT}
$V_{PG, LO}$	PG output low voltage	I_{PG} = 1 mA (sinking), V_{OUT} < V_{IT}			0.3	V
$I_{PG, LKG}$	PG leakage current	V_{PG} = 5.25 V, V_{OUT} > V_{IT}		0.03	1	μA
TSD	Thermal shutdown temperature	Shutdown, temperature increasing Reset, temperature decreasing		+165 +140		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
13. Adjustable devices tested at 0.8 V; external resistor tolerance is not taken into account.
14. Dropout is defined as the voltage from the input to V_{OUT} when V_{OUT} is 2% below nominal.

TYPICAL CHARACTERISTICS

At T_J = +25°C, V_{OUT} = 1.5 V, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 3.3 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 μF, C_{BIAS} = 1 μF, C_{SS} = 0.01 μF, and C_{OUT} = 10 μF, unless otherwise noted.

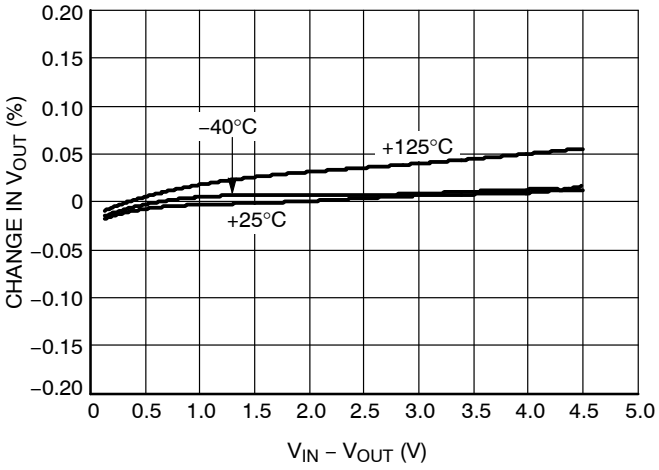


Figure 4. V_{IN} Line Regulation

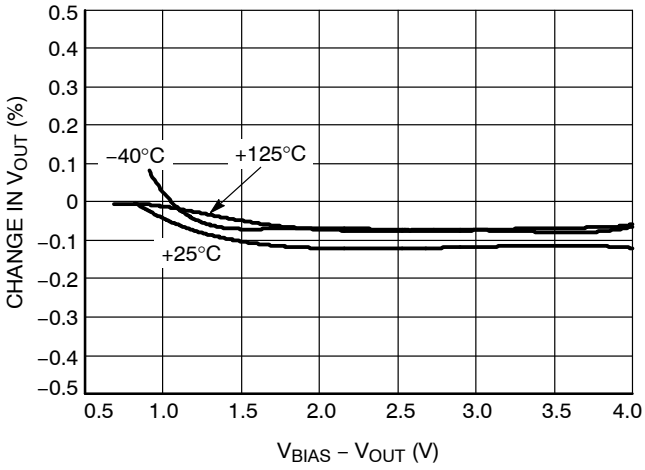


Figure 5. V_{BIAS} Line Regulation

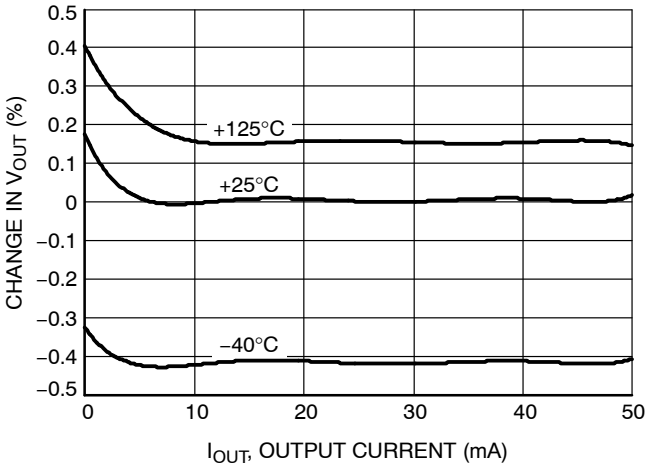


Figure 6. Load Regulation

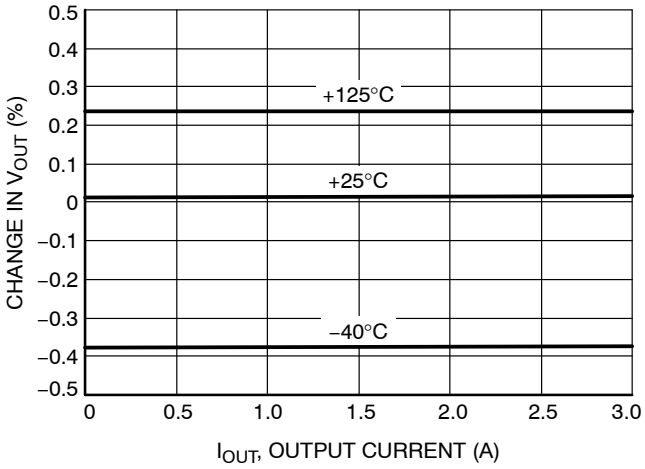


Figure 7. Load Regulation

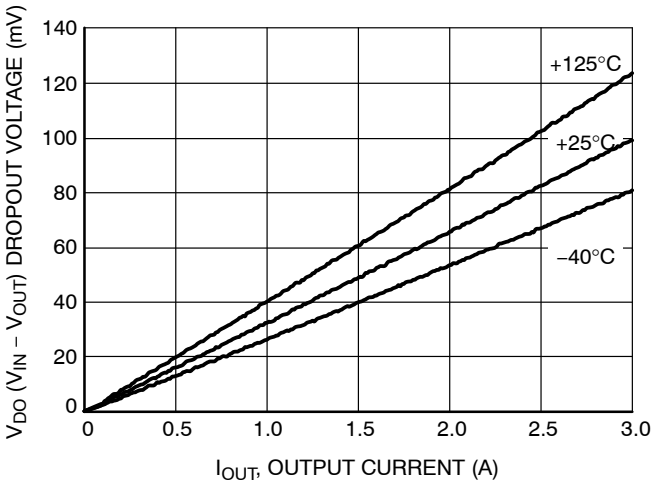


Figure 8. V_{IN} Dropout Voltage vs. I_{OUT} and Temperature T_J

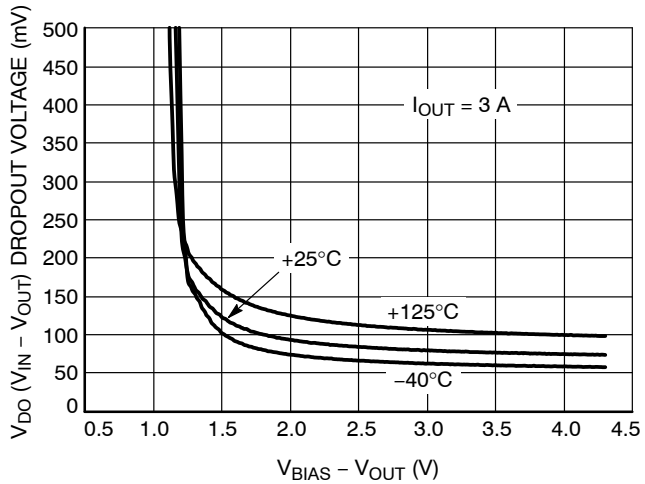


Figure 9. V_{IN} Dropout Voltage vs. (V_{BIAS} – V_{OUT}) and Temperature T_J

TYPICAL CHARACTERISTICS

At T_J = +25°C, V_{OUT} = 1.5 V, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 3.3 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 μF, C_{BIAS} = 1 μF, C_{SS} = 0.01 μF, and C_{OUT} = 10 μF, unless otherwise noted.

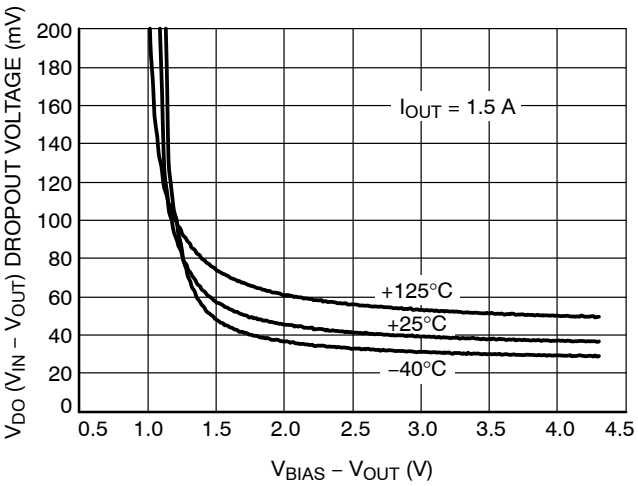


Figure 10. V_{IN} Dropout Voltage vs. (V_{BIAS} – V_{OUT}) and Temperature T_J

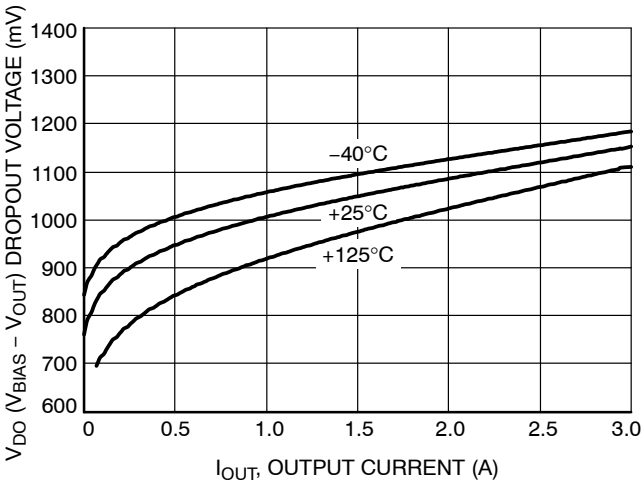


Figure 11. V_{BIAS} Dropout Voltage vs. I_{OUT} and Temperature T_J

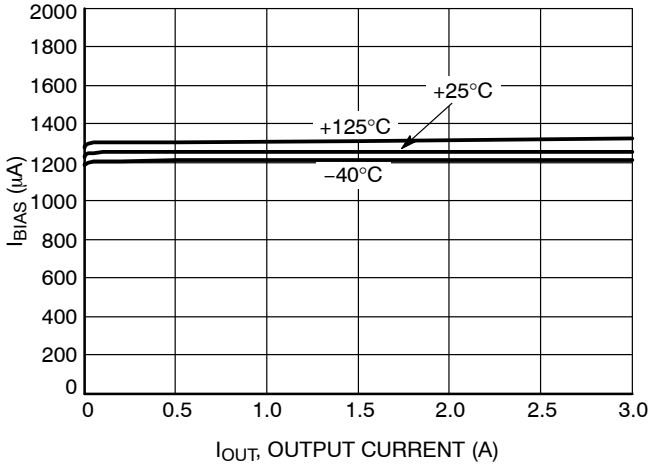


Figure 12. BIAS Pin Current vs. I_{OUT} and Temperature T_J

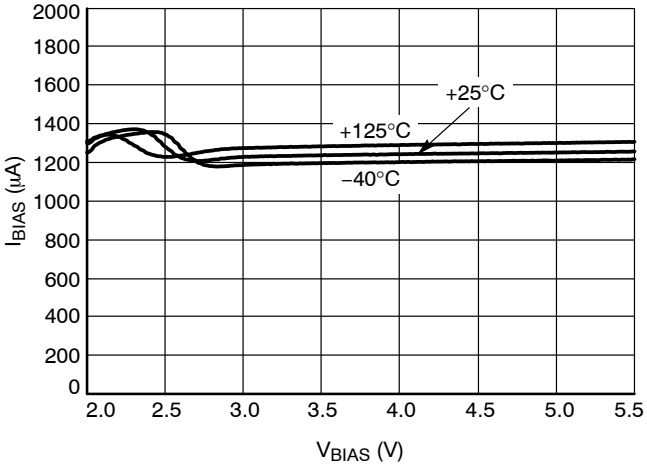


Figure 13. BIAS Pin Current vs. V_{BIAS} and Temperature T_J

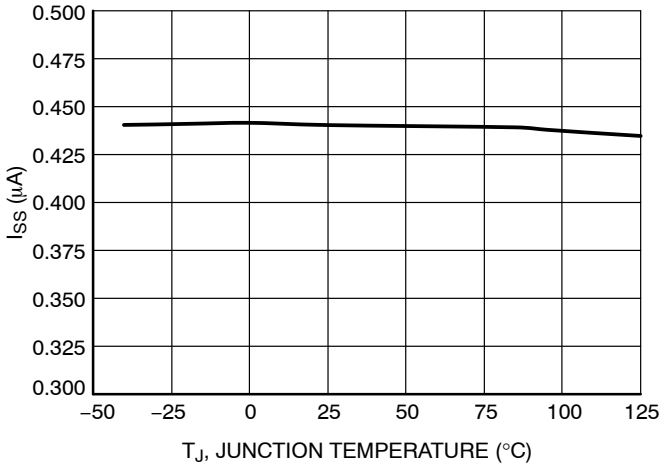


Figure 14. Soft Start Charging Current I_{SS} vs. Temperature T_J

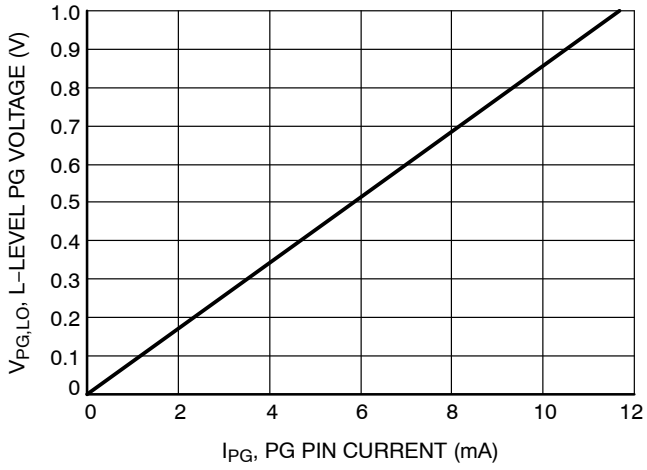


Figure 15. L–level PG Voltage vs. Current

TYPICAL CHARACTERISTICS

At T_J = +25°C, V_{OUT} = 1.5 V, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 3.3 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 μF, C_{BIAS} = 1 μF, C_{SS} = 0.01 μF, and C_{OUT} = 10 μF, unless otherwise noted.

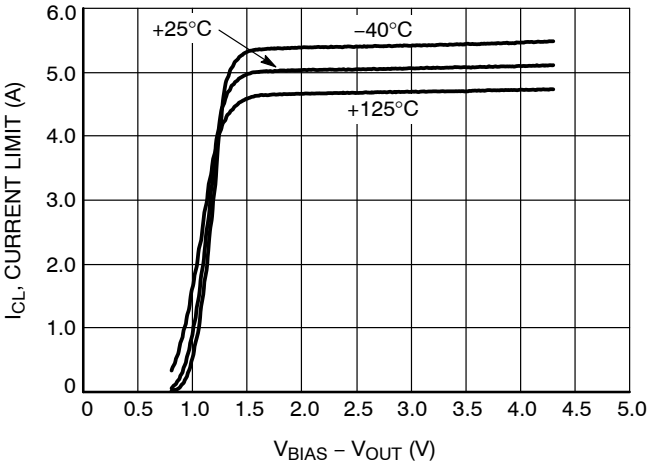


Figure 16. Current Limit vs. (V_{BIAS} − V_{OUT})

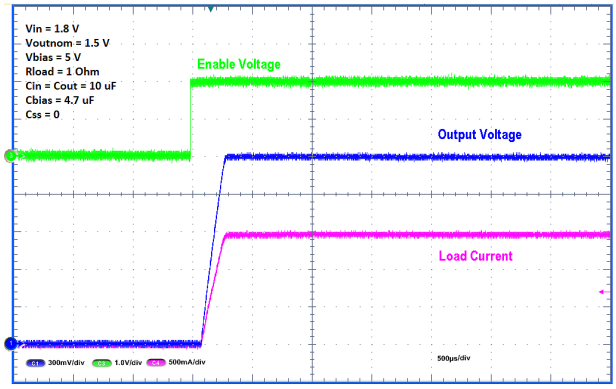


Figure 17. Start by Enable at C_{SS} = 0

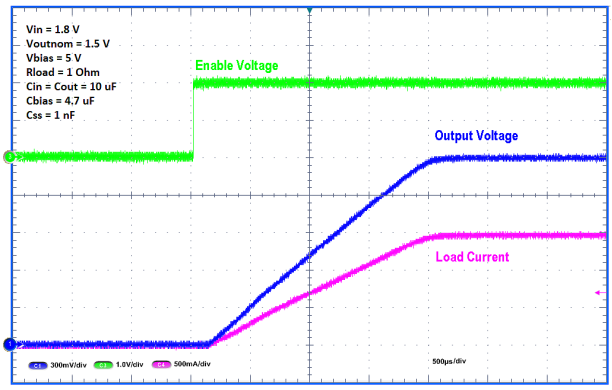


Figure 18. Start by Enable at C_{SS} = 1 nF

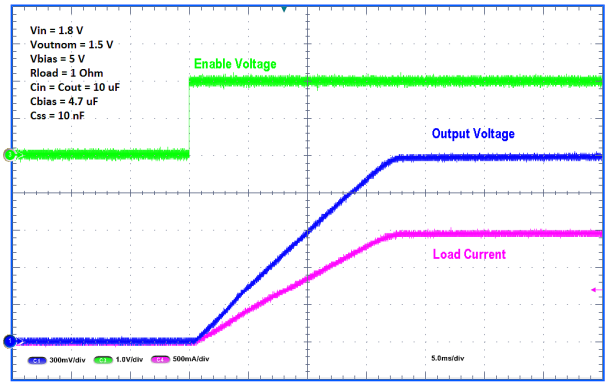


Figure 19. Start by Enable at C_{SS} = 10 nF

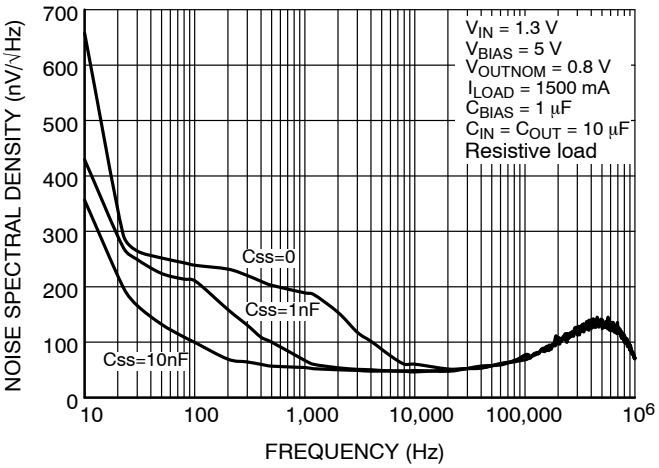


Figure 20. Output Voltage Noise Spectral Density at V_{OUT} = 0.8 V

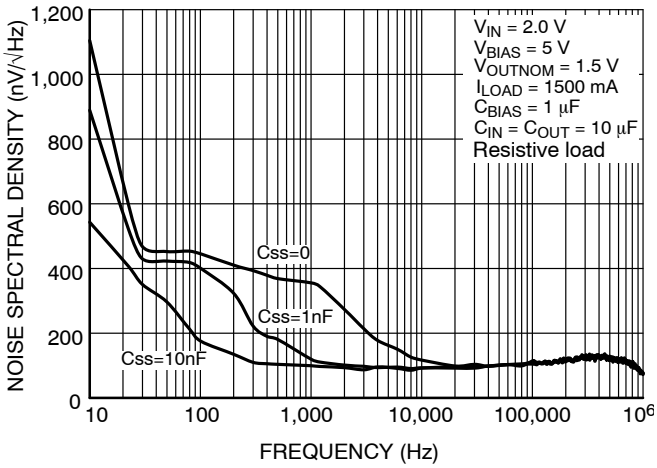


Figure 21. Output Voltage Noise Spectral Density at V_{OUT} = 1.5 V

TYPICAL CHARACTERISTICS

At T_J = +25°C, V_{OUT} = 1.5 V, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 3.3 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 μF, C_{BIAS} = 1 μF, C_{SS} = 0.01 μF, and C_{OUT} = 10 μF, unless otherwise noted.

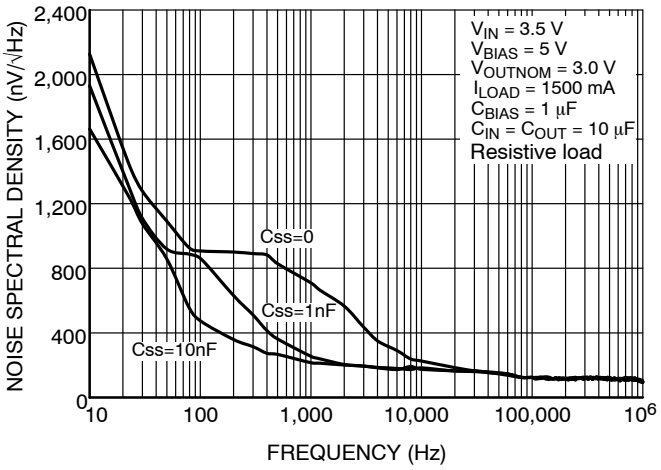


Figure 22. Output Voltage Noise Spectral Density at V_{OUT} = 3.0 V

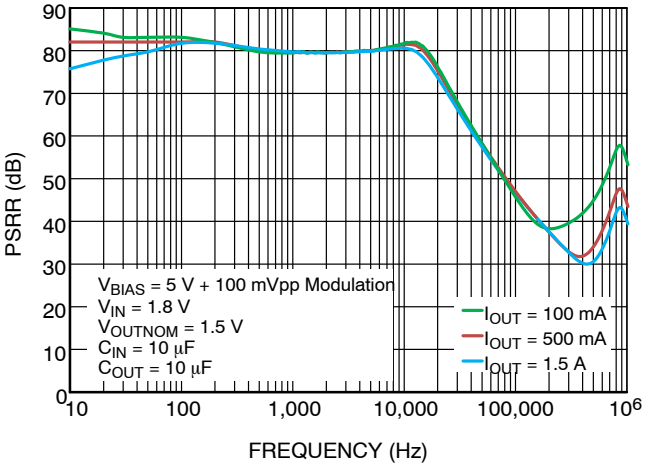


Figure 23. V_{BIAS} PSRR

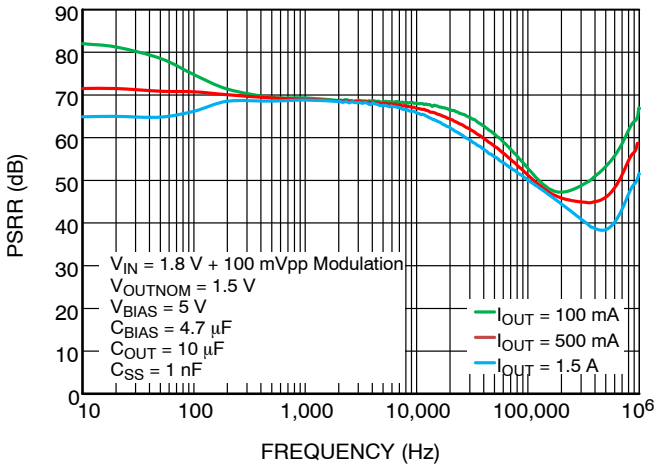


Figure 24. V_{IN} PSRR

APPLICATIONS INFORMATION

The NCP59744 dual−rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from V_{IN} voltage. All the low current internal controll circuitry is powered from the V_{BIAS} voltage.

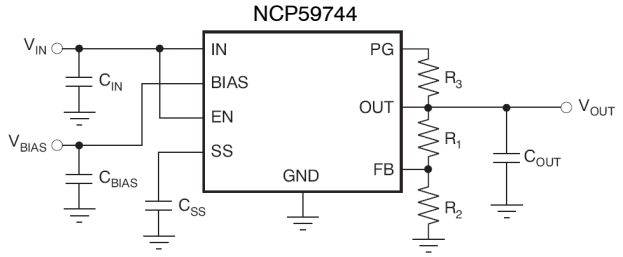
The use of an NMOS pass transistor offers several advantages in applications. Unlike a PMOS topology devices, the output capacitor has reduced impact on loop stability. Vin to Vout operating voltage difference can be very low compared with standard PMOS regulators in very low Vin applications.

The NCP59744 offers programmable smooth monotonic start-up. The controlled voltage rising limits the inrush current what is advantageous in applications with large capacitive loads. The Voltage Controlled Soft Start timing is programmable by external Css capacitor value.

The Enable (EN) input is equipped with internal hysteresis and deglitch filter.

Open Drain type Power Good (PG) output is available for Vout monitoring and sequencing of other devices.

NCP59744 is a Adjustable linear regulator. The required Output voltage can be adjusted by two external resistors. Typical application schematics is shown in Figure 25.



$$V_{OUT} = 0.8 \times (1 + R_1/R_2)$$

Figure 25. Typical Application Schematics

Dropout Voltage

Because of two power supply inputs V_{IN} and V_{BIAS} and one V_{OUT} regulator output, there are two Dropout voltages specified.

The first, the V_{IN} Dropout voltage is the voltage difference ($V_{IN} - V_{OUT}$) when V_{OUT} starts to decrease by percents specified in the Electrical Characteristics table. V_{BIAS} is high enough, specific value is published in the Electrical Characteristics table.

The second, V_{BIAS} dropout voltage is the voltage difference ($V_{BIAS} - V_{OUT}$) when V_{IN} and V_{BIAS} pins are joined together and V_{OUT} starts to decrease.

Input and Output Capacitors

The device is designed to be stable for all available types and values of output capacitors ≥ 2.2 μF. The device is also stable with multiple capacitors in parallel, which can be of any type or value.

In applications where no low input supply impedance is available (PCB inductance in Vin and/or Vbias inputs as an example) the recommended Cin and Cbias value is 1 μF or greater. In order to avoid any excessive input voltage transients caused i.e. by a sudden output short circuit conditions the input capacitor value should be sized properly for each particular application to counteract any input inductance. For Vin of 5.5 V the recommended input capacitance is 22 μF or greater. Ceramic or other low ESR capacitors are recommended. For the best performance all capacitors should be connected to the NCP59744 respective pins directly in the device PCB copper layer, not through vias having not negligible impedance.

Enable Operation

The enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet. If the enable function is not to be used then the pin should be connected to V_{IN} or V_{BIAS}.

To get the full functionality of Soft−Start, it is recommended to turn on the V_{IN} and V_{BIAS} supply voltages first and activate the Enable pin no sooner than when V_{IN} and V_{BIAS} are on their nominal levels.

The NCP59744 device is equipped with Output Active Discharge transistor that is pulling the output to GND through a 1.2 kΩ (typ.) resistor when the device is disabled.

Output Noise

When the NCP59744 device reaches the end of the Soft−Start cycle, the Soft Start capacitor is switched to serve as a Noise filtering capacitor.

Output Voltage Adjust

The output voltage can be adjusted from 0.8 V to 3.6 V using resistors divider between the output and the FB input. Recommended resistor values for frequently used voltages can be found in the Table 8.

Programmable Soft−Start

The Soft-Start ramp time depends on the Soft Start charging current I_{SS}, Soft-Start capacitor value C_{SS} and internal reference voltage V_{REF}.

The Soft –Start time can be calculated using following equations:

$t_{ss} = C_{SS}$ x (V_{REF} / I_{SS}) [s, F,V,A]

or in more practical units

$t_{SS} = C_{SS}$ x 0.8V / 0.45 = C_{SS} x 1.78

where

t_{ss} = Soft−Start time in miliseconds

C_{SS} = Soft−Start capacitor value in nano Farads

Capacitor values for frequently used Soft-Start times can be found in the Table 9.

The maximal recommended value of C_{SS} capacitor is 15 nF. For higher C_{SS} values the capacitor full discharging before new Soft-Start cycle is not guaranteed.

Power Good

Power−Good (PG) is an open−drain, active−high output that indicates the status of V_{OUT}. When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high−impedance state. When V_{OUT} is below this threshold the pin is driven to a low−impedance state. A pull−up resistor from 10 kΩ to 1 MΩ should be connected from this pin to a supply up to 5.5 V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left floating if output monitoring is not necessary.

Current Limitation

The internal Current Limitation circuitry allows the device to supply the full nominal current and surges but protects the device against Current Overload or Short.

Thermal Protection

Internal thermal shutdown (TSD) circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When TSD activated , the regulator output turns off. When cooling down under the low temperature threshold, device output is activated again. This TSD feature is provided to prevent failures from accidental overheating.

Table 8. RESISTOR VALUES FOR PROGRAMMING THE OUTPUT VOLTAGE

V_{OUT} (V)	R_1 (kΩ)	R_2 (kΩ)
0.8	Short	Open
0.9	0.619	4.99
1.0	1.13	4.53
1.05	1.37	4.33
1.1	1.87	4.99
1.2	2.49	4.99
1.5	4.12	4.75
1.8	3.57	2.87
2.5	3.57	1.69
3.3	3.57	1.15

NOTE: $V_{OUT} = 0.8 \times (1 + R_1/R_2)$
Resistors in the table are standard 1% types

Table 9. CAPACITOR VALUES FOR PROGRAMMING THE SOFT−START TIME

Soft−Start Time	C_{SS}
0.2 ms	Open
0.5 ms	270 pF
1 ms	560 pF
5 ms	2.7 nF
10 ms	5.6 nF
18 ms	10 nF

Table 10. ORDERING INFORMATION

Device	Output Current	Output Voltage	Junction Temp. Range	Package	Shipping†
NCP59744MN1ADJTBG	3.0 A	ADJ	−40°C to +125°C	DFN10 (Pb−Free)	3000 / Tape & Reel
NCP59744MN2ADJTBG	3.0 A	ADJ	−40°C to +125°C	QFN20 (Pb−Free)	3000 / Tape & Reel

DISCONTINUED (Note 15)

NCP59744FCTCADJT2G	3.0 A	ADJ	−40°C to +125°C	WLCSP10 (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

15. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

DFN10, 3x3, 0.5P
CASE 485C
ISSUE F

DATE 16 DEC 2021

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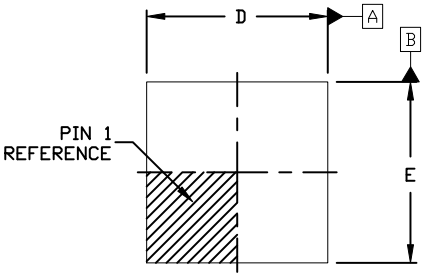
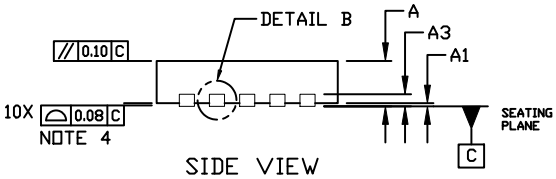
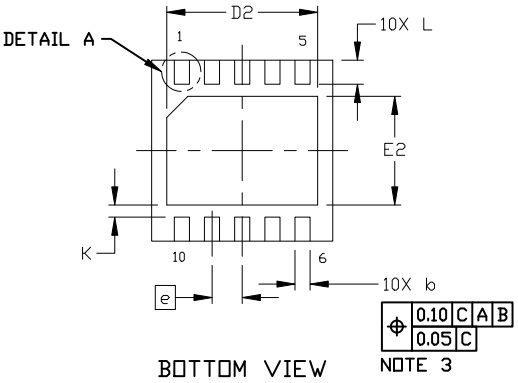


TOP VIEW

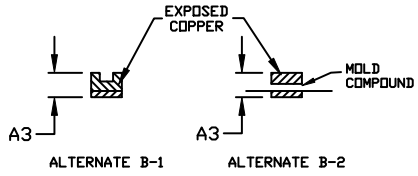


SIDE VIEW

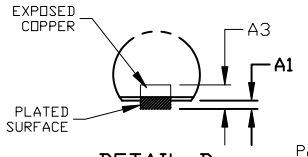


BOTTOM VIEW

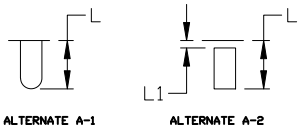
NOTES:
1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASH MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL A AND DETAIL B ALTERNATE CONSTRUCTIONS ARE NOT APPLICABLE. WETTABLE FLANK CONSTRUCTION IS DETAIL B AS SHOWN ON SIDE VIEW OF PACKAGE.



DETAIL B
ALTERNATE CONSTRUCTION

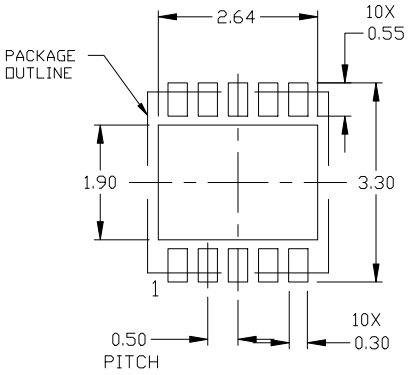


DETAIL B
WETTABLE FLANK
CONSTRUCTION



DETAIL A
ALTERNATE CONSTRUCTION

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3		0.20 REF	
b	0.18	0.23	0.30
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.70	1.80	1.90
e		0.50 BSC	
K		0.20 REF	
L	0.30	0.40	0.50
L1	---	---	0.03



RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

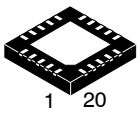
DOCUMENT NUMBER:	**98AON03161D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**DFN10, 3X3 MM, 0.5 MM PITCH**		**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

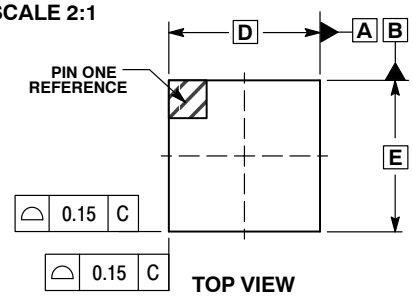
ON Semiconductor®

QFN20 5x5, 0.65P
CASE 485DB
ISSUE O

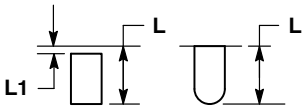
DATE 02 APR 2013



SCALE 2:1

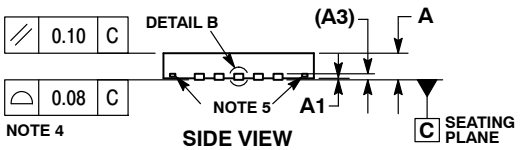


TOP VIEW

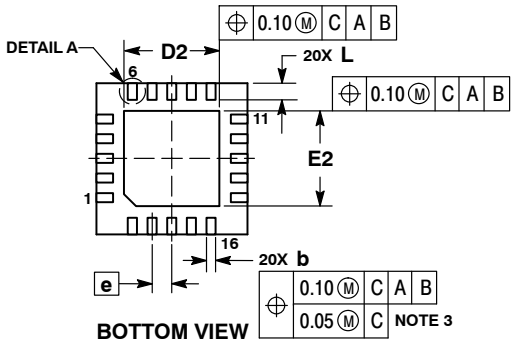


DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

DETAIL B
ALTERNATE CONSTRUCTION



SIDE VIEW



BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. OPTIONAL FEATURES.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.25	0.35
D	5.00 BSC	
D2	3.05	3.25
E	5.00 BSC	
E2	3.05	3.25
e	0.65 BSC	
L	0.45	0.65
L1	---	0.15

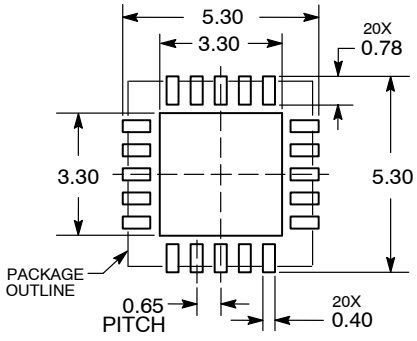
GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

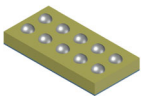
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

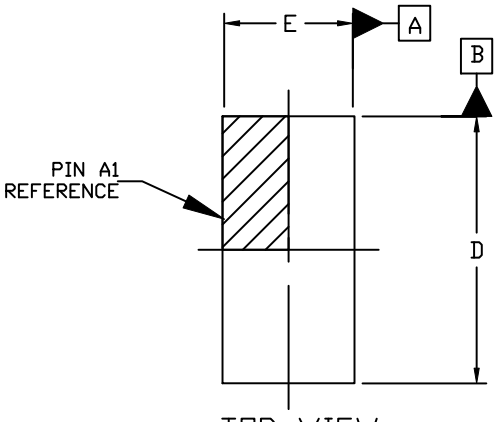
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

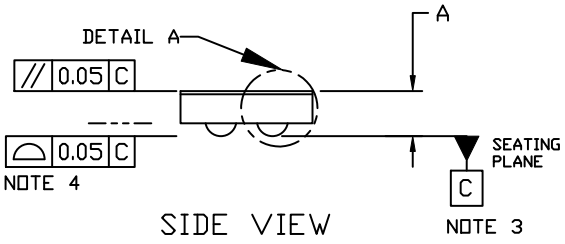
DOCUMENT NUMBER:	**98AON88183E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**QFN20 5x5, 0.65P**	**PAGE 1 OF 1**



WLCSP10, 2.075x1.025x0.35
CASE 567ZC
ISSUE O

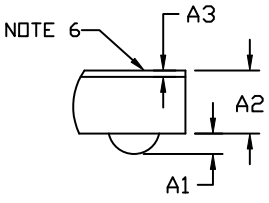
DATE 29 APR 2020



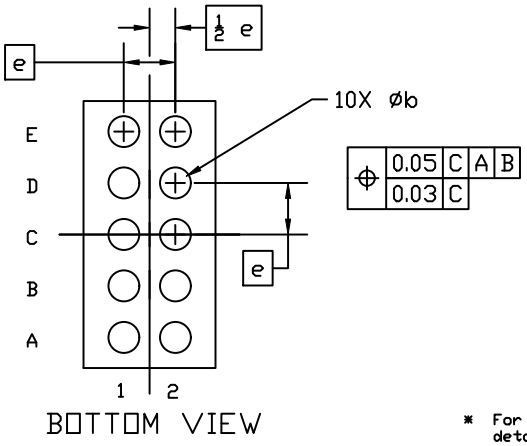


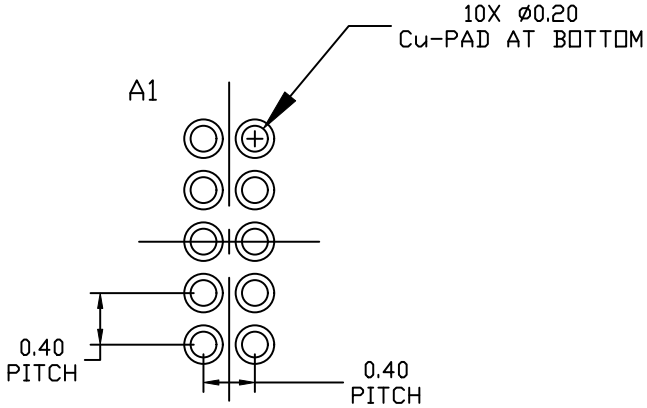
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPERICAL CROWNS OF THE CONTACT BALLS.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE CONTACT BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.
6. BACKSIDE COATING. IS OPTIONAL



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.310	0.350	0.390
A1	0.080	0.100	0.120
A2		0.25 REF	
A3		0.025 REF	
b	0.22	0.24	0.26
D	2.050	2.075	2.100
E	1.000	1.025	1.050
e		0.40 BSC	





* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WLCSP10, 2.075x1.025x0.35**	**PAGE 1 OF 1**

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