

NCP5603

High Efficiency Charge Pump Converter

The NCP5603 is an integrated circuit dedicated to the medium power White LED applications. The power conversion is achieved by means of a charge pump structure, using two external ceramic capacitors, making the system extremely tiny. The device supplies a constant voltage to the load from a low battery voltage source. It is particularly suited for the High Efficiency LED used in low cost, low power applications, with high extended battery life.

Features

- Wide Battery Supply Voltage Range: $2.7 < V_{CC} < 5.5$ V
- Automatic Operating Mode 1X, 1.5X and 2X Improves Efficiency
- Dimmable Output Current
- Up to 350 mA Output Pulsed Current
- Selectable Output Voltage
- High Efficiency Up To 90%
- Supports 2.5 kV ESD, Human Body Model
- Supports 200 V Machine Model ESD
- Low 40 mA Short Circuit Current
- Pb-Free Package is Available

Applications

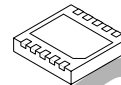
- High Power LED
- Back Light Display
- High Power Flash



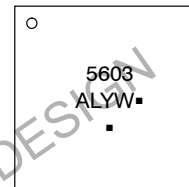
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MARKING DIAGRAM



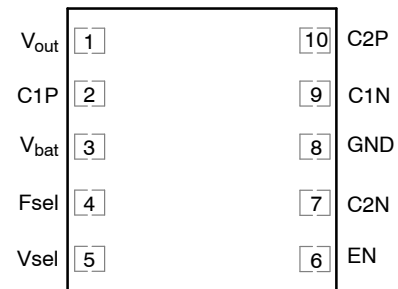
**DFN10, 3x3
MN SUFFIX
CASE 485C**



5603 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

| Device | Package | Shipping† |
|--------------|--------------------|-------------------|
| NCP5603MNR2 | DFN10 | 3000/ Tape & Reel |
| NCP5603MNR2G | DFN10 (Pb-Free) | 3000/ Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NCP5603

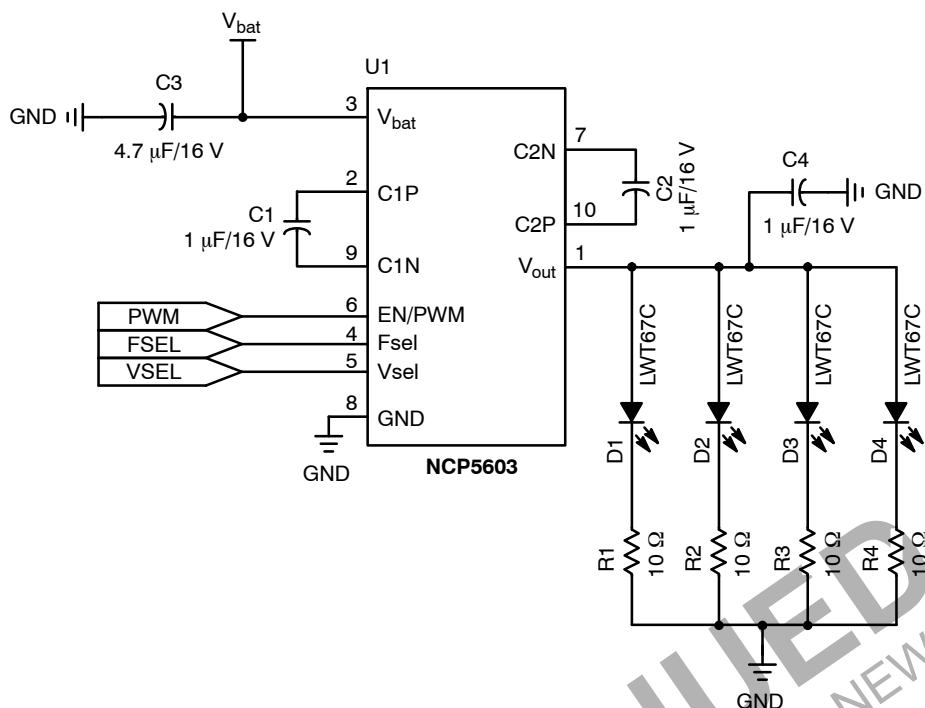


Figure 1. Typical Application

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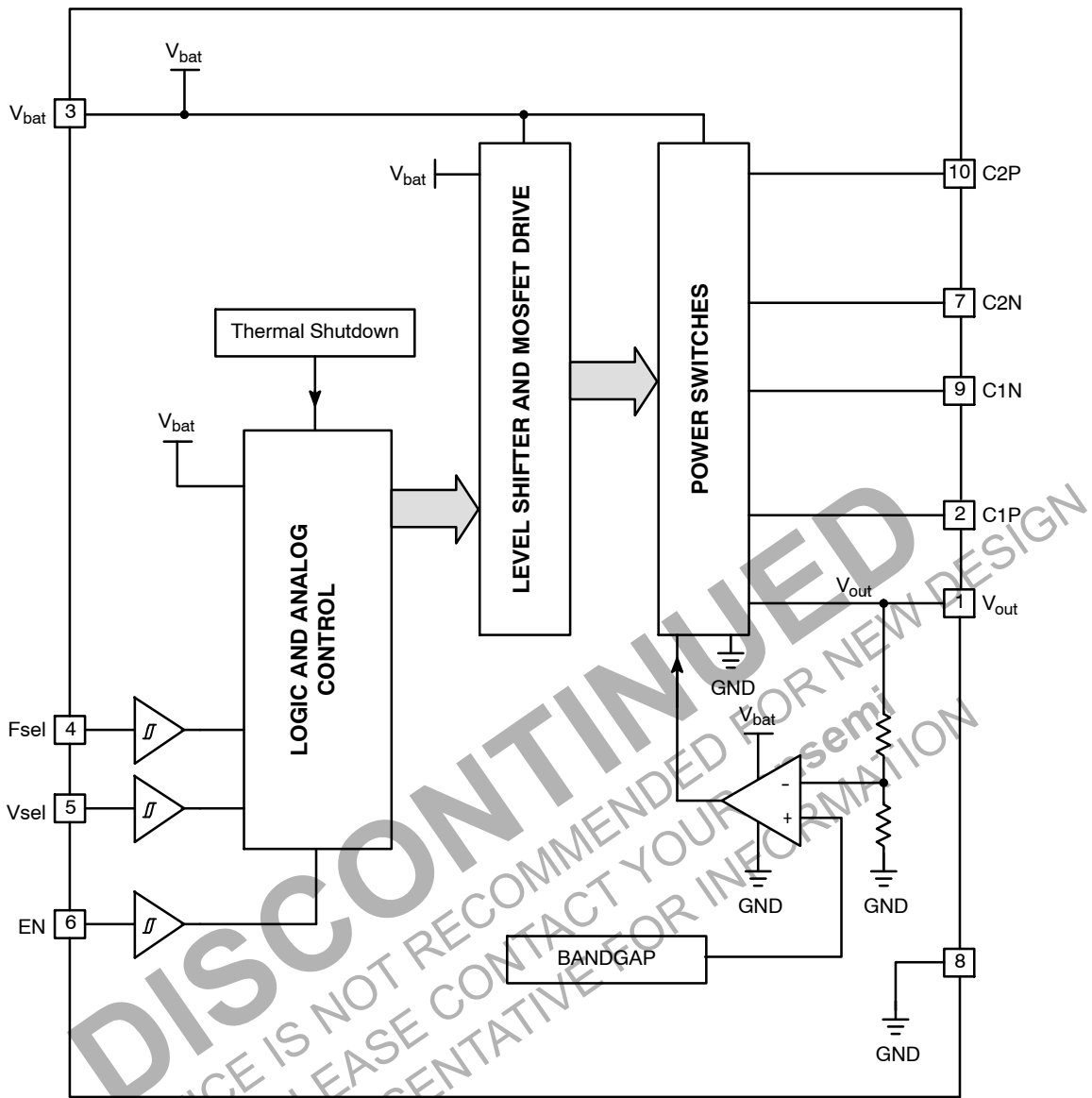


Figure 2. Block Diagram

NCP5603

PIN FUNCTION DESCRIPTION

| Pin | Symbol | Type | Description |
|-----|------------------|----------------|--|
| 1 | V _{out} | OUTPUT, PWR | This pin supplies the regulated voltage to the external LED. Since high current transients are present in this pin, care must be observed to avoid voltage spikes in the system. Good high frequency layout technique must be observed. |
| 2 | C1N | POWER | One side of the external charge pump capacitor (C _{FLY}) is connected to this pin, associated with C1P, pin 9. Using low ESR ceramic capacitor is recommended to optimize the Charge Pump efficiency. |
| 3 | V _{bat} | POWER | This pin shall be connected to the power source, and must be decoupled to Ground by a low ESR capacitor (2.2 μF/6.3 V ceramic or better (see Note 1)). |
| 4 | Fsel | INPUT, Digital | This pin is used to program the operating frequency: Fsel = 0 → Fop = 262 kHz Fsel = 1 → Fop = 650 kHz |
| 5 | Vsel | INPUT, Digital | This pin setup the output voltage: Vsel = 0 → V _{out} = 4.5 V Vsel = 1 → V _{out} = 5.0 V |
| 6 | EN/PWM | INPUT, Digital | This pin controls the activity of the NCP5603 chip: EN/PWM = Low → the chip is deactivated, the load is disconnected EN/PWM = High → the chip is activated and the load is connected to the regulated output current. The NCP5603 can operate either in a continuous mode (EN/PWM = High), or can be controlled by a PWM pulse applied to EN/PWM to dim the output light. When EN/PWM is Low, the external load is disconnected from the converter, providing a very low standby current. The pull down built-in resistance makes sure the chip is deactivated even if the EN/PWM pin is disconnected (see Note 2). |
| 7 | C2N | POWER | One side of the external charge pump capacitor (C _{FLY}) is connected to this pin, associated with C2P, pin 10. Using low ESR ceramic capacitor is recommended to optimize the Charge Pump efficiency. |
| 8 | GND | GROUND | This pin combines the Signal ground and the Power ground and must be connected to the system ground. Using good quality ground plane is mandatory to avoid spikes on the logic signal lines. |
| 9 | C1P | POWER | One side of the external charge pump capacitor (C _{FLY}) is connected to this pin, associated with C1N, pin 2. Using low ESR ceramic capacitor is recommended to optimize the Charge Pump efficiency. |
| 10 | C2P | POWER | One side of the external charge pump capacitor is connected to this pin, associated with C2N, pin 7. Using low ESR ceramic capacitor is recommended to optimize the Charge Pump efficiency. |

1. Using ceramic 16 V working voltage capacitors is recommended to compensate the DC bias effect encountered with such type of capacitors.
2. Any external impedance connected to pin 6 shall be 10 kΩ or higher.

NCP5603

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|-----------------------------|---|----------------------------|
| Power Supply Voltage | V_{bat} | 7.0 | V |
| Power Supply Current | I_{bat} | 800 | mA |
| Digital Input Pins | V_{in} | $-0.5\text{ V} < V_{bat} < V_{bat} + 0.5\text{ V} < 6.0\text{ V}$ | V |
| Digital Input Pins | I_{in} | ± 5.0 | mA |
| Output Voltage | V_{out} | 5.5 | V |
| ESD Capability (Note 3) Human Body Model Machine Model | V_{ESD} | 2.5 200 | kV V |
| DFN10, 3x3 Package Power Dissipation @ $T_{amb} = +85^{\circ}\text{C}$ Thermal Resistance, Junction-to-Air ($R_{\theta JA}$) | P_{DS} $R_{\theta JA}$ | 580 68.5 | mW $^{\circ}\text{C/W}$ |
| Operating Ambient Temperature Range | T_A | -40 to +85 | $^{\circ}\text{C}$ |
| Operating Junction Temperature Range | T_J | -40 to +125 | $^{\circ}\text{C}$ |
| Maximum Junction Temperature | T_{Jmax} | +150 | $^{\circ}\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^{\circ}\text{C}$ |
| Latchup Current Maximum Rating | | 100 mA per JEDEC standard, JESD78 | |
| Moisture Sensitivity Level (MSL) | | 1 per IPC/JEDEC standard, J-STD-020A | |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. This device series contains ESD protection and exceeds the following tests:

Human Body Model (HBM) $\pm 2.5\text{ kV}$ per JEDEC Standard: JESD22-A114

Machine Model (MM) $\pm 200\text{ V}$ per JEDEC Standard: JESD22-A115.

4. The maximum package power dissipation limit must not be exceeded.

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NCP5603

ELECTRICAL CHARACTERISTICS @ 2.85 V < V_{bat} < 5.5 V (–40°C to +85°C ambient temperature, unless otherwise noted).

| Characteristic | Pin | Symbol | Min | Typ | Max | Unit |
|---|---------|-------------------|---------------|------------|-------------------------|------|
| Power Supply | 3 | V _{bat} | 2.85 | – | 5.5 | V |
| Quiescent Current @ V _{bat} = 3.7 V, I _{out} = 0 μA @ Pulsed Clock F _{op} = 262 kHz @ Pulsed Clock F _{op} = 650 kHz @ Continuous Clock F _{op} = 262 kHz @ Continuous Clock F _{op} = 650 kHz | 3 | I _{qsc} | – | – | 0.8 1.2 – – | mA |
| Shutdown Current @ I _{out} = 0 mA, EN/PWM = L @ 2.85 < V _{bat} < 4.2 V @ V _{bat} = 5.5 V | 3 | I _{stdb} | – | – | 2.5 4.0 | μA |
| Output Voltage Regulation @ V _{sel} = 1, 2.85 V < V _{bat} < 4.3 V @ V _{sel} = 0, 2.85 V < V _{bat} < 4.3 V | 3 | V _{out} | 4.75 4.275 | 5.0 4.5 | 5.25 4.725 | V |
| Continuous DC Load Current (Note 7) C _{in} = 1.0 μF, C _{FLY} = 1.0 μF, C _{out} = 1.0 μF @ V _{sel} = 1, 3.2 V < V _{bat} < 4.3 V @ V _{sel} = 0, 3.2 V < V _{bat} < 4.3 V @ V _{sel} = 1, 2.85 V < V _{bat} < 4.3 V @ V _{sel} = 0, 2.85 V < V _{bat} < 4.3 V | 3 | I _{out} | – | – | 160 200 80 120 | mA |
| Pulsed Output Current C _{in} = 10 μF, C _{FLY} = 1.0 μF, C _{out} = 10 μF, V _{bat} = 3.6 V Pwidth = 500 ms, –40°C < T _A < +65°C | 3 | I _{FLH} | – | 350 | – | mA |
| Output Continuous Short Circuit Current, V _{out} = 0 V | 3 | I _{sch} | – | 40 | 100 | mA |
| Operating Frequency (Note 5) @ F _{sel} = 0, 2.85 V < V _{bat} < 4.5 V @ F _{sel} = 1, 2.85 V < V _{bat} < 4.5 V | | F _{op} | 210 500 | 262 650 | 320 1000 | kHz |
| Output Voltage Ripple (Note 6) F _{op} = 262 kHz, I _{out} = 60 mA (Note 7) @ C _{out} = 1.0 μF @ C _{out} = 4.7 μF | 3 | V _{PP} | – | 150 25 | – 60 | mV |
| Digital Input High Level | 4, 5, 6 | V _{IH} | 1.3 | – | – | V |
| Digital Input Low level | 4, 5, 6 | V _{IL} | – | – | 0.4 | V |
| Output Power Efficiency @ V _{bat} = 3.3 V, V _{out} = 5.0 V, I _{out} = 60 mA, F _{op} = 262 kHz @ V _{bat} = 3.9 V, V _{out} = 5.0 V, I _{out} = 160 mA, F _{op} = 650 kHz | | P _η | – | 75 84 | – – | % |
| Thermal Shut Down Protection Hysteresis | | T _{HSD} | – | 160 20 | – – | °C |

- Temperature range guaranteed by design, not production tested.
- Smaller footprint associated to lower working voltages (10 V or 6.3 V, size 0805 or 0602) can be used, but care must be observed to prevent DC bias effect on the capacitance final value. See capacitor manufacturer data sheets.
- Ceramic X7R, ESR < 100 mΩ, SMD type capacitors are mandatory to achieve the I_{out} specifications. Depending upon the PCB layout, it might be necessary to use two 2.2 μF/6.3 V/ceramic capacitors in parallel, yielding an improved V_{out} noise over the temperature range. On the other hand, care must be observed to take into account the DC bias impact on the capacitance value. See ceramic capacitor manufacturer data sheets.
- Digital inputs undershoot < – 0.30 V to ground, Digital inputs overshoot < 0.30 V to V_{bat}.

TYPICAL CHARACTERISTICS

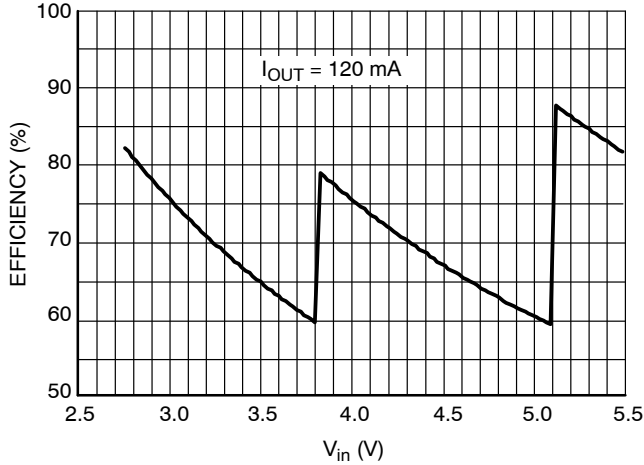


Figure 3. Operating Modes Transitions and Output Power Efficiency @ $V_{out} = 4.5\text{ V}/262\text{ kHz}$

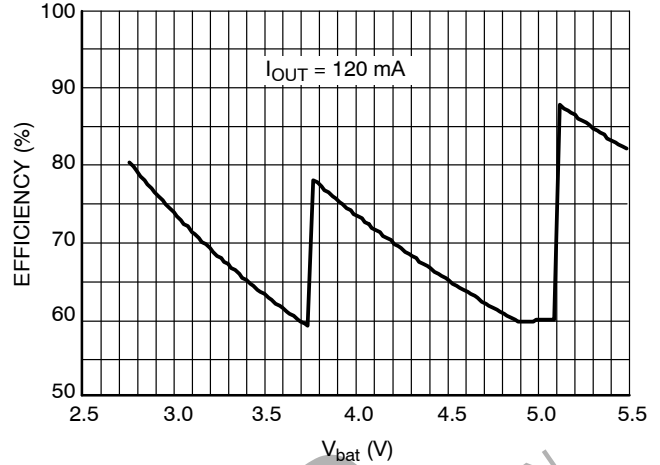


Figure 4. Operating Modes Transitions and Output Power Efficiency @ $V_{out} = 4.5\text{ V}/650\text{ kHz}$

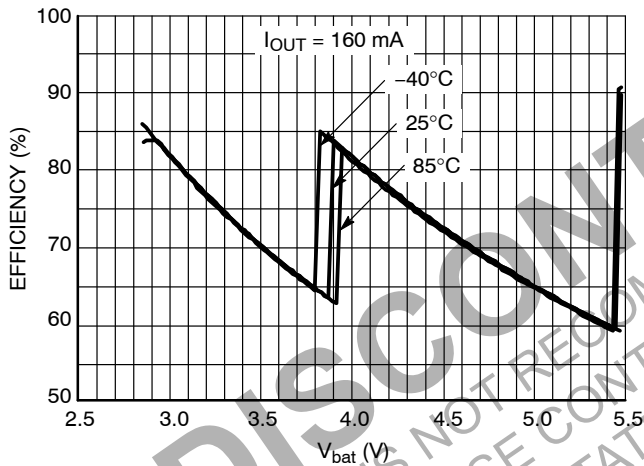


Figure 5. Operating Modes Transitions and Output Power Efficiency @ $V_{out} = 5.0\text{ V}/650\text{ kHz}$

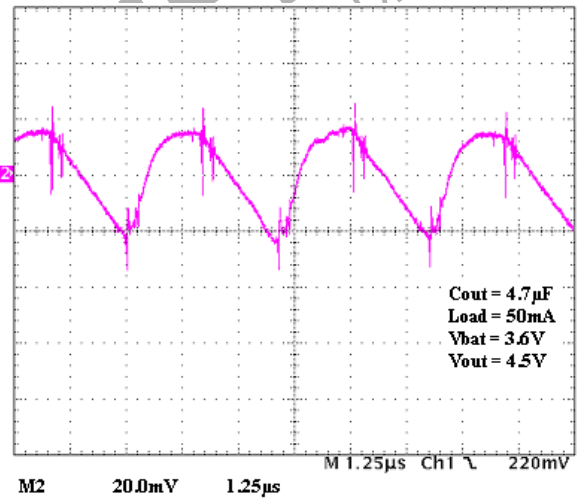


Figure 6. Typical Output Voltage Ripple

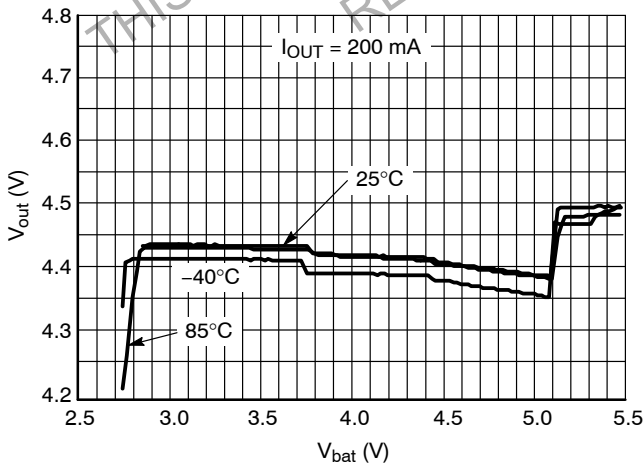
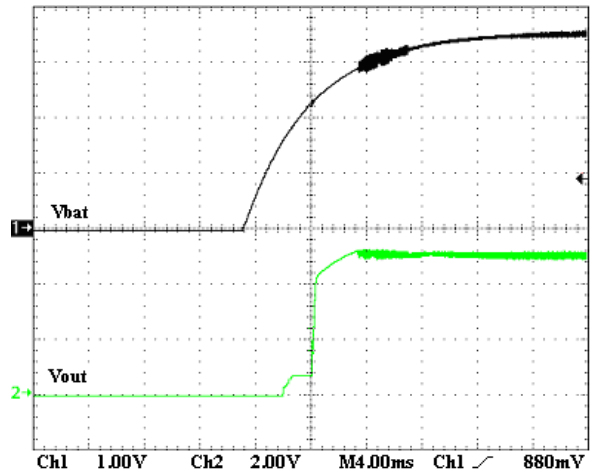


Figure 7. Typical Output Voltage Line Regulation

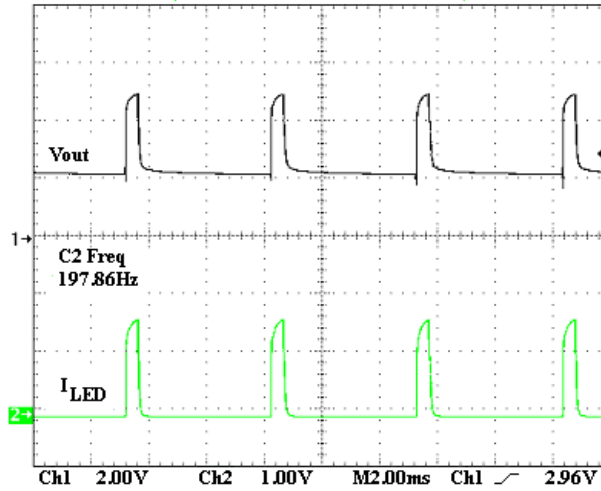


Test conditions: $V_{bat} = 3.6\text{ V}$, $V_{out} = 5\text{ V}$, Load = $4 \times \text{LW87S}$, $I_{LED} = 25\text{ mA}$

Figure 8. Output Voltage Startup from Scratch

NCP5603

TYPICAL CHARACTERISTICS



Test conditions: $V_{bat} = 3.6\text{ V}$, $V_{out} = 5\text{ V}$, Load = 4*LW87S,
 $I_{LED} = 25\text{ mA}$

Figure 9. Typical PWM Dimming

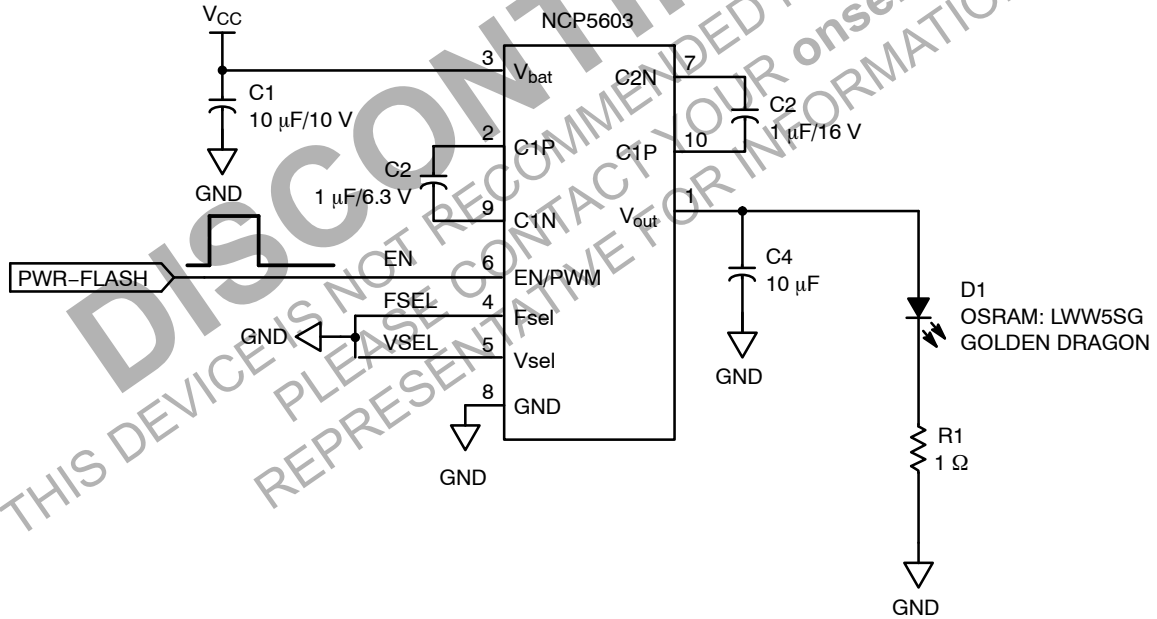


Figure 10. Typical High Power Flash Circuit

NCP5603

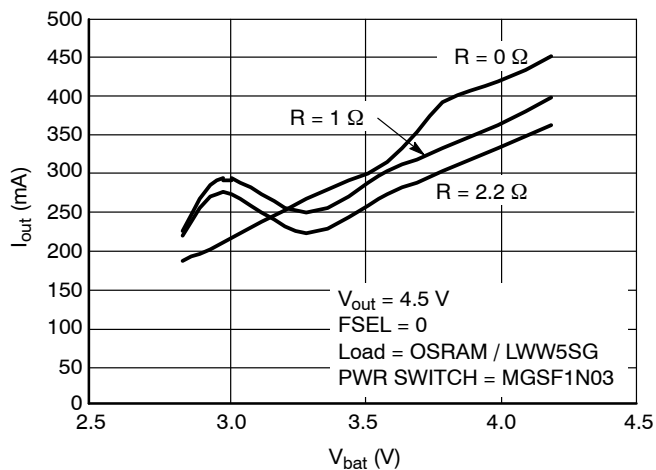


Figure 11. NCP5603 Output Current

Table 1. Ceramic Preferred Capacitors

| Manufacturer | Type/Series | Format | Value |
|--------------|-----------------|--------|--------------------|
| TDK | C3216X5R1C475MT | 1206 | 4.7 μ F / 16 V |
| TDK | C2012X5R1C225MT | 0805 | 2.2 μ F / 16 V |
| TDK | C2012X5R1C105MT | 0805 | 1.0 μ F / 16 V |

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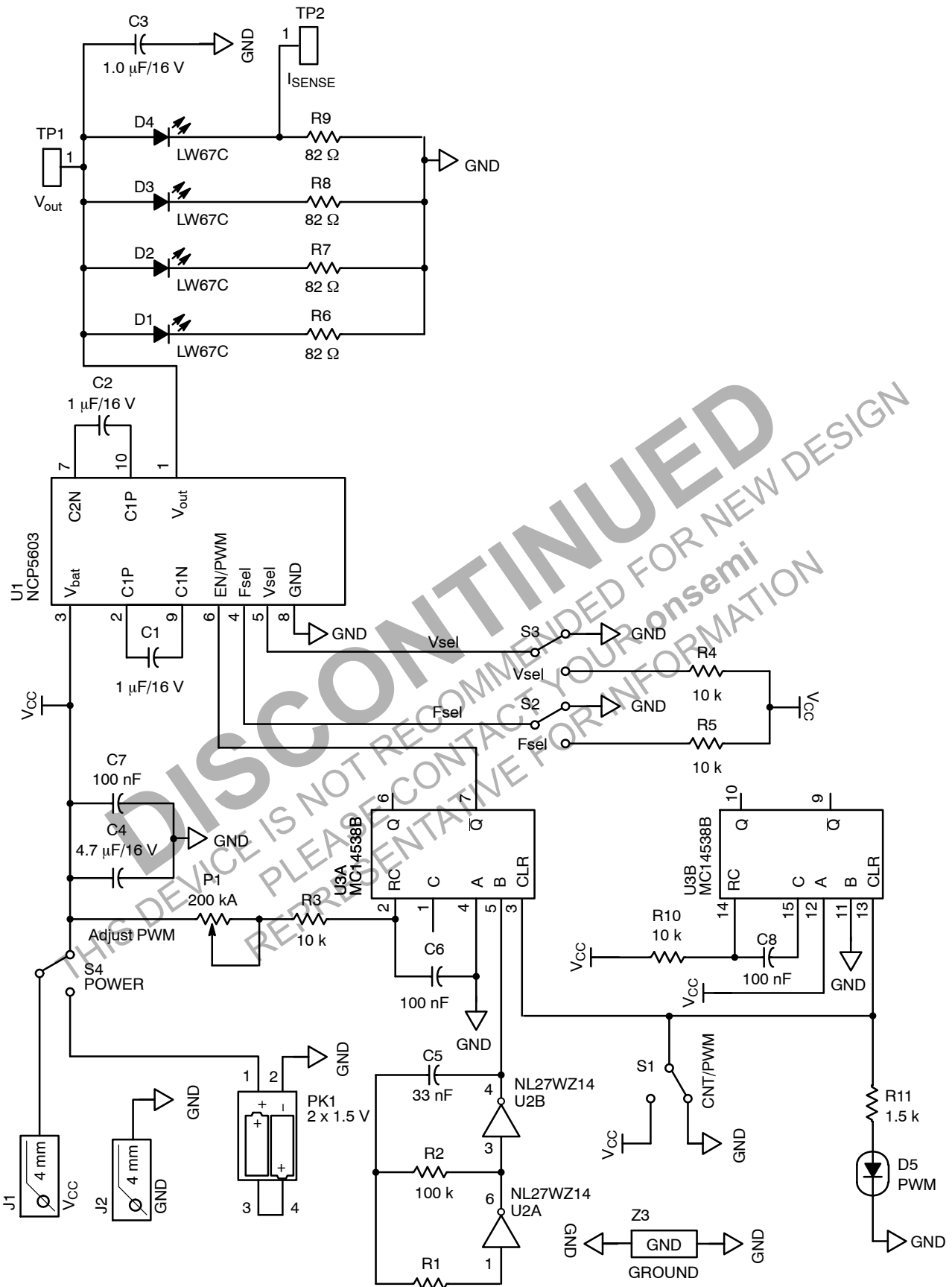


Figure 12. Evaluation Board Schematic Diagram

NCP5603

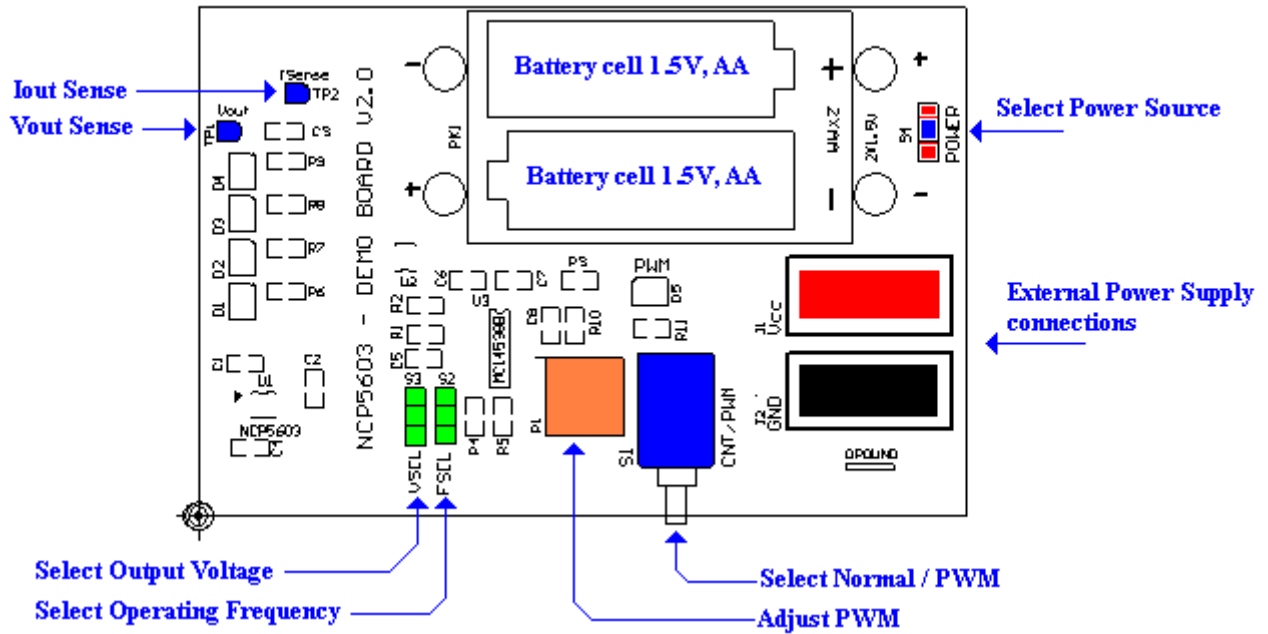


Figure 13. Evaluation Board: Silk View (Top View)

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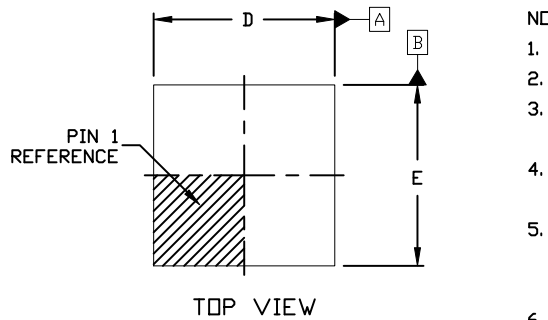
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



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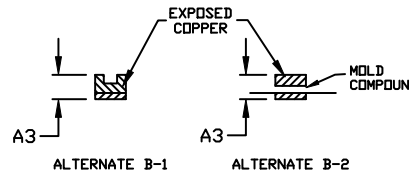
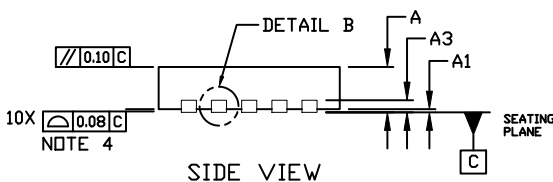
DFN10, 3x3, 0.5P CASE 485C ISSUE F

DATE 16 DEC 2021

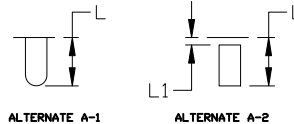
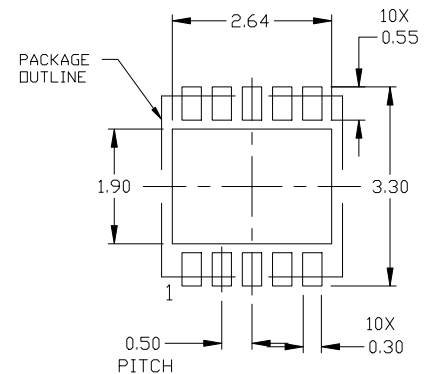
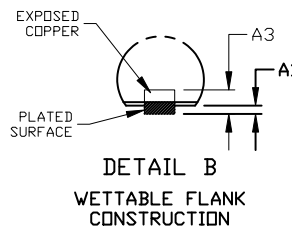
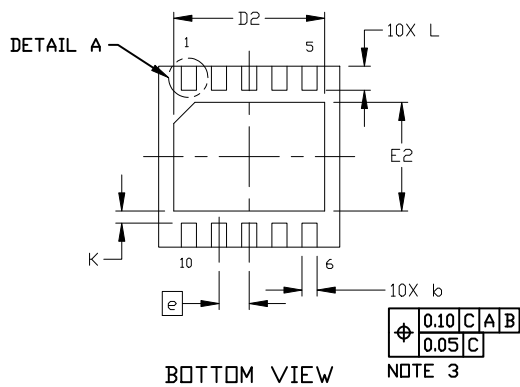


NOTES:

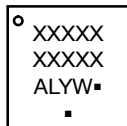
1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL *b* MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASH MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL A AND DETAIL B ALTERNATE CONSTRUCTIONS ARE NOT APPLICABLE. WETTABLE FLANK CONSTRUCTION IS DETAIL B AS SHOWN ON SIDE VIEW OF PACKAGE.



| DIM | MILLIMETERS | | |
|----------|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | --- | 0.05 |
| A3 | 0.20 REF | | |
| <i>b</i> | 0.18 | 0.23 | 0.30 |
| D | 2.90 | 3.00 | 3.10 |
| D2 | 2.40 | 2.50 | 2.60 |
| E | 2.90 | 3.00 | 3.10 |
| E2 | 1.70 | 1.80 | 1.90 |
| <i>e</i> | 0.50 BSC | | |
| K | 0.20 REF | | |
| L | 0.30 | 0.40 | 0.50 |
| L1 | --- | --- | 0.03 |



GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
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| DESCRIPTION: | DFN10, 3X3 MM, 0.5 MM PITCH | PAGE 1 OF 1 |

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