NCP4640

50 mA, Wide Input Range, Voltage Regulator

The NCP4640 is a CMOS 50 mA linear voltage regulator with high input voltage and ultra−low supply current. It incorporates multiple protection features such as peak current limit, short circuit current limit and thermal shutdown to ensure a very robust device.

A high maximum input voltage tolerance of 50 V and a wide temperature range make the NCP4640 suitable for a variety of demanding applications.

Features

- Operating Input Voltage Range: 4 V to 36 V
- Output Voltage Range: 2.0 to 12.0 V (0.1 steps)
- ±2% Output Voltage Accuracy
- Output Current: min 50 mA (V_{IN} = 8 V, V_{OUT} = 5 V)
- Line Regulation: 0.05%/V
- Peak Current Limit Circuit
- Short Current Limit Circuit
- Thermal Shutdown Circuit
- Available in SOT−89−5 and SOIC6−TL Package
- These are Pb−Free Devices

Typical Applications

- Power source for home appliances
- Power source for car audio equipment, navigation system
- Power source for notebooks, digital TVs, cordless phones and private LAN systems
- Power source for office equipment machines such as copiers, printers, facsimiles, scanners, projectors, etc.

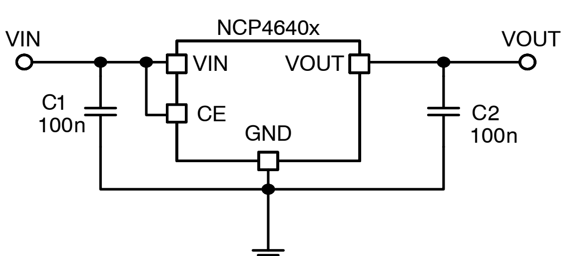

Figure 1. Typical Application Schematic

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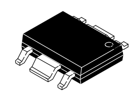
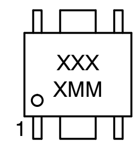
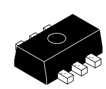
MARKING DIAGRAMS

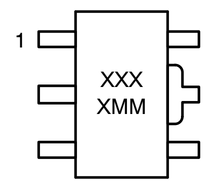


SOIC6−TL
CASE 751BR





SOT−89 5
CASE 528AB



XXXX = Specific Device Code
MM = Date Code

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

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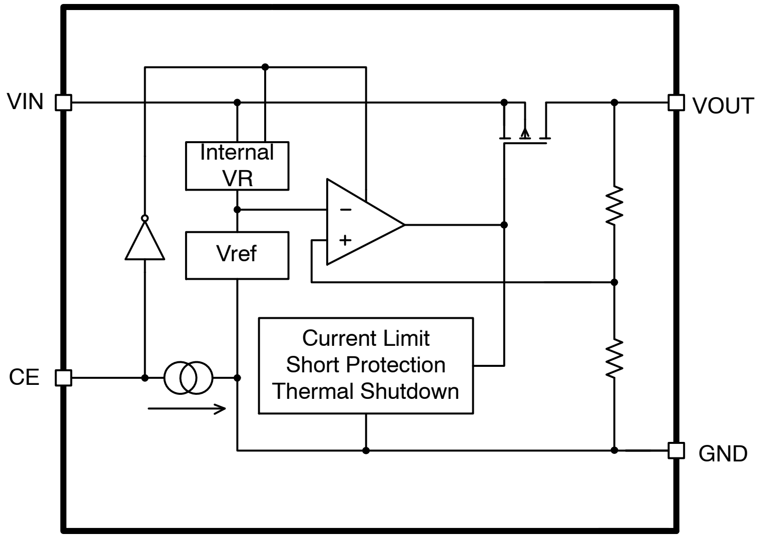


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. SOT89	Pin No. SOIC6−TL	Pin Name	Description
5	6	VIN	Input pin
2	2	GND	Ground pin, all ground pins must be connected together when it is mounted on board
4	4	GND	Ground pin, all ground pins must be connected together when it is mounted on board
−	5	GND	Ground pin, all ground pins must be connected together when it is mounted on board
3	3	CE	Chip enable pin (“H” active)
1	1	VOUT	Output pin

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{IN}	−0.3 to 50	V
Peak Input Voltage (Note 1)	V_{IN}	60	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} + 0.3 ≤ 50	V
Chip Enable Input	V_{CE}	−0.3 to V_{IN} + 0.3 ≤ 50	V
Output Current	I_{OUT}	150	mA
Power Dissipation SOT−89	P_D	900	mW
Power Dissipation SOIC6−TL		1700	
Junction Temperature	T_J	−40 to 150	°C
Storage Temperature	T_{STG}	−55 to 125	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Duration time = 200 ms
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOT−89 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	111	°C/W
Thermal Characteristics, SOIC6−TL Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	59	°C/W

ELECTRICAL CHARACTERISTICS T_A = 25°C

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	4		36	V
Output Voltage	$V_{IN} = V_{OUT} + 3$ V, $I_{OUT} = 1$ mA		V_{OUT}	x0.98		x1.02	V
Output Voltage Temp. Coefficient	$V_{IN} = V_{OUT} + 3$ V, $I_{OUT} = 1$ mA, $T_A = -40$ to 105°C				±100		ppm/°C
Line Regulation	$V_{IN} = V_{OUT} + 1.5$ V to 36 V, $I_{OUT} = 1$ mA		$Line_{Reg}$		0.05	0.20	%/V
Load Regulation	$V_{IN} = V_{OUT} + 3$ V, I_{OUT} = 1 mA to 40 mA	2.0 V ≤ V_{OUT} < 5.0 V	$Load_{Reg}$		10	25	mV
		5.0 V ≤ V_{OUT} < 12.0 V			20	35	
Dropout Voltage	$I_{OUT} = 20$ mA	2.0 V ≤ V_{OUT} < 3.7 V	V_{DO}			(Note 3)	V
		3.7 V ≤ V_{OUT} < 4.0 V			0.35	0.60	
		4.0 V ≤ V_{OUT} < 5.0 V			0.25	0.40	
		5.0 V ≤ V_{OUT} < 12.0 V			0.20	0.35	
Output Current	$V_{IN} = V_{OUT} + 3$ V		I_{OUT}	50			mA
Short Current Limit	$V_{OUT} = 0$ V		I_{SC}		50		mA
Quiescent Current	$V_{IN} = V_{OUT} + 3$ V, $I_{OUT} = 0$ mA		I_Q		9	20	µA
Standby Current	$V_{IN} = 36$ V, $V_{CE} = 0$ V		I_{STB}		0.1	1	µA
CE Pin Threshold Voltage	CE Input Voltage "H"		V_{CEH}	1.5		V_{IN}	V
	CE Input Voltage "L"		V_{CEL}	0		0.3	
Thermal Shutdown Temperature			T_{SD}		150		°C
Thermal Shutdown Release Temperature			T_{SR}		125		°C
Power Supply Rejection Ratio	$V_{IN} = 5.0$ V, $V_{OUT} = 2.0$ V, $\Delta V_{IN\ PK-PK} = 0.2$ V, $I_{OUT} = 30$ mA, f = 1 kHz		PSRR		30		dB
Output Noise Voltage	$V_{OUT} = 2.0$ V, $I_{OUT} = 30$ mA, f = 10 Hz to 100 kHz		V_N		80		μV_{rms}

3. Dropout voltage for 2.0 V ≤ V_{OUT} < 3.7 V can be computed by this formula: $V_{DO} = 4\text{ V} - V_{OUTSET}$

TYPICAL CHARACTERISTICS

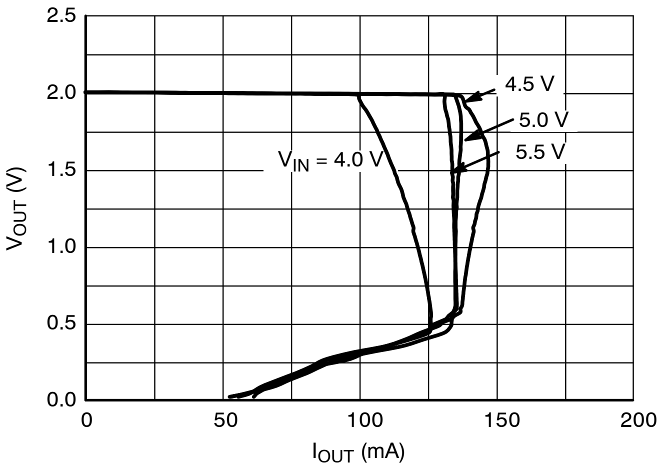


Figure 3. Output Voltage vs. Output Current 2.0 V Version (T_J = 25°C)

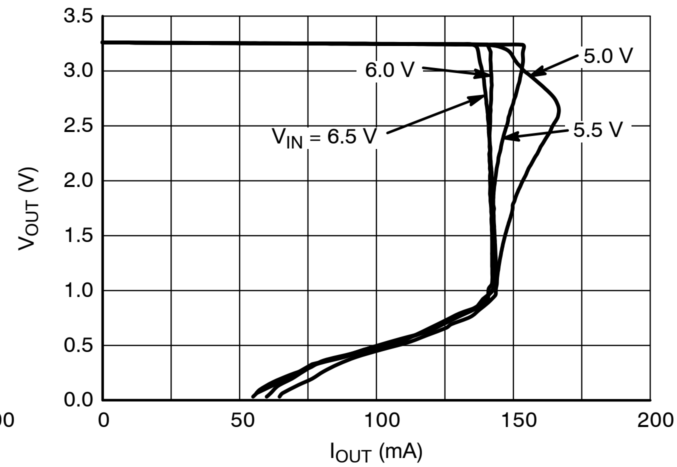


Figure 4. Output Voltage vs. Output Current 3.3 V Version (T_J = 25°C)

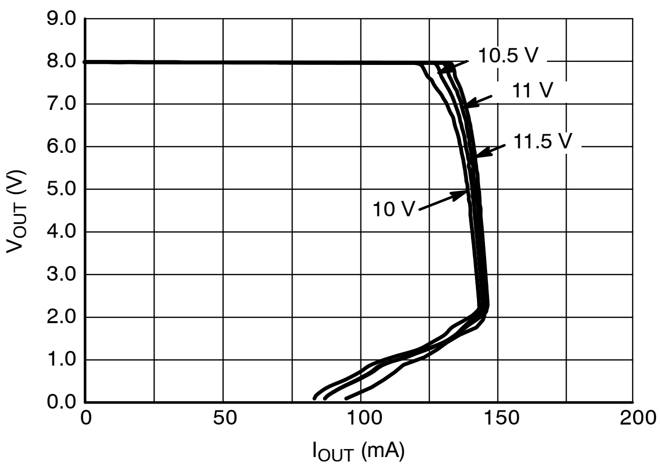


Figure 5. Output Voltage vs. Output Current 8.0 V Version (T_J = 25°C)

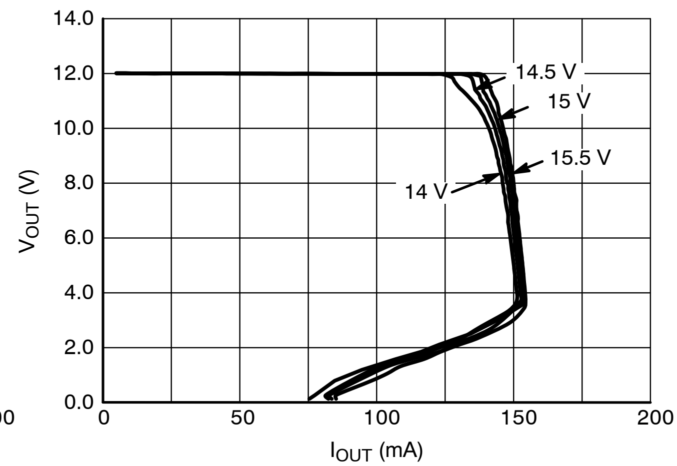


Figure 6. Output Voltage vs. Output Current 12 V Version (T_J = 25°C)

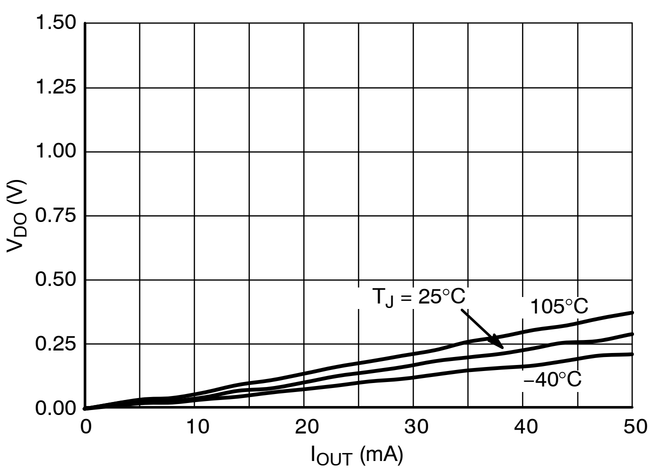


Figure 7. Dropout Voltage vs. Output Current 8.0 V Version

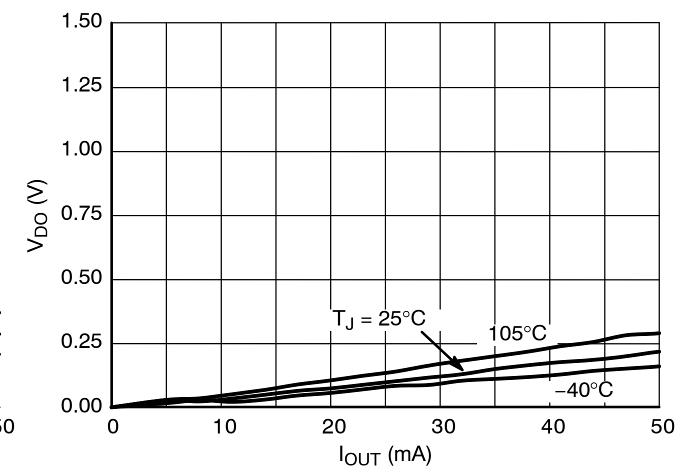


Figure 8. Dropout Voltage vs. Output Current 12 V Version

TYPICAL CHARACTERISTICS

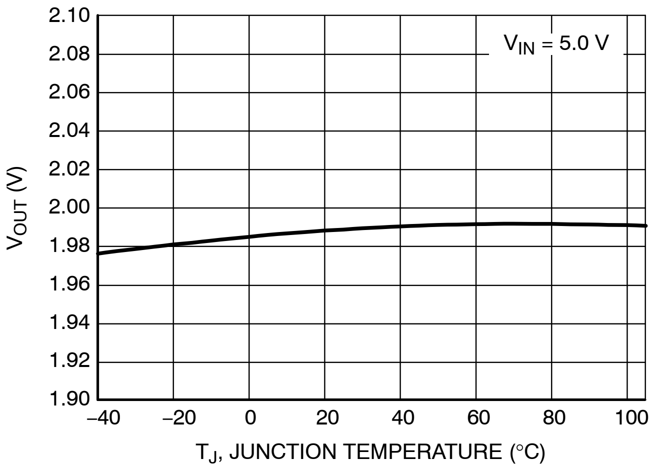


Figure 9. Output Voltage vs. Temperature, 2.0 V Version

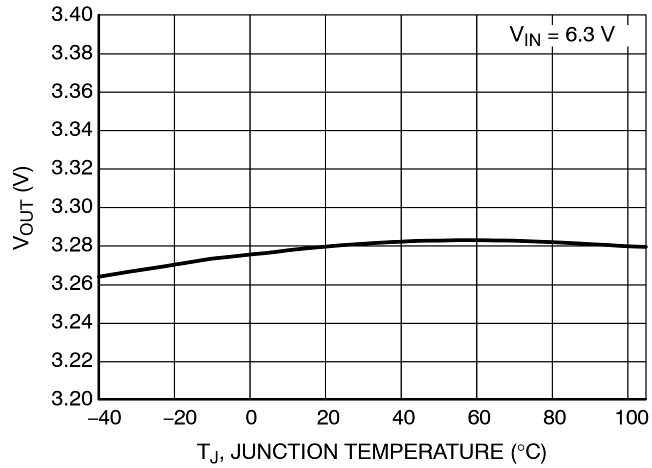


Figure 10. Output Voltage vs. Temperature, 3.3 V Version

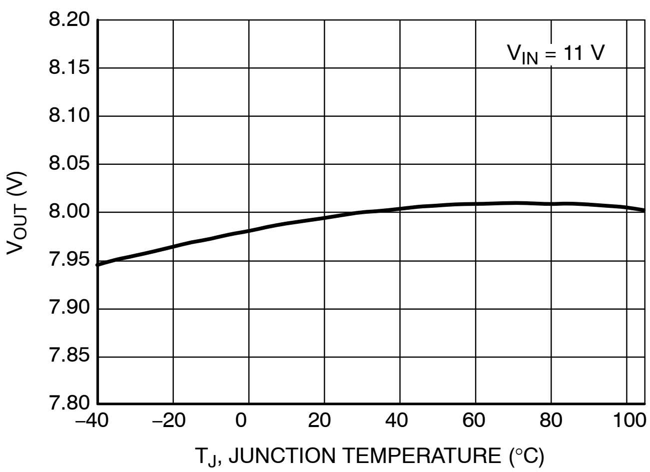


Figure 11. Output Voltage vs. Temperature, 8.0 V Version

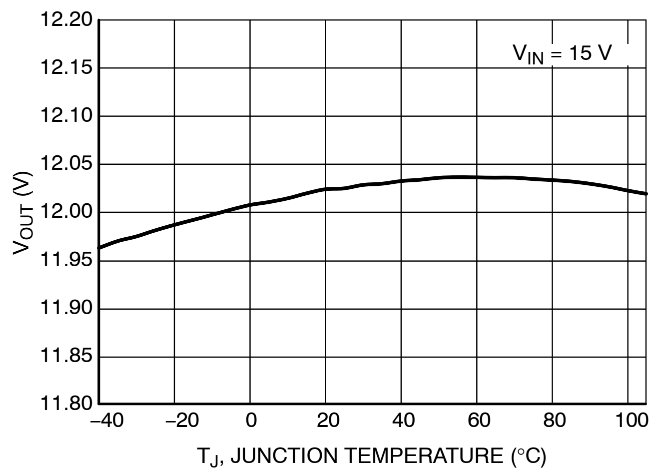


Figure 12. Output Voltage vs. Temperature, 12 V Version

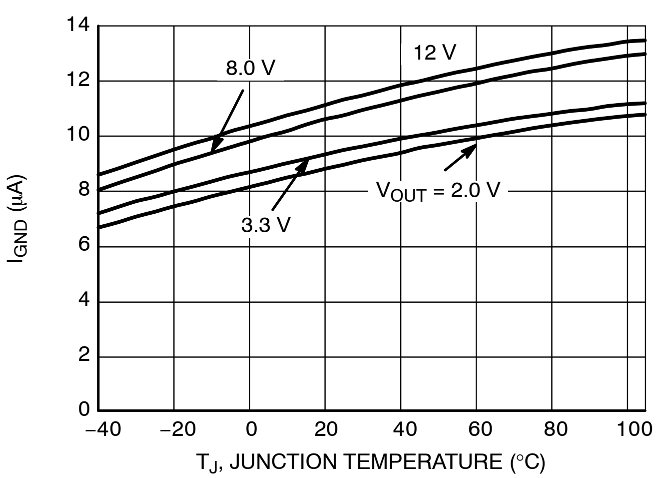


Figure 13. Supply Current vs. Temperature

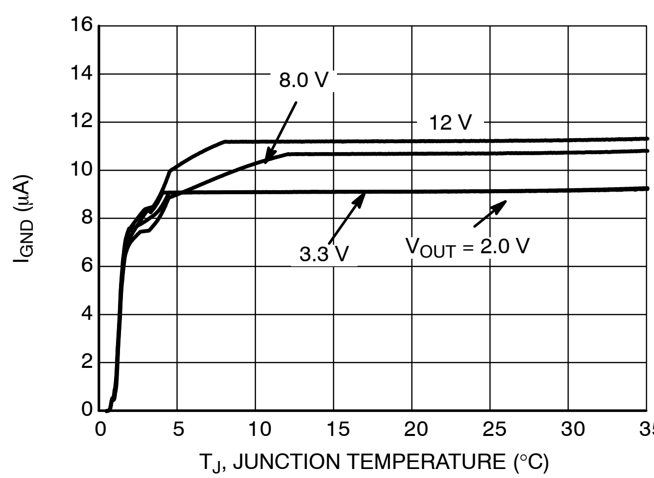


Figure 14. Supply Current vs. Input Voltage

TYPICAL CHARACTERISTICS

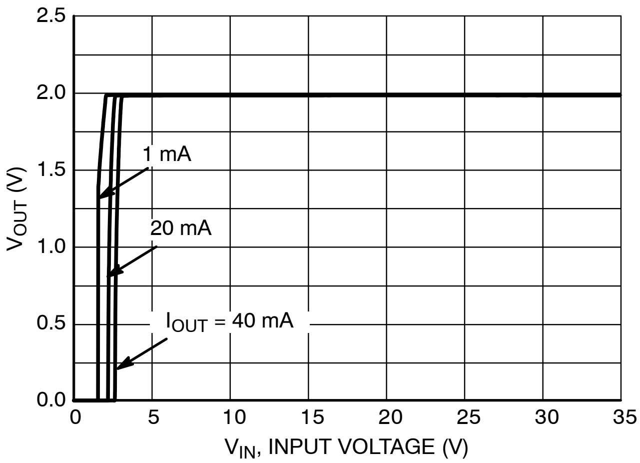


Figure 15. Output Voltage vs. Input Voltage, 2.0 V Version

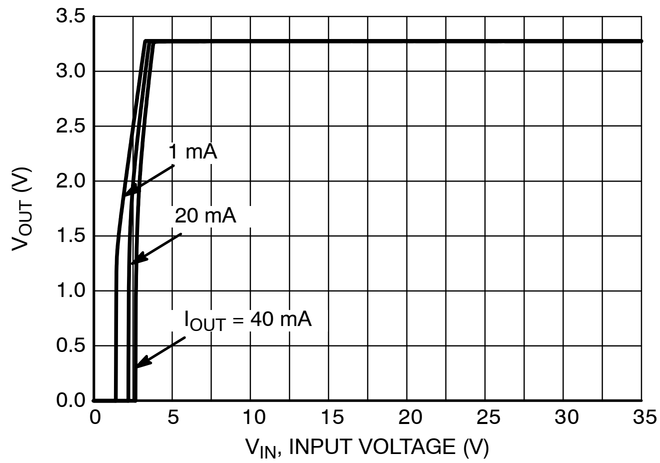


Figure 16. Output Voltage vs. Input Voltage, 3.3 V Version

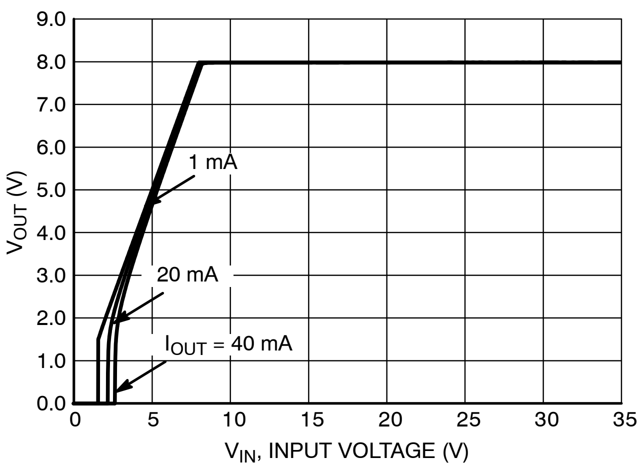


Figure 17. Output Voltage vs. Input Voltage, 8.0 V Version

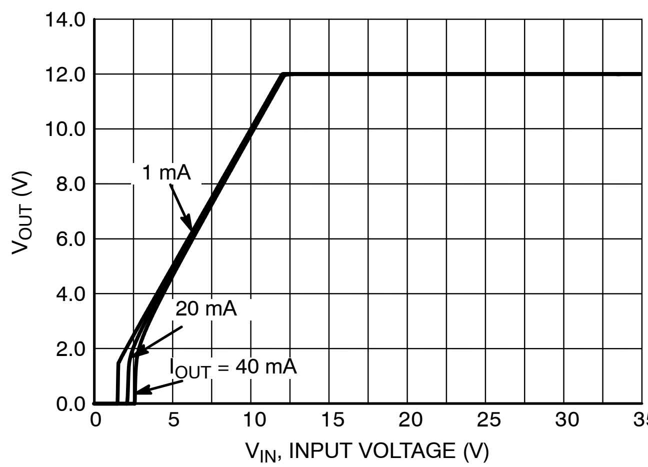


Figure 18. Output Voltage vs. Input Voltage, 12 V Version

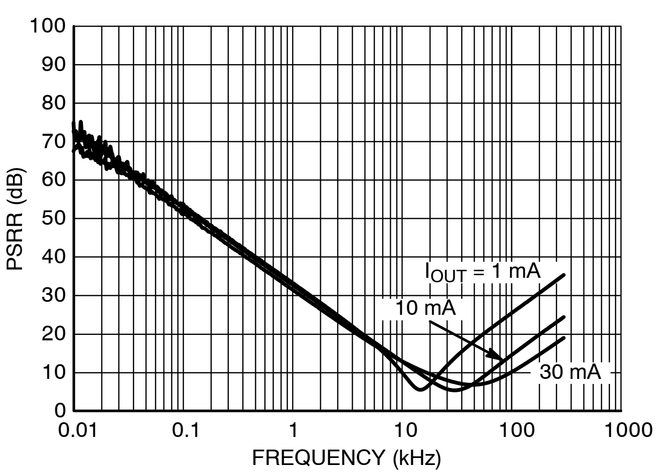


Figure 19. PSRR, 2.0 V Version, V_{IN} = 5.0 V

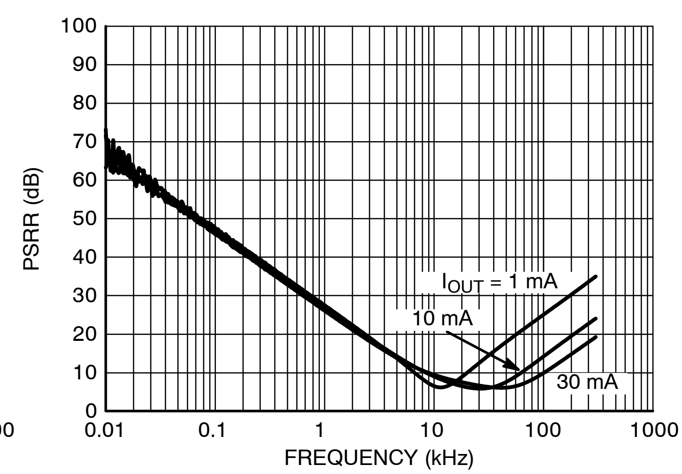


Figure 20. PSRR, 3.3 V Version, V_{IN} = 6.3 V

TYPICAL CHARACTERISTICS

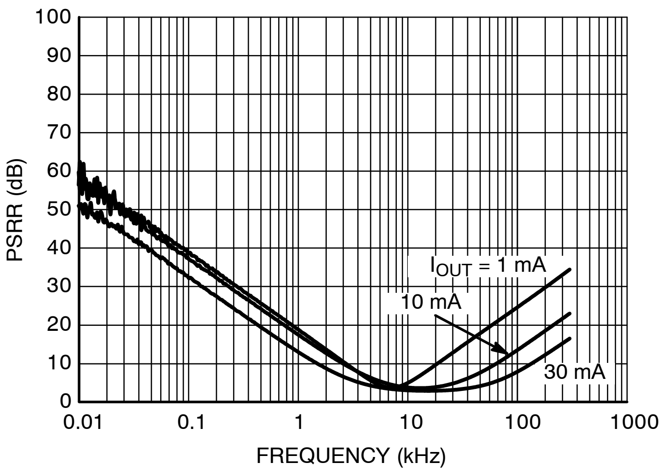


Figure 21. PSRR, 3.3 V Version, V_{IN} = 6.3 V

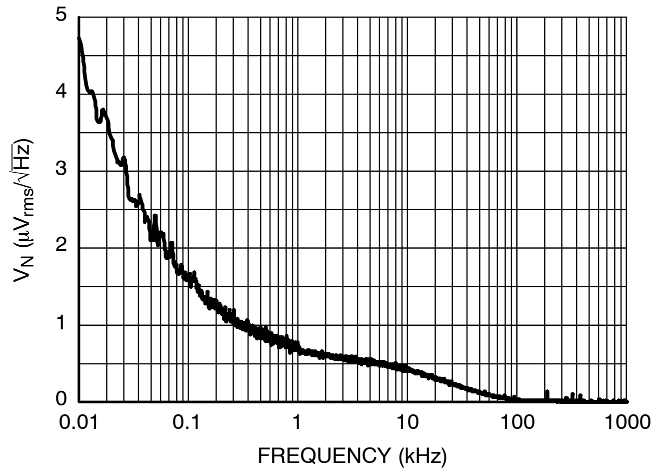


Figure 22. Output Voltage Noise, 2.0 V Version, V_{IN} = 5.0 V, I_{OUT} = 30 mA

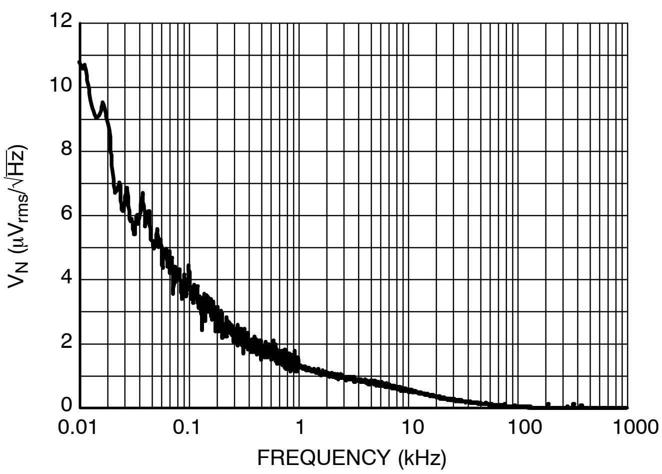


Figure 23. Output Voltage Noise, 3.3 V Version, V_{IN} = 6.3 V, I_{OUT} = 30 mA

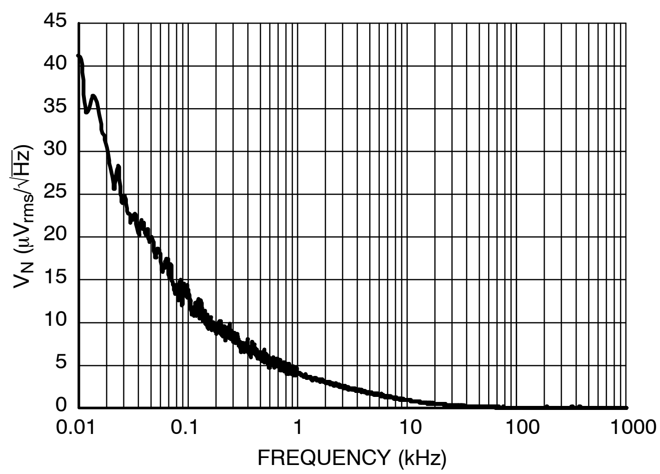


Figure 24. Output Voltage Noise, 8.0 V Version, V_{IN} = 11.0 V, I_{OUT} = 30 mA

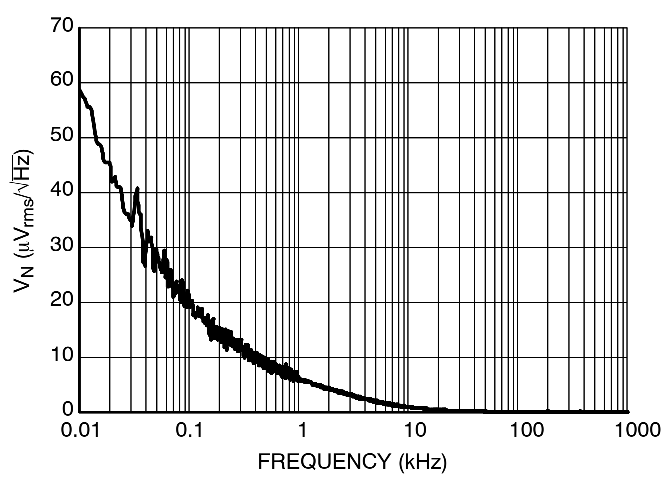


Figure 25. Output Voltage Noise, 12.0 V Version, V_{IN} = 15.0 V, I_{OUT} = 30 mA

TYPICAL CHARACTERISTICS

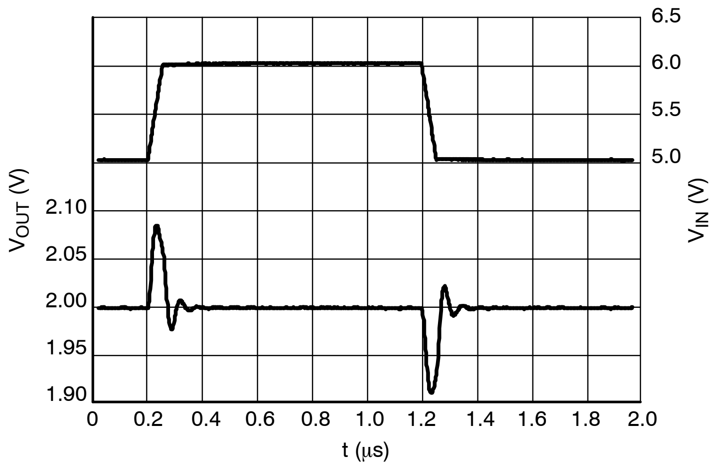


Figure 26. Line Transients, 2.0 V Version, $t_R = t_F = 50\ \mu s$, $I_{OUT} = 1\ mA$

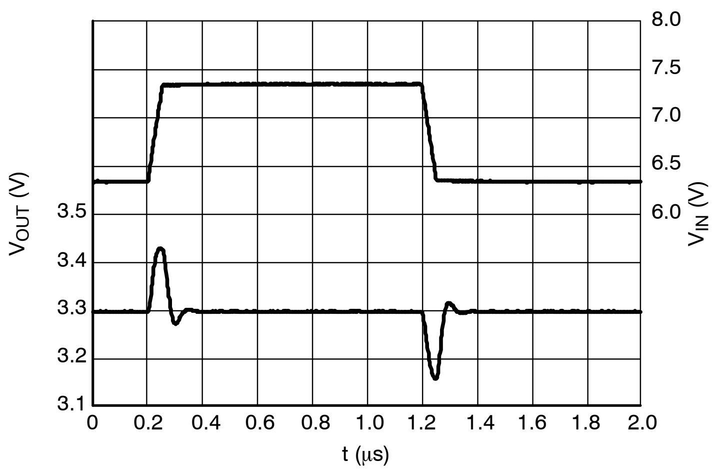


Figure 27. Line Transients, 3.3 V Version, $t_R = t_F = 50\ \mu s$, $I_{OUT} = 1\ mA$

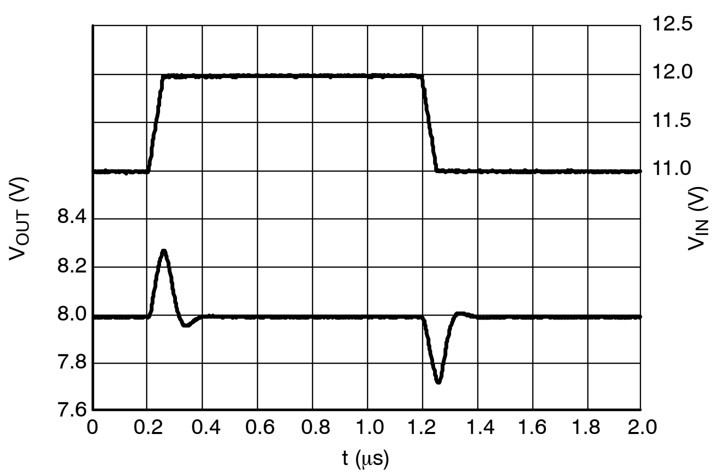


Figure 28. Line Transients, 8.0 V Version, $t_R = t_F = 50\ \mu s$, $I_{OUT} = 1\ mA$

TYPICAL CHARACTERISTICS

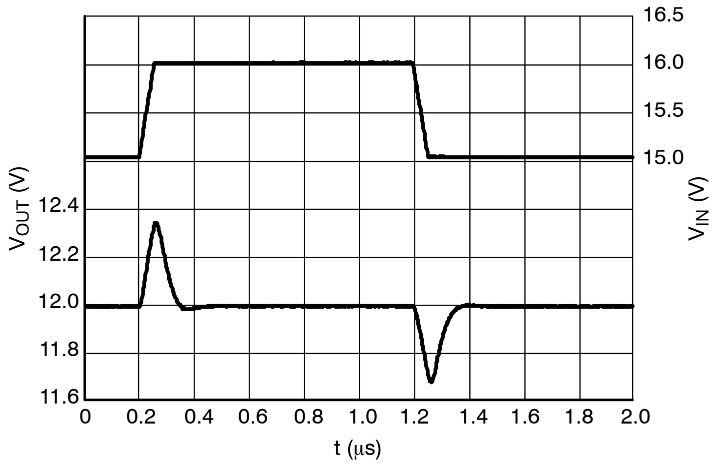


Figure 29. Line Transients, 12.0 V Version, $t_R = t_F = 50\ \mu s$, $I_{OUT} = 1$ mA

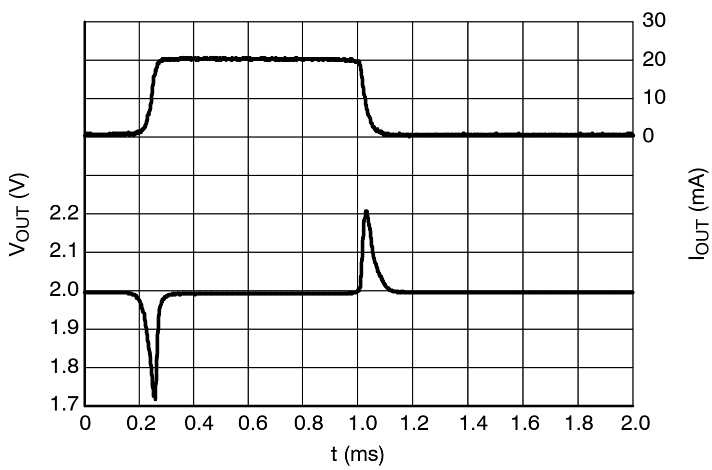


Figure 30. Load Transients, 2.0 V Version, $I_{OUT} = 1 – 20$ mA, $t_R = t_F = 50\ \mu s$, $V_{IN} = 5.0$ V

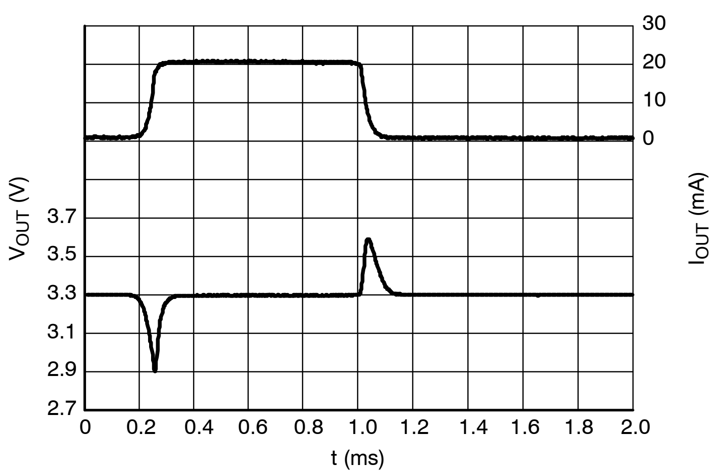


Figure 31. Load Transients, 3.3 V Version, $I_{OUT} = 1 – 20$ mA, $t_R = t_F = 50\ \mu s$, $V_{IN} = 6.3$ V

TYPICAL CHARACTERISTICS

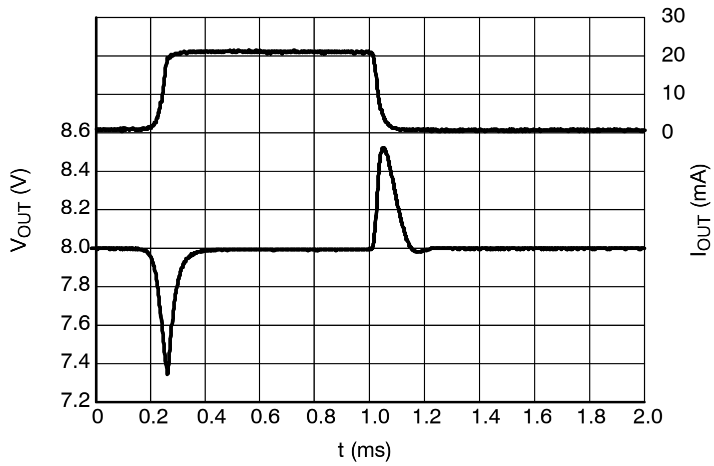


Figure 32. Load Transients, 8.0 V Version, I_{OUT} = 1 – 20 mA, $t_R = t_F$ = 50 μs, V_{IN} = 11.0 V

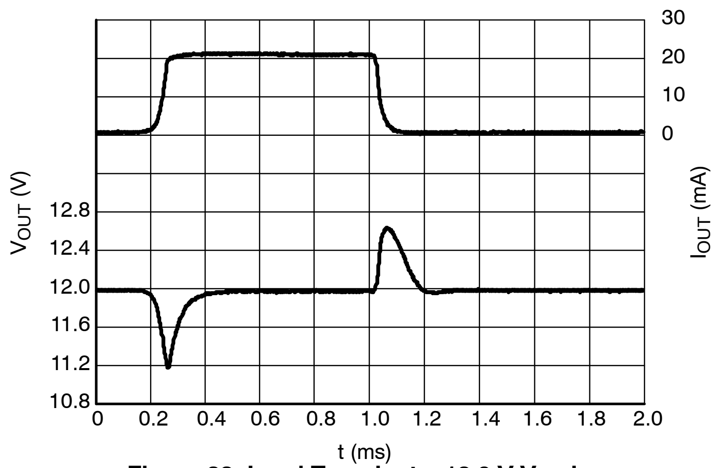


Figure 33. Load Transients, 12.0 V Version, I_{OUT} = 1 – 20 mA, $t_R = t_F$ = 50 μs, V_{IN} = 15.0 V

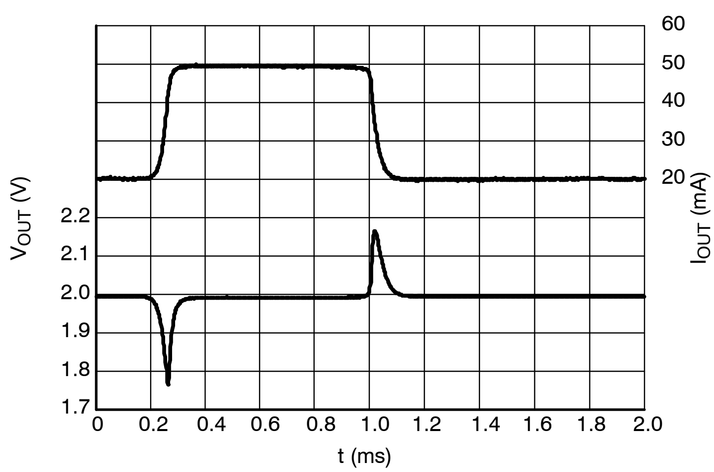


Figure 34. Load Transients, 2.0 V Version, I_{OUT} = 20 – 50 mA, $t_R = t_F$ = 50 μs, V_{IN} = 5.0 V

TYPICAL CHARACTERISTICS

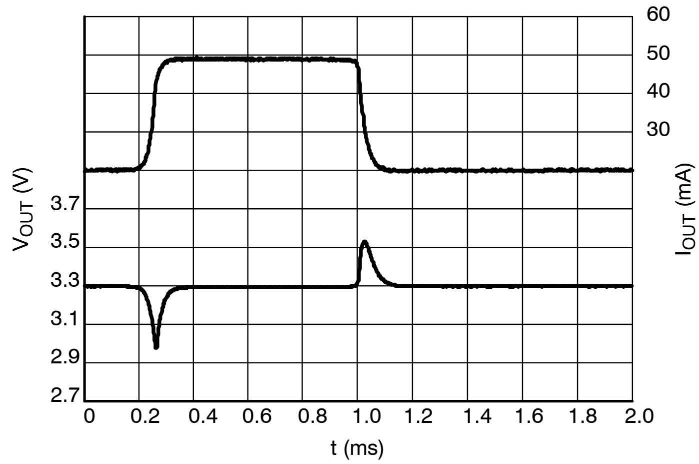


Figure 35. Load Transients, 3.3 V Version, I_{OUT} = 20 – 50 mA, t_R = t_F = 50 μs, V_{IN} = 6.3 V

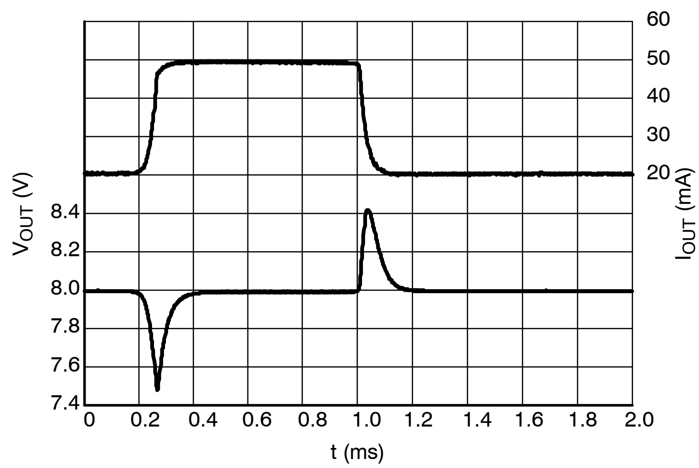


Figure 36. Load Transients, 8.0 V Version, I_{OUT} = 20 – 50 mA, t_R = t_F = 50 μs, V_{IN} = 11.0 V

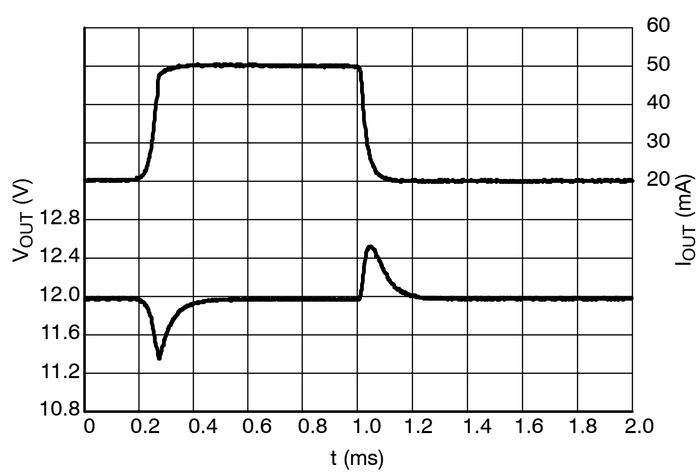


Figure 37. Load Transients, 12.0 V Version, I_{OUT} = 20 – 50 mA, t_R = t_F = 50 μs, V_{IN} = 15.0 V

TYPICAL CHARACTERISTICS

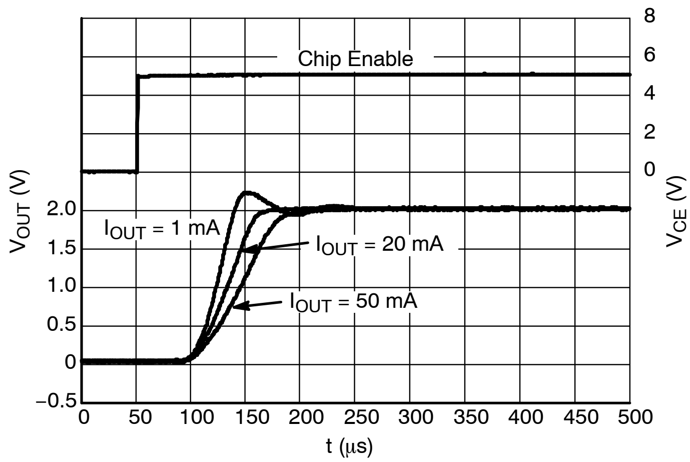


Figure 38. Start−up, 2.0 V Version, V_{IN} = 5.0 V

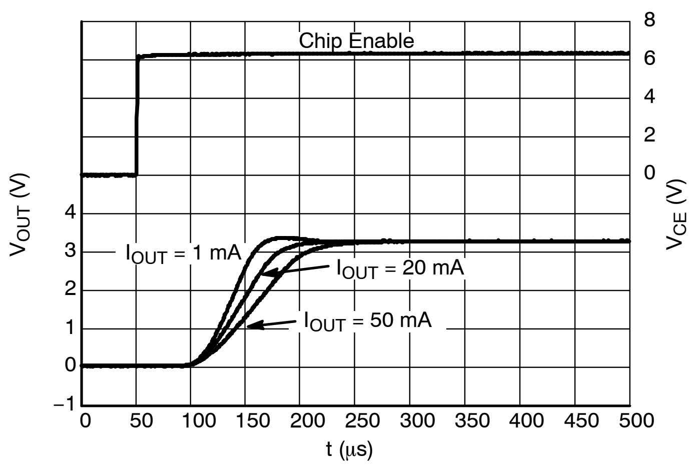


Figure 39. Start−up, 3.3 V Version, V_{IN} = 6.3 V

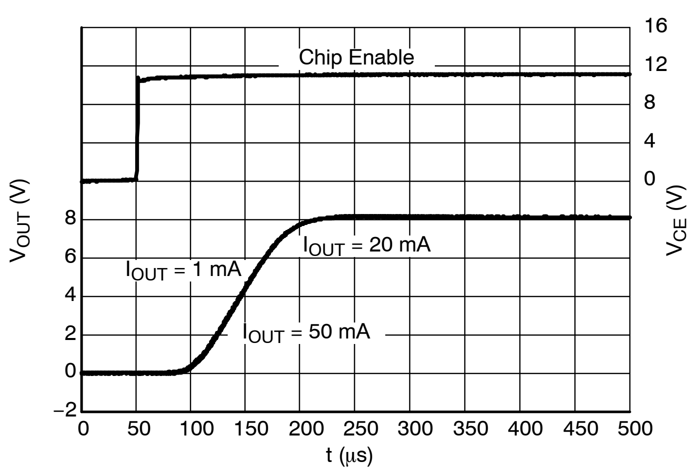


Figure 40. Start−up, 8.0 V Version, V_{IN} = 11.0 V

TYPICAL CHARACTERISTICS

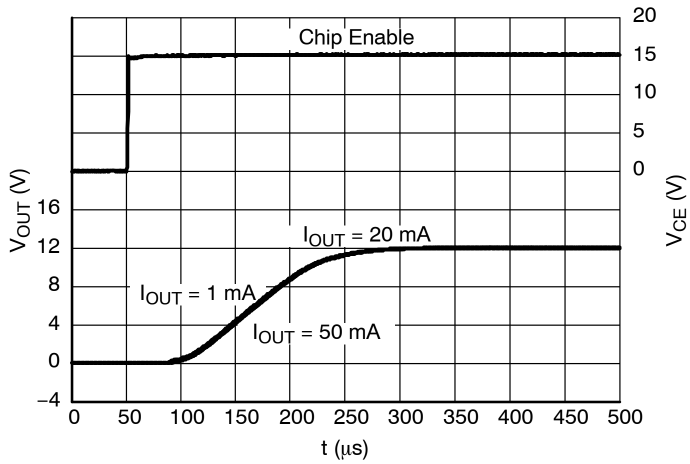


Figure 41. Start−up, 12.0 V Version, V_{IN} = 15.0 V

APPLICATION INFORMATION

A typical application circuit for NCP4640 series is shown in Figure 42.

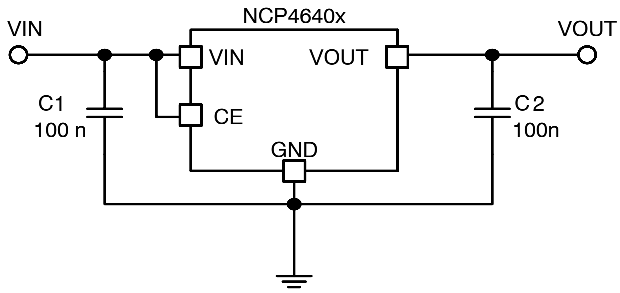


Figure 42. Typical Application Schematic

Input Decoupling Capacitor (C1)

The device is stable without any input capacitance, but if input line is long and has high impedance or if more stable operation is needed, input capacitor C1 should be connected as close as possible to the IC. Recommended range of input capacitor value is 100 nF to 10 μF.

Output Decoupling Capacitor (C2)

The NCP4641 can work stable without output capacitor, but if faster response and higher stability reserve is needed, output capacitor should be connected as close as possible to the device. Recommended range of output capacitance is 100 nF to 10 μF. Larger values of output capacitance and lower ESR improves dynamic parameters.

Enable Operation

The enable pin CE may be used for turning the regulator on and off. The device is activated when high level is connected to CE pin. Do not keep CE pin not connected or between VCEH and VCEL voltage levels. Otherwise output voltage would be unstable or indefinite and unexpected would flow internally.

Thermal

As a power across the IC increase, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and also the ambient temperature affect the rate of temperature increase for the part. When the device has good thermal conductivity through the PCB the junction temperature will be relatively low in high power dissipation applications.

The IC includes internal thermal shutdown circuit that stops operation of regulator, if junction temperature is higher than 150°C. After that, when junction temperature decreases below 125°C, the operation of voltage regulator would restart. While high power dissipation condition is, the regulator starts and stops repeatedly and protects itself against overheating.

PCB layout

Pins number 2 and 4 of SOT89−5 package and pins number 2, 4 and 5 of SOIC6−TL must be wired to the GND plane while it is mounted on board. Make VIN and GND lines sufficient. If their impedance is high, noise pickup or unstable operation may result. Connect capacitors C1 and C2 as close as possible to the IC, and make wiring as short as possible.

ORDERING INFORMATION

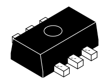
Device	Nominal Output Voltage	Description	Marking	Package	Shipping†
NCP4640H020T1G	2.0 V	Enable High	N020	SOT89−5 (Pb−Free)	1000 / Tape & Reel
NCP4640H030T1G	3.0 V	Enable High	N030	SOT89−5 (Pb−Free)	1000 / Tape & Reel
NCP4640H033T1G	3.3 V	Enable High	N033	SOT89−5 (Pb−Free)	1000 / Tape & Reel
NCP4640H080T1G	8.0 V	Enable High	N080	SOT89−5 (Pb−Free)	1000 / Tape & Reel
NCP4640H120T1G	12.0 V	Enable High	N120	SOT89−5 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*To order other package and voltage variants, please contact your ON Semiconductor sales representative.

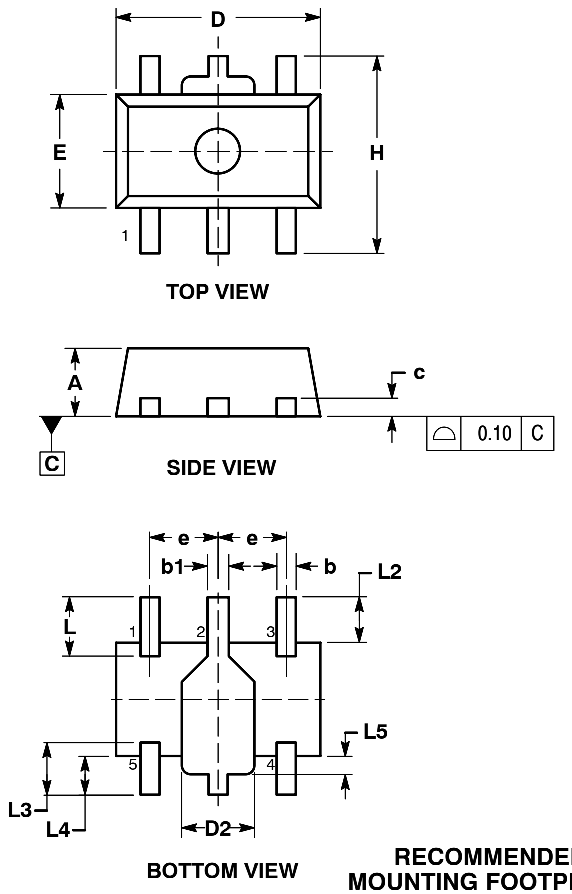
ON Semiconductor®

SOT−89, 5 LEAD
CASE 528AB−01
ISSUE O

DATE 23 NOV 2009



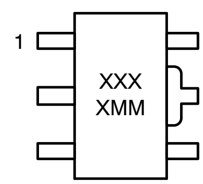
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. LEAD THICKNESS INCLUDES LEAD FINISH.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. DIMENSIONS L, L2, L3, L4, L5, AND H ARE MEASURED AT DATUM PLANE C.

	MILLIMETERS	
DIM	MIN	MAX
A	1.40	1.60
b	0.32	0.52
b1	0.37	0.57
c	0.30	0.50
D	4.40	4.60
D2	1.40	1.80
E	2.40	2.60
e	1.40	1.60
H	4.25	4.45
L	1.10	1.50
L2	0.80	1.20
L3	0.95	1.35
L4	0.65	1.05
L5	0.20	0.60

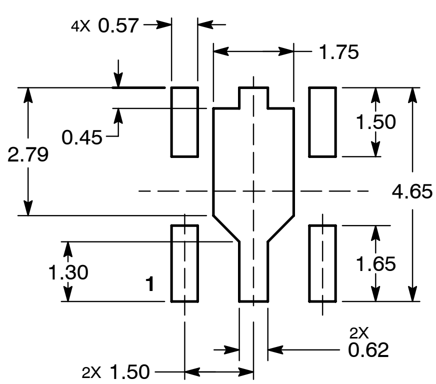
GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
MM = Lot Number
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	SOT−89, 5 LEAD	PAGE 1 OF 1

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