NCP1631

Interleaved, 2-Phase Power Factor Controller

The NCP1631 integrates a dual MOSFET driver for interleaved PFC applications. Interleaving consists of paralleling two small stages in lieu of a bigger one, more difficult to design. This approach has several merits like the ease of implementation, the use of smaller components or a better distribution of the heating.

Also, Interleaving extends the power range of Critical Conduction Mode that is an efficient and cost−effective technique (no need for low t_{rr} diodes). In addition, the NCP1631 drivers are 180° phase shift for a significantly reduced current ripple.

Housed in a SOIC16 package, the circuit incorporates all the features necessary for building robust and compact interleaved PFC stages, with a minimum of external components.

General Features

- Near−Unity Power Factor
- Substantial 180° Phase Shift in All Conditions Including Transient Phases
- Frequency Clamped Critical Conduction Mode (**FCCrM**) i.e., Fixed Frequency, Discontinuous Conduction Mode Operation with Critical Conduction Achievable in Most Stressful Conditions
- FCCrM Operation Optimizes the PFC Stage Efficiency Over the Load Range
- Out−of−phase Control for Low EMI and a Reduced rms Current in the Bulk Capacitor
- Frequency Fold−back at Low Power to Further Improve the Light Load Efficiency
- Accurate Zero Current Detection by Auxiliary Winding for Valley Turn On
- Fast Line / Load Transient Compensation
- High Drive Capability: −500 mA / +800 mA
- Signal to Indicate that the PFC is Ready for Operation (“pfcOK” Pin)
- V_{CC} Range: from 10 V to 20 V

Safety Features

- Output Over and Under Voltage Protection
- Brown−Out Detection with a 50−ms Delay to Help Meet Hold−up Time Specifications
- Soft−Start for Smooth Start−up Operation
- Programmable Adjustment of the Maximum Power
- Over Current Limitation
- Detection of Inrush Currents

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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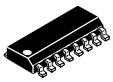
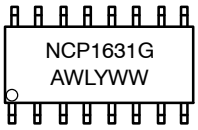


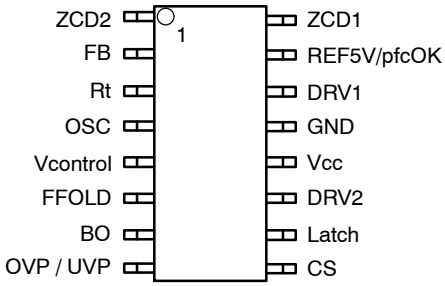
SOIC−16
D SUFFIX
CASE 751B

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

PIN ASSIGNMENT



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1631DR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Typical Applications

- Computer Power Supplies
- LCD / Plasma Flat Panels
- All Off Line Appliances Requiring Power Factor Correction

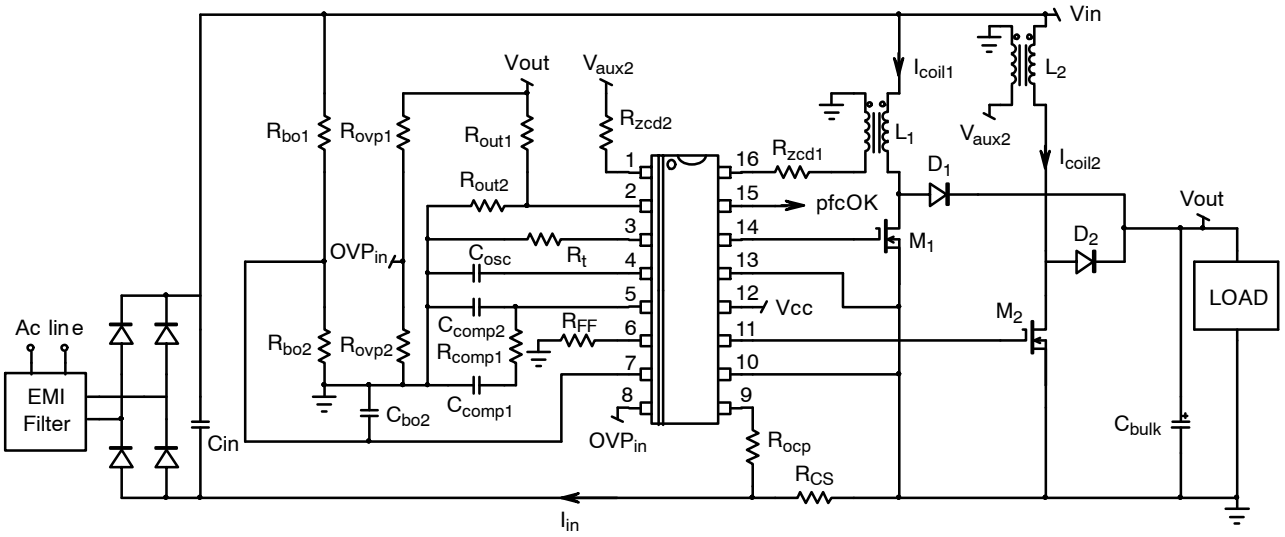


Figure 1. Typical Application Schematic

Table 1. MAXIMUM RATINGS

Symbol	Rating	Pin	Value	Unit
$V_{CC(MAX)}$	Maximum Power Supply Voltage Continuous	12	−0.3, +20	V
DRV_{MAX}	Maximum Voltage on DRV Pins	11, 14	−0.3 V, V_{CC}	V
V_{MAX}	Maximum Input Voltage on Low Power Pins	1, 2, 3, 4, 6, 7, 8, 9, 10, 15, and 16	−0.3, +9.0	V
$V_{Control(MAX)}$	$V_{Control}$ Pin Maximum Input Voltage	5	−0.3, $V_{Control(clamp)}$ (Note 1)	V
	Power Dissipation and Thermal Characteristics			
P_D	Maximum Power Dissipation @ T_A = 70°C		550	mW
$R_{\theta J-A}$	Thermal Resistance Junction−to−Air		145	°C/W
T_J	Operating Junction Temperature Range		−55 to +150	°C
$T_{J(MAX)}$	Maximum Junction Temperature		150	°C
$T_{S(MAX)}$	Storage Temperature Range		−65 to +150	°C
$T_{L(MAX)}$	Lead Temperature (Soldering, 10s)		300	°C
	ESD Capability, HBM model (Note 2)		3	kV
	ESD Capability, Machine Model (Note 2)		250	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. "$V_{Control(clamp)}$" is the pin5 clamp voltage.
2. This device(s) contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per JEDEC Standard JESD22−A114E
   Machine Model Method 200 V per JEDEC Standard JESD22−A115−A
3. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.

Table 2. TYPICAL ELECTRICAL CHARACTERISTICS TABLE (Conditions: V_{CC} = 15 V, V_{pin7} = 2 V, V_{pin10} = 0 V; for typical values T_J = 25°C, for min/max values T_J = −55°C to +125°C, unless otherwise specified) (Note 6)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
STARTUP AND SUPPLY CIRCUITS						
Supply Voltage						V
Startup Threshold	V_{CC} increasing	$V_{CC(on)}$	11	11.85	12.7	
Minimum Operating Voltage	V_{CC} decreasing	$V_{CC(off)}$	9.5	10	10.5	
Hysteresis $V_{CC(on)} - V_{CC(off)}$		$V_{CC(hyst)}$	1.5	1.85	–	
Internal Logic Reset	V_{CC} decreasing	$V_{CC(reset)}$	4.0	5.75	7.5	
Startup current	V_{CC} = 9.4 V	$I_{CC(start)}$	–	35	100	μA
Supply Current						mA
Device Enabled/No output load on pin6	F_{sw} = 130 kHz (Note 4)	I_{CC1}	–	5.0	7.0	
Current that discharges V_{CC} in latch mode	V_{CC} = 15 V, V_{pin10} = 5 V	$I_{CC(latch)}$	–	0.4	0.8	
Current that discharges V_{CC} in OFF mode	V_{CC} = 15 V, pin 7 grounded	$I_{CC(off)}$	–	0.4	0.8	
OSCILLATOR AND FREQUENCY FOLDBACK						
Clamping Charging Current	Pin 6 open	$I_{OSC(clamp)}$				μA
	T_J = −40°C to +125°C		31.5	35	38.5	
	T_J = −55°C to +125°C (Note 6)		30	35	38.5	
Charge Current with no frequency foldback	Pin 6 grounded	$I_{OSC(CH1)}$				μA
	T_J = −40°C to +125°C		126	140	154	
	T_J = −55°C to +125°C (Note 6)		120	140	154	
Charge Current @ I_{pin6} = 50 μA	I_{pin6} = 50 μA	$I_{OSC(CH2)}$	76.5	85	93.5	μA
Maximum Discharge Current with no frequency foldback	Pin 6 grounded	$I_{OSC(DISCH1)}$				μA
	T_J = −40°C to +125°C		94.5	105	115.5	
	T_J = −55°C to +125°C (Note 6)		90	105	115.5	
Discharge Current @ I_{pin6} = 50 μA	I_{pin6} = 50 μA	$I_{OSC(DISCH2)}$	45	50	55	μA
Voltage on pin 6	I_{pin6} = 50 μA, V_{pin5} = 2.5 V	V_{FF}	0.9	1.0	1.3	V
Oscillator Upper Threshold		$V_{OSC(high)}$	–	5	–	V
Oscillator Lower Threshold		$V_{OSC(low)}$	3.6	4.0	4.4	V
Oscillator Swing (Note 5)		$V_{OSC(swing)}$	0.93	0.98	1.03	V
CURRENT SENSE						
Current Sense Voltage Offset	I_{pin9} = 100 μA	$V_{CS(TH100)}$	−20	0	20	mV
	I_{pin9} = 10 μA	$V_{CS(TH10)}$	−10	0	10	
Current Sense Protection Threshold	T_J = 25°C	I_{ILIM1}	202	210	226	μA
	T_J = −40°C to 125°C		194	210	226	
	T_J = −55°C to +125°C (Note 6)		173	210	226	
Threshold for In−rush Current Detection (Note 5)	T_J = −40°C to +125°C	$I_{in-rush}$	11	14	17	μA
	T_J = −55°C to +125°C		10.4	14	17	
GATE DRIVE (Note 7)						
Drive Resistance						Ω
DRV1 Sink	I_{pin14} = 100 mA	R_{SNK1}	–	7	15	
DRV1 Source	I_{pin14} = −100 mA	R_{SRC1}	–	15	25	
DRV2 Sink	I_{pin11} = 100 mA	R_{SNK2}	–	7	15	
DRV2 Source	I_{pin11} = −100 mA	R_{SRC2}	–	15	25	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. DRV1 and DRV2 pulsating at half this frequency, that is, 65 kHz.
5. Not tested. Guaranteed by design and characterization.
6. For coldest temperature, QA sampling at −40°C in production and −55°C specification is Guaranteed by Characterization.
7. Guaranteed by design, the VCC pin can handle the double of the DRV peak source current, that is, 1 A typically.

Table 2. TYPICAL ELECTRICAL CHARACTERISTICS TABLE (Conditions: V_{CC} = 15 V, V_{pin7} = 2 V, V_{pin10} = 0 V; for typical values T_J = 25°C, for min/max values T_J = −55°C to +125°C, unless otherwise specified) (Note 6)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
GATE DRIVE (Note 7)						
Drive Current Capability (Note 5)						mA
DRV1 Sink	V_{DRV1} = 10 V	I_{SNK1}	–	800	–	
DRV1 Source	V_{DRV1} = 0 V	I_{SRC1}	–	500	–	
DRV2 Sink	V_{DRV2} = 10 V	I_{SNK1}	–	800	–	
DRV2 Source	V_{DRV2} = 0 V	I_{SRC1}	–	500	–	
Rise Time						ns
DRV1	C_{DRV1} = 1 nF, V_{DRV1} = 1 to 10 V	t_{r1}	–	40	–	
DRV2	C_{DRV2} = 1 nF, V_{DRV2} = 1 to 10 V	t_{r2}	–	40	–	
Fall Time						ns
DRV1	C_{DRV1} = 1 nF, V_{DRV1} = 10 to 1 V	t_{f1}	–	20	–	
DRV2	C_{DRV2} = 1 nF, V_{DRV2} = 10 to 1 V	t_{f2}	–	20	–	
REGULATION BLOCK						
Feedback Voltage Reference		V_{REF}	2.44	2.500	2.56	V
Error Amplifier Source Current Capability	@ V_{pin2} = 2.4 V	$I_{EA(SRC)}$		−20		μA
Error Amplifier Sink Current Capability	@ V_{pin2} = 2.6 V	$I_{EA(SNK)}$		+20		
Error Amplifier Gain		G_{EA}	110	200	290	μS
Pin 5 Source Current when ($V_{out(low)}$ Detect) is activated	T_J = −40°C to 125°C T_J = −55°C to +125°C (Note 6)	$I_{Control(boost)}$	184 178	230 230	276 276	μA μA
Pin2 Bias Current	V_{pin2} = 2.5 V	$I_{FB(bias)}$	−500		500	nA
Pin 5 Voltage:	@ V_{pin2} = 2.4 V @ V_{pin2} = 2.6 V	$V_{Control(clamp)}$ $V_{Control(MIN)}$ $V_{Control(range)}$	3.0 0 2.7	3.6 0.6 3	4.2 1.2 3.3	V
Internal V_{REGUL} Voltage (measured on pin 6):	@ V_{pin2} = 2.6 V, I_{pin6} = 90 μA @ V_{pin2} = 2.4 V, I_{pin6} = 90 μA	$V_{REGUL(MIN)}$ $V_{REGUL(Clamp)}$	– –	– 1.66	0.1 –	V
Ratio ($V_{out(low)}$ Detect Threshold / V_{REF}) (Note 5)	FB falling	$V_{out(low)}/V_{REF}$	95.0	95.5	96.0	%
Ratio ($V_{out(low)}$ Detect Hysteresis / V_{REF}) (Note 5)	FB rising	$H_{out(low)}/V_{REF}$	–	–	0.5	%
SKIP MODE						
Duty Cycle	V_{pin2} = 3 V	D_{MIN}	–	–	0	%
RAMP CONTROL (valid for the two phases)						
Maximum DRV1 and DRV2 On−Time (FB pin grounded) T_J = −25°C to +125°C	V_{pin7} = 1.1 V, I_{pin3} = 50 μA V_{pin7} = 1.1 V, I_{pin3} = 200 μA (Note 5) V_{pin7} = 2.2 V, I_{pin3} = 100 μA (Note 5) V_{pin7} = 2.2 V, I_{pin3} = 400 μA (Note 5)	t_{on1} t_{on2} t_{on3} t_{on4}	14.5 1.10 4.00 0.35	19.5 1.35 5.00 0.41	22.5 1.60 6.00 0.48	μs
Maximum DRV1 and DRV2 On−Time (FB pin grounded) T_J = −40°C to +125°C	V_{pin7} = 1.1 V, I_{pin3} = 50 μA V_{pin7} = 1.1 V, I_{pin3} = 200 μA (Note 5) V_{pin7} = 2.2 V, I_{pin3} = 100 μA (Note 5) V_{pin7} = 2.2 V, I_{pin3} = 400 μA (Note 5)	t_{on1} t_{on2} t_{on3} t_{on4}	14.0 1.05 3.84 0.33	19.5 1.35 5.00 0.41	22.5 1.60 6.00 0.48	μs

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Table 2. TYPICAL ELECTRICAL CHARACTERISTICS TABLE (Conditions: V_{CC} = 15 V, V_{pin7} = 2 V, V_{pin10} = 0 V; for typical values T_J = 25°C, for min/max values T_J = −55°C to +125°C, unless otherwise specified) (Note 6)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
RAMP CONTROL (valid for the two phases)						
Maximum DRV1 and DRV2 On−Time (FB pin grounded) T_J = −55°C to +125°C	V_{pin7} = 1.1 V, I_{pin3} = 50 μA (Note 6) V_{pin7} = 1.1 V, I_{pin3} = 200 μA (Note 5) V_{pin7} = 2.2 V, I_{pin3} = 100 μA (Note 5) V_{pin7} = 2.2 V, I_{pin3} = 400 μA (Note 5)	t_{on1} t_{on2} t_{on3} t_{on4}	13.0 1.00 3.70 0.32	19.5 1.35 5.00 0.41	22.5 1.60 6.00 0.48	μs
Pin 3 voltage	V_{BO} = V_{pin7} = 1.1 V, I_{pin3} = 50 μA V_{BO} = V_{pin7} = 1.1 V, I_{pin3} = 200 μA V_{BO} = V_{pin7} = 2.2 V, I_{pin3} = 50 μA V_{BO} = V_{pin7} = 2.2 V, I_{pin3} = 200 μA	V_{Rt1} V_{Rt2} V_{Rt3} V_{Rt4}	1.071 1.071 2.169 2.169	1.096 1.096 2.196 2.196	1.121 1.121 2.223 2.223	V
Maximum V_{ton} Voltage	Not tested	$V_{ton(MAX)}$		5		V
Pin 3 Current Capability		$I_{Rt(MAX)}$	1	–	–	mA
Pin 3 sourced current below which the controller is OFF		$I_{Rt(off)}$		7		μA
Pin 3 Current Range	Not tested	$I_{Rt(range)}$	20		1000	μA
ZERO VOLTAGE DETECTION CIRCUIT (valid for ZCD1 and ZCD2)						
ZCD Threshold Voltage	V_{ZCD} increasing V_{ZCD} falling	$V_{ZCD(TH),H}$ $V_{ZCD(TH),L}$	0.40 0.20	0.50 0.25	0.60 0.30	V
ZCD Hysteresis	V_{ZCD} decreasing	$V_{ZCD(HYS)}$		0.25		V
Input Clamp Voltage High State Low State	 I_{pin1} = 5.0 mA I_{pin1} = −5.0 mA	 $V_{ZCD(high)}$ $V_{ZCD(low)}$	 9.0 −1.1	 11 −0.65	 13 −0.1	V
Internal Input Capacitance (Note 5)		C_{ZCD}	–	10	–	pF
ZCD Watchdog Delay		t_{ZCD}	80	200	320	μs
BROWN−OUT DETECTION						
Brown−Out Comparator Threshold		$V_{BO(TH)}$	0.97	1.00	1.03	V
Brown−Out Current Source	T_J = −40°C to 125°C T_J = −55°C to +125°C (Note 6)	I_{BO}	6 5.7	7 7	8 8	μA
Brown−Out Blanking Time (Note 5)	T_J = −40°C to 125°C T_J = −55°C to +125°C	$t_{BO(BLANK)}$	38 38	50 50	62 63.5	ms
Brown−Out Monitoring Window (Note 5)		$t_{BO(window)}$	38	50	62	ms
Pin 7 clamped voltage if V_{BO} < $V_{BO(TH)}$ during $t_{BO(BLANK)}$	I_{pin7} = −100 μA	$V_{BO(clamp)}$	–	965	–	mV
Current Capability of the BO Clamp		$I_{BO(clamp)}$	100	–	–	μA
Hysteresis $V_{BO(TH)}$ − $V_{BO(clamp)}$	I_{pin7} = − 100 μA	$V_{BO(HYS)}$	10	35	60	mV
Current Capability of the BO pin Clamp PNP Transistor		$I_{BO(PNP)}$	100	–	–	μA
Pin BO voltage when clamped by the PNP	I_{pin7} = − 100 μA	$V_{BO(PNP)}$	0.35	0.70	0.90	V
OVER AND UNDER VOLTAGE PROTECTIONS						
Over−Voltage Protection Threshold		V_{OVP}	2.425	2.500	2.575	V
Ratio (V_{OVP} / V_{REF}) (Note 5)		V_{OVP}/V_{REF}	99.2	99.7	100.2	%
Ratio UVP Threshold over V_{REF}		V_{UVP}/V_{REF}	8	12	16	%

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Table 2. TYPICAL ELECTRICAL CHARACTERISTICS TABLE (Conditions: V_{CC} = 15 V, V_{pin7} = 2 V, V_{pin10} = 0 V; for typical values T_J = 25°C, for min/max values T_J = −55°C to +125°C, unless otherwise specified) (Note 6)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
OVER AND UNDER VOLTAGE PROTECTIONS						
Pin 8 Bias Current	V_{pin8} = 2.5 V V_{pin8} = 0.3 V	$I_{OVP(bias)}$	−500	–	500	nA
LATCH INPUT						
Pin Latch Threshold for Shutdown		V_{Latch}	2.375	2.500	2.625	V
Pin Latch Bias Current	V_{pin10} = 2.3 V	$I_{Latch(bias)}$	−500	–	500	nA
pfcOK / REF5V						
Pin 15 Voltage Low State	V_{pin7} = 0 V, I_{pin15} = 250 μA	$V_{REF5V(low)}$	–	60	120	mV
Pin 15 Voltage High State	V_{pin7} = 0 V, I_{pin15} = 5 mA	$V_{REF5V(high)}$	4.7	4.85	5.3	V
Current Capability		I_{REF5V}	5	10	–	mA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold		T_{SHDN}	130	140	150	°C
Thermal Shutdown Hysteresis		$T_{SHDN(HYS)}$	–	50	–	°C

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7. Guaranteed by design, the VCC pin can handle the double of the DRV peak source current, that is, 1 A typically.

Table 3. DETAILED PIN DESCRIPTION

Pin Number	Name	Function
1	ZCD2	This is the zero current detection pin for phase 2 of the interleaved PFC stage. Apply the voltage from an auxiliary winding to detect the core reset of the inductor and the valley of the MOSFET drain source voltage
2	FB	This pin receives a portion of the pre−converter output voltage. This information is used for the regulation and the “output low” detection (V_{OUT}L) that drastically speed−up the loop response when the output voltage drops below 95.5% of the wished level.
3	R_T	The resistor placed between pin 3 and ground adjusts the maximum on−time of our system for both phases, and hence the maximum power that can be delivered by the PFC stage.
4	OSC	Connect a capacitor to set the clamp frequency of the PFC stage. If wished, this frequency can be reduced in light load as a function of the resistor placed between pin 6 and ground (frequency fold−back). If the coil current cycle is longer than the selected switching period, the circuit delays the next cycle until the core is reset. Hence, the PFC stage can operate in Critical Conduction Mode in the most stressful conditions.
5	$V_{Control}$	The error amplifier output is available on this pin. The capacitor connected between this pin and ground adjusts the regulation loop bandwidth that is typically set below 20 Hz to achieve high Power Factor ratios. Pin5 is grounded when the circuit is off so that when it starts operation, the power increases slowly (soft−start).
6	Freq. Foldback	Apply a resistor between pin 6 and ground to adjust the oscillator charge current. Clamped not to exceed 100 μA, this charge current is made proportional to the power level for a reduced switching frequency at light load and an optimum efficiency over the load range.
7	BO (Brown−out Protection)	Apply an averaged portion of the input voltage to detect brown−out conditions when V_{pin2} drops below 1 V. A 50−ms internal delay blanks short mains interruptions to help meet hold−up time requirements. When it detects a brown−out condition, the circuit stops pulsing and grounds the “pfcOK” pin to disable the downstream converter. Also an internal 7−μA current source is activated to offer a programmable hysteresis. The pin2 voltage is internally re−used for feed−forward. Grounding pin 7 disables the part (after the 50−ms blanking time has elapsed).
8	OVP / UVP	The circuit turns off when V_{pin9} goes below 480 mV (UVP) and disables the drive as long as the pin voltage exceeds 2.5 V (OVP).
9	CS	This pin monitors a negative voltage proportional to the coil current. This signal is sensed to limit the maximum coil current and protect the PFC stage in presence of in−rush currents.
10	Latch	Apply a voltage higher than 2.5 V to latch−off the circuit. The device is reset by unplugging the PFC stage (practically when the circuit detects a brown−out detection) or by forcing the circuit V_{CC} below V_{CC}RST (4 V typically). Operation can then resume when the line is applied back.
11	DRV2	This is the gate drive pin for phase 2 of the interleaved PFC stage. The high current capability of the totem pole gate drive (+0.5/−0.8 A) makes it suitable to effectively drive high gate charge power MOSFETs.
12	V_{CC}	This pin is the positive supply of the IC. The circuit starts to operate when V_{CC} exceeds 12 V and turns off when V_{CC} goes below 10 V (typical values). After start−up, the operating range is 9.5 V up to 20 V.
13	GND	Connect this pin to the pre−converter ground.
14	DRV1	This is the gate drive pin for phase 1 of the interleaved PFC stage. The high current capability of the totem pole gate drive (+0.5/−0.8 A) makes it suitable to effectively drive high gate charge power MOSFETs.
15	REF5V / pfcOK	The pin15 voltage is high (5 V) when the PFC stage is in a normal, steady state situation and low otherwise. This signal serves to “inform” the downstream converter that the PFC stage is ready and that hence, it can start operation.
16	ZCD1	This is the zero current detection pin for phase 1 of the interleaved PFC stage. Apply the voltage from an auxiliary winding to detect the core reset of the inductor and the valley of the MOSFET drain source voltage.

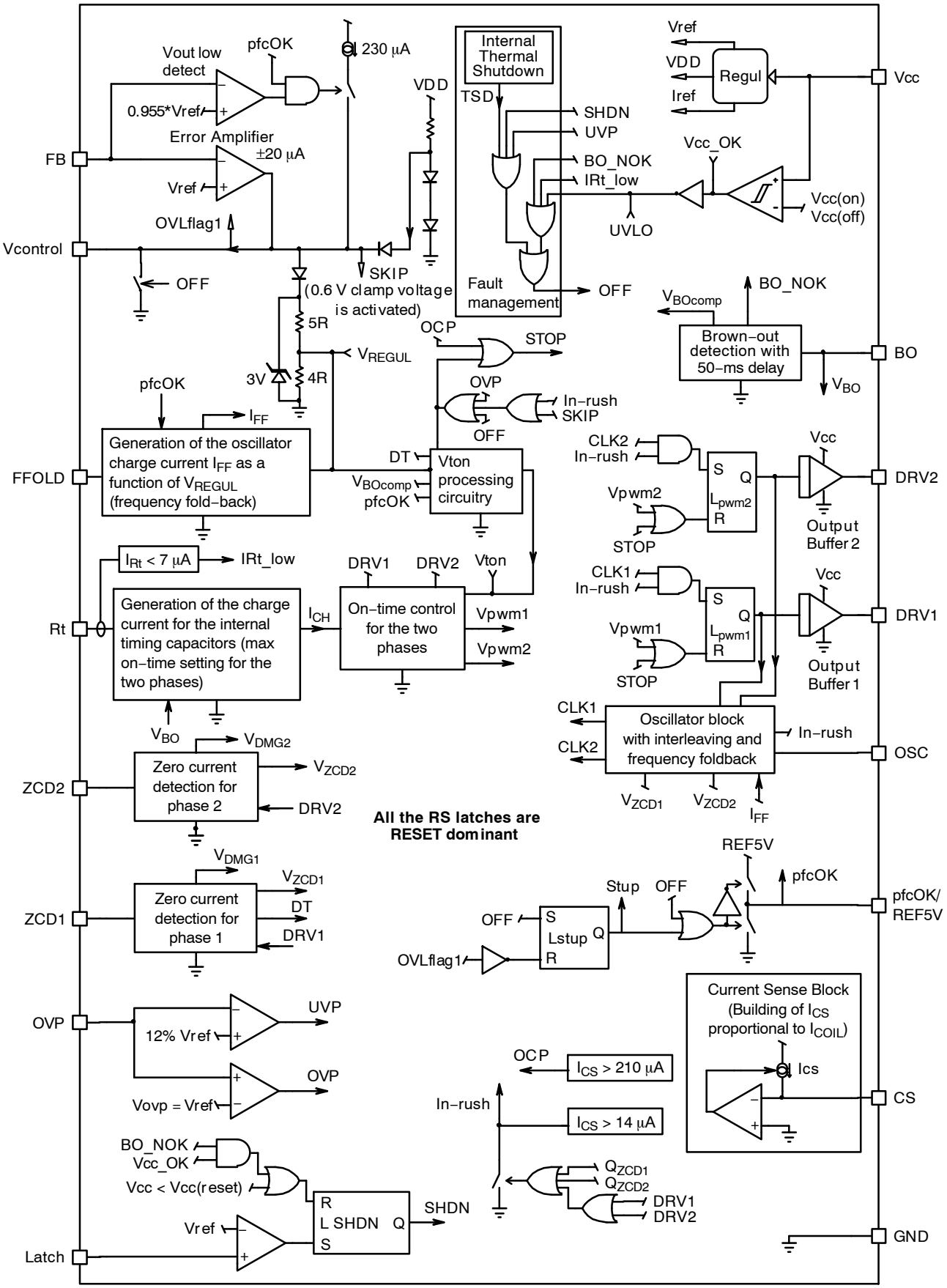


Figure 2. Functional Block Diagram

Detailed Operating Description

The NCP1631 integrates a dual MOSFET driver for interleaved, 2−phase PFC applications. It drives the two branches in so−called ***F**requency **C**lamped **C**ritical conductio**n** **M**ode* (**FCCrM**) where each phase operates in ***C**ritical conduction **M**ode* (CrM) in the most stressful conditions and in ***D**iscontinuous **C**onduction **M**ode* (DCM) otherwise, acting as a CrM controller with a frequency clamp (given by the oscillator). According to the conditions, the PFC stage actually jumps from DCM to CrM (and vice versa) with no discontinuity in operation and without degradation of the current shape.

Furthermore, the circuit incorporates protection features for a rugged operation together with some special circuitry to lower the power consumed by the PFC stage in no−load conditions. More generally, the NCP1631 is ideal in systems where cost−effectiveness, reliability, low stand−by power and high power factor are the key parameters:

Fully Stable FCCrM and Out−Of−Phase Operation.

Unlike master/slave controllers, the NCP1631 utilizes an interactive−phase approach where the two branches operate independently. Hence, the two phases necessarily operate in FCCrM, preventing risks of undesired dead−times or continuous conduction mode sequences. In addition, the circuit makes them interact so that they run out−of−phase. The NCP1631 unique interleaving technique substantially maintains the wished 180° phase shift between the 2 branches, in all conditions including start−up, fault or transient sequences.

Optimized Efficiency Over The Full Power Range.

The NCP1631 optimizes the efficiency of your PFC stage in the whole line/load range. Its clamp frequency is a major contributor at nominal load. For medium and light load, the clamp frequency linearly decays as a function of the power to maintain high efficiency levels even in very light load. The power threshold under which frequency reduces is programmed by the resistor placed between pin 6 and ground. To prevent any risk of regulation loss at no load, the circuit further skips cycles when the error amplifier reaches its low clamp level.

Fast Line / Load Transient Compensation.

Characterized by the low bandwidth of their regulation loop, PFC stages exhibit large over and under−shoots when abrupt load or line transients occur (e.g. at start−up). The NCP1631 dramatically narrows the output voltage range. First, the controller dedicates one pin to set an accurate Over−Voltage Protection level and interrupts the power delivery as long as the output voltage exceeds this threshold. Also, the NCP1631 ***dynamic response enhancer*** drastically speeds−up the regulation loop when the output voltage is 4.5% below its desired level. As a matter of fact, a PFC stage provides the downstream converter with a very narrow voltage range.

A “pfcOK” signal.

The circuit detects when the PFC stage is in steady state or if on the contrary, it is in a start−up or fault condition. In the first case, the “pfcOK” pin (pin15) is in high state and low otherwise. This signal is to disable the downstream converter unless the bulk capacitor is charged and no fault is detected. Finally, the downstream converter can be optimally designed for the narrow voltage provided by the PFC stage in normal operation.

Safety Protections.

The NCP1631 permanently monitors the input and output voltages, the input current and the die temperature to protect the system from possible over−stresses and make the PFC stage extremely robust and reliable. In addition to the aforementioned OVP protection, one can list:

Maximum Current Limit: the circuit permanently senses the total input current and prevents it from exceeding the preset current limit, still maintaining the out−of−phase operation.

In−rush Detection: the NCP1631 prevents the power switches turn on for the large in−rush currents sequence that occurs during the start−up phase.

Under−Voltage Protection: this feature is mainly to prevent operation in case of a failure in the OVP monitoring network (e.g., bad connection).

Brown−Out Detection: the circuit stops operating if the line magnitude is too low to protect the PFC stage from the excessive stress that could damage it in such conditions.

Thermal Shutdown: the circuit stops pulsing when its junction temperature exceeds 150°C typically and resumes operation once it drops below about 100°C (50°C hysteresis).

NCP1631 Operating Modes

The NCP1631 drives the two branches of the interleaved in FCCrM where each phase operates in *Critical conduction Mode* (CrM) in the most stressful conditions and in *Discontinuous Conduction Mode* (DCM) otherwise, acting as a CrM controller with a frequency clamp (given by the oscillator). According to the conditions, the PFC stage actually jumps from DCM to CrM (and vice versa) with no discontinuity in operation and without degradation of the current shape.

The circuit can also transition within an ac line cycle so that:

- CrM reduces the current stress around the sinusoid top.
- DCM limits the frequency around the line zero crossing.

This capability offers the best of each mode without the drawbacks. The way the circuit modulates the MOSFET on−time allows this facility.

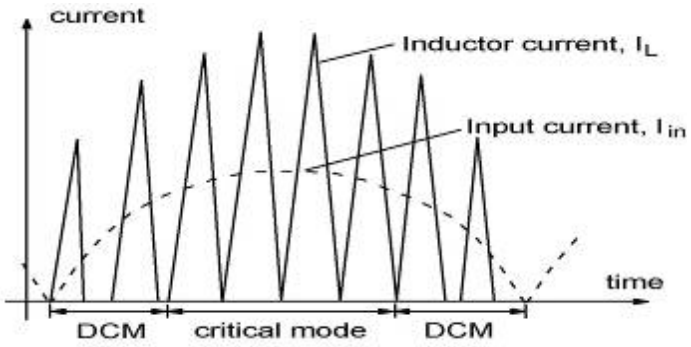


Figure 3. DCM and CRM Operation Within a Sinusoid Cycle for One Branch

NCP1631 On−time Modulation

Let's study the ac line current absorbed by one phase of the interleaved PFC converter.

The current waveform of the inductor (L) during one switching period (T_{sw}) is portrayed by Figure 5.

The ac line current is the averaged value of the coil current as the result of the EMI filter "polishing" action. Hence, the line current produced by one of the phase is:

$$I_{in} = \frac{1}{2}\left(\frac{t_1}{L}\right)\left(\frac{t_1 + t_2}{T_{sw}}\right)V_{in} \qquad \text{(eq. 1)}$$

Where ($T_{sw} = t_1 + t_2 + t_3$) is the switching period and V_{in} is the ac line rectified voltage.

Equation 1 shows that I_{in} is proportional to V_{in} if $\left(\frac{t_1(t_1 + t_2)}{T_{sw}}\right)$ is a constant.

Forcing $\left(\frac{t_1(t_1 + t_2)}{T_{sw}}\right)$ constant is what the NCP1631 does to perform ***FCCrM*** operation that is, to operate in discontinuous or critical conduction mode according to the conditions, without degradation of the power factor.

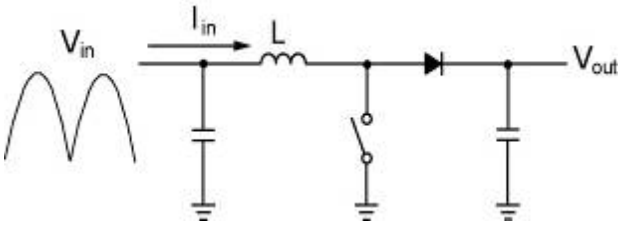


Figure 4. Boost Converter

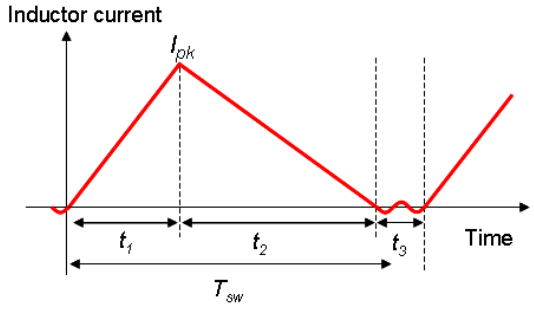


Figure 5. Inductor Current in DCM

The NCP1631 operates in voltage mode. As portrayed by Figure 6, the MOSFET on time t_1 is controlled by the signal V_{ton} generated by the regulation block as follows:

$$t_1 = \frac{C_t V_{TON}}{I_t} \qquad \text{(eq. 2)}$$

Where:

- C_t is the internal timing capacitor
- I_t is the internal current source for the timing capacitor.

The I_t charge current is constant for a given resistor placed on the R_t pin. C_t is also a constant. Hence, the condition

$$\left(\frac{t_1(t_1 + t_2)}{T_{sw}}\right)$$

to be a constant for proper power factor correction can be changed into:

$\left(\frac{V_{TON}(t_1 + t_2)}{T_{sw}}\right)$ is constant.

The output of the regulation block ($V_{CONTROL}$) is linearly changed into a signal (V_{REGUL}) varying between 0 and 1.66 V. (V_{REGUL}) is the voltage that is injected into the PWM section to modulate the MOSFET duty−cycle. However, the NCP1631 inserts some circuitry that processes (V_{REGUL}) to form the signal (V_{TON}) that is used in the PWM section instead of (V_{REGUL}) (see Figure 7). (V_{TON}) is modulated in response to the dead−time sensed during the precedent current cycles, that is, for a proper shaping of the ac line current. This modulation leads to:

$$V_{TON} = \frac{T_{sw} V_{REGUL}}{t_1 + t_2} \quad \text{or:} \quad V_{TON}\frac{t_1 + t_2}{T_{sw}} = V_{REGUL} \qquad \text{(eq. 3)}$$

Substitution of Equation 3 into Equation 2 leads to the following on−time expression:

$$t_1 = \frac{C_t\left(\frac{T_{sw} V_{REGUL}}{t_1 + t_2}\right)}{I_t} \qquad \text{(eq. 4)}$$

Replacing "t_1" by its expression of Equation 4, Equation 1 simplifies as follows:

$$I_{in(phase1)} = I_{in(phase2)} = \frac{V_{in}}{2L}\frac{C_t V_{REGUL}}{I_t} \qquad \text{(eq. 5)}$$

Given the regulation low bandwidth of the PFC systems, ($V_{CONTROL}$) and then (V_{REGUL}) are slow varying signals. Hence, the line current absorbed by each phase is:

$$I_{in(phase1)} = I_{in(phase2)} = k\,V_{in} \qquad \text{(eq. 6)}$$

$$\text{where: } k = \text{constant} = \left[\frac{C_t V_{REGUL}}{2\,L\,I_t}\right]$$

Hence, the input current is then proportional to the input voltage and the ac line current is properly shaped.

One can note that this analysis is also valid for CrM operation that is just a particular case of this functioning where (t_3=0), which leads to (t_1+t_2=T_{sw}) and (V_{TON}=V_{REGUL}). That is why the NCP1631 automatically adapts to the conditions and jumps from DCM and CrM (and vice versa) without power factor degradation and without discontinuity in the power delivery.

The charging current I_t is internally processed to be proportional to the square of the line magnitude. Its value is however programmed by the pin 3 resistor to adjust the available on−time as defined by the T_{on1} to T_{on4} parameters of the data sheet.

From these data, we can deduce:

$$t_1 = T_{on}(\mu s) = 50\,n\frac{R_t{}^2}{V_{pin7}{}^2} \qquad \text{(eq. 7)}$$

From this equation, we can check that if V_{pin7} (BO voltage) is 1 V and R_t is 20 kΩ (I_{pin3} = 50 μA) that the on−time is 20 μs as given by parameter T_{on1}.

Since:

$$V_{REGUL(max)} = 1.66\ V$$

$$T_{on} = \frac{C_t V_{REGUL}}{I_t}$$

$$V_{pin7} = \frac{2\sqrt{2}\ V_{in(rms)}}{\pi} k_{BO}$$

where $\mathbf{k_{BO}}$ is the scale down factor of the BO sensing network

$$\left(k_{BO} = \frac{R_{bo2}}{R_{bo1} + R_{bo2}}\right)$$

(see Brown−out section)

We can deduce the total input current value and the average input power:

$$I_{in(rms)} \cong \frac{(R_t)^2 V_{REGUL}}{26.9 \cdot 10^{12}\,L\,k_{BO}{}^2 V_{in,rms}} \qquad \text{(eq. 8)}$$

$$P_{in,avg} \cong \frac{(R_t)^2 V_{REGUL}}{26.9 \cdot 10^{12}\,L\,k_{BO}{}^2} \qquad \text{(eq. 9)}$$

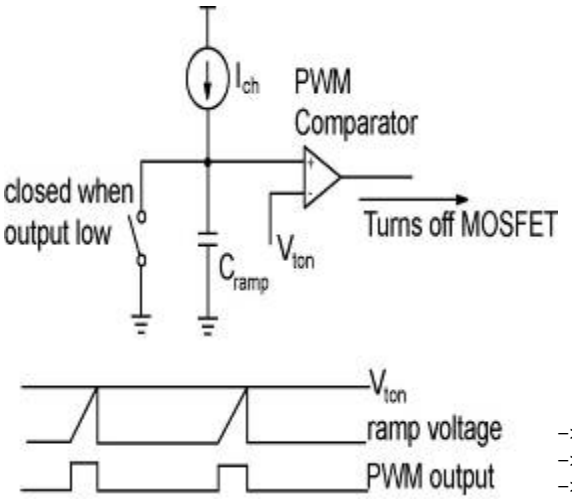
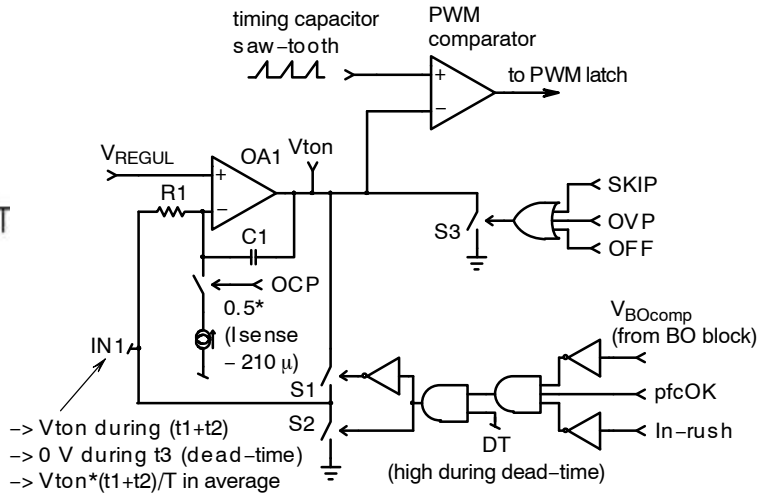


Figure 6. PWM Circuit and Timing Diagram



The integrator OA1 amplifies the error between V_{REGUL} and IN1 so that in average, (V_{TON}*(t_1+t_2)/T_{sw}) equates V_{REGUL}.

Figure 7. V_{TON} Processing Circuit

The "V_{TON} processing circuit" is "informed" when there is an OVP condition or a skip sequence, not to over−dimension V_{TON} in that conditions. Otherwise, an OVP sequence or a skipped cycle would be viewed as a "normal" dead−time phase by the circuit and V_{TON} would inappropriately increase to compensate it. (Refer to Figure 7).

The output of the "V_{TON} processing circuit" is also grounded when the circuit is in OFF state to discharge the capacitor C1 and initialize it for the next active phase.

Finally, the "V_{TON}" is not allowed to be further increased compared to V_{REGUL} when the circuit has not completed the start−up phase (pfcOK low) and if V_{BOcomp} from the brown−out block is high (refer to brown−out section for more information).

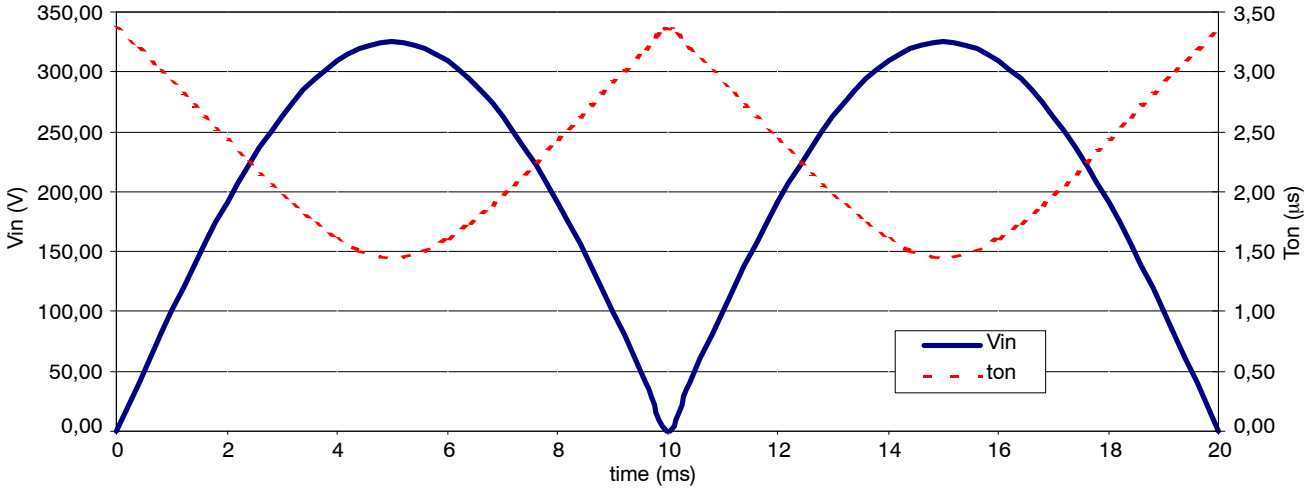


Figure 8. Input Voltage and On−time vs. Time (example with F_{SW} = 100 kHz, Pin = 150 W, V_{AC} = 230 V, L = 200 µH)

Regulation Block and Low Output Voltage Detection

A trans−conductance error amplifier with access to the inverting input and output is provided. It features a typical trans−conductance gain of 200 µS and a typical capability of ±20 µA. The output voltage of the PFC stage is typically scaled down by a resistors divider and monitored by the inverting input (feed−back pin – pin2). The bias current is minimized (less than 500 nA) to allow the use of a high impedance feed−back network. The output of the error amplifier is pinned out for external loop compensation (pin5). Typically a type−2 compensator is applied between pin5 and ground, to set the regulation bandwidth below 20 Hz, as need in PFC applications (refer to application note AND8407).

The swing of the error amplifier output is limited within an accurate range:

- It is forced above a voltage drop (V_F) by the “low clamp” circuitry. When this circuitry is activated, the power demand is minimum and the NCP1631 enters skip mode (the controller stops pulsating) until the clamp is no more active.
- It is clamped not to exceed 3.0 V + the same V_F voltage drop.

Hence, V_{pin5} features a 3 V voltage swing. V_{pin5} is then offset down by (V_F) and further divided before it connects to the “V_{ton} processing block” and the PWM section. Finally, the output of the regulation is a signal (“V_{REGUL}” of the block diagram) that varies between 0 and 1.66 V.

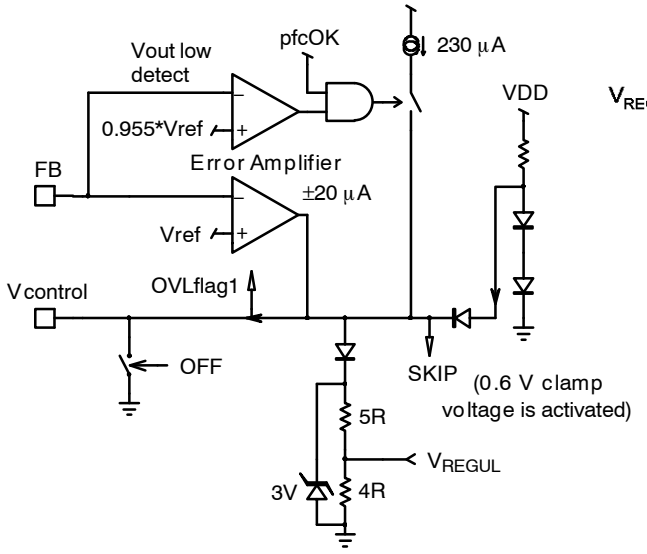


Figure 9. Regulation Block

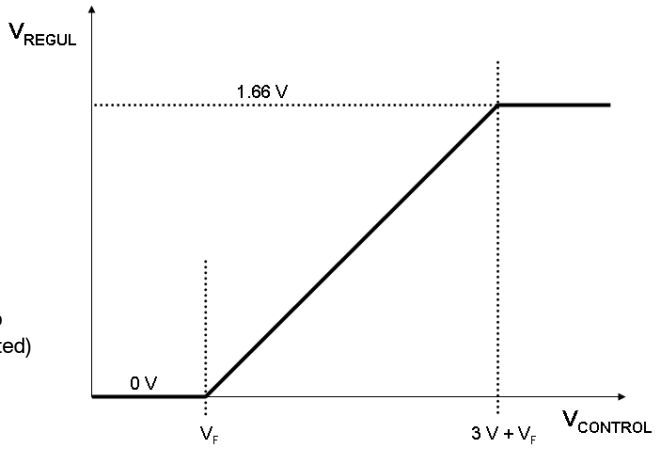


Figure 10. Correspondence Between $V_{CONTROL}$ and V_{REGUL}

Provided the low bandwidth of the regulation loop, sharp variations of the load, may result in excessive over and under−shoots. Over−shoots are limited by the Over−Voltage Protection (see OVP section). To contain the under−shoots, an internal comparator monitors the feed−back signal (V_{pin2}) and when V_{pin2} is lower than 95.5% of its nominal value, it connects a 230 μA current source to speed−up the charge of the compensation capacitor (C_{pin5}). Finally, it is like if the comparator multiplied the error amplifier gain by 10.

One must note that this circuitry for under−shoots limitation, is not enabled during the start−up sequence of the PFC stage but only once the converter has stabilized (that is when the "pfcOK" signal of the block diagram, is high). This is because, at the beginning of operation, the pin5 capacitor must charge slowly and gradually for a soft start−up.

Zero Current Detection

While the on time is constant, the core reset time varies with the instantaneous input voltage. The NCP1631 determines the demagnetization completion by sensing the inductor voltage, more specifically, by detecting when the inductor voltage drops to zero.

Practically, an auxiliary winding in flyback configuration is taken off of the boost inductor and gives a scaled down version of the inductor voltage that is usable by the controller (Figure 12). In that way, the ZCD voltage ("V_{AUX}") falls and starts to ring around zero volts when the inductor current drops to zero. The NCP1631 detects this falling edge and allows the next driver on time.

Figure 1 shows how it is implemented.

For each phase, a comparator detects when the voltage of the ZCD winding exceeds 0.5 V. When this is the case, the coil is in demagnetization phase and the latch L_{ZCD} is set. This latch is reset when the next driver pulse occurs.

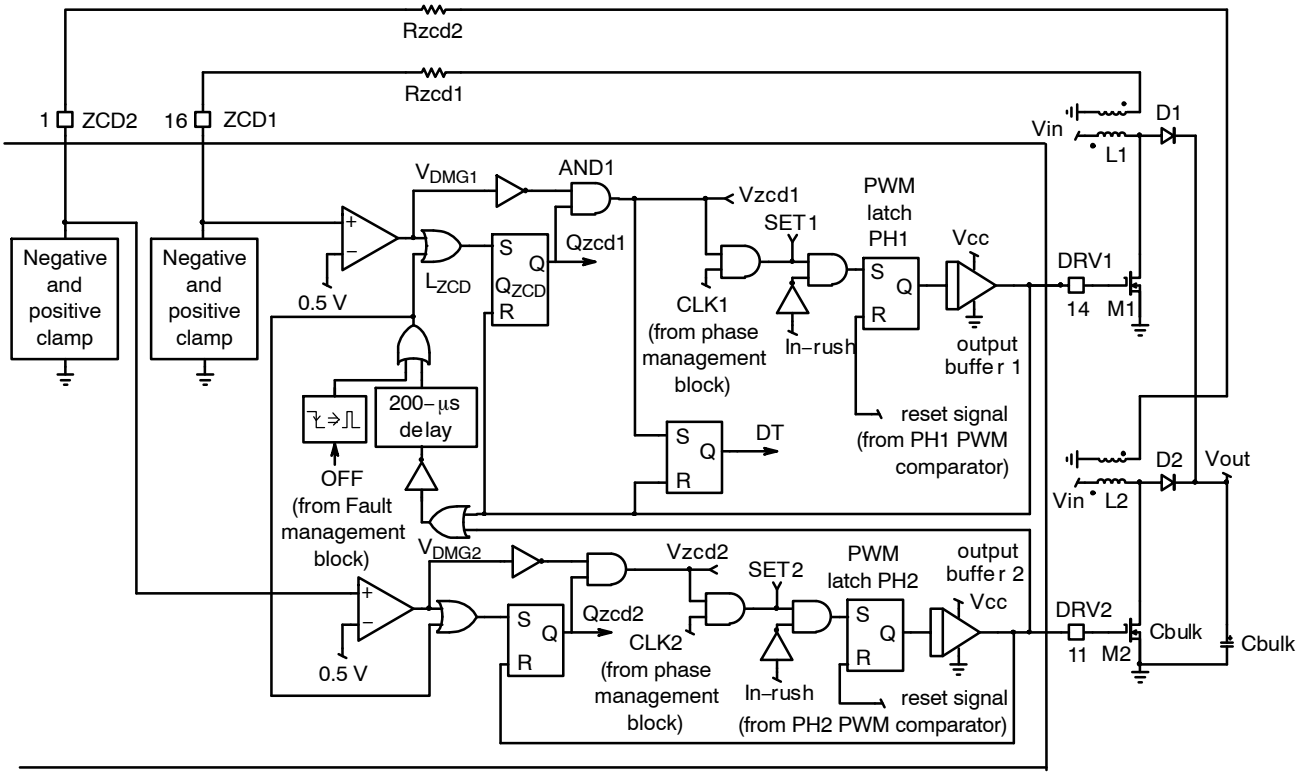


Figure 11. Zero Current Detection

To prevent negative voltages on the ZCD pins (ZCD1 for phase 1 and ZCD2 for phase 2), these pins are internally clamped to about 0 V when the voltage applied by the corresponding ZCD winding is negative. Similarly, the ZCD pins are clamped to $V_{ZCD(high)}$ (10 V typical), when the ZCD voltage rises too high. Because of these clamps, a resistor (R_{ZCD} of Figure 11) is necessary to limit the current from the ZCD winding to the ZCD pin. The clamps are designed to respectively source and sink 5 mA minimum. It is recommended not to exceed this 5 mA level within the ZCD clamps for a proper operation.

At startup or after an inactive period (because of a protection that has tripped for instance), there is no energy in the ZCD winding and therefore no voltage signal to activate the ZCD comparator. This means that the driver will never turn on. To avoid this, an internal watchdog timer is integrated into the controller. If the driver remains low for more than 200 μs (typical), the timer sets the L_{ZCD} latch as the ZCD winding signal would do. Obviously, this 200−μs delay acts as a minimum off−time if there is no demagnetization winding while it has no action if there is a ZCD voltage provided by the auxiliary winding.

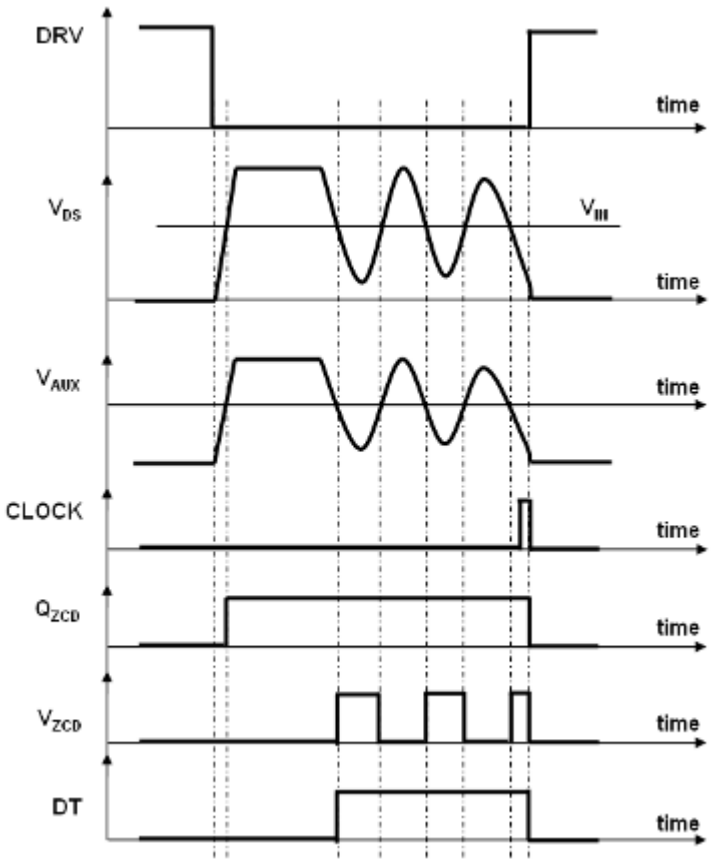


Figure 12. Zero Current Detection Timing Diagram (V_{AUX} is the Voltage Provided by the ZCD Winding)

Current Sense

The NCP1631 is designed to monitor a negative voltage proportional to total input current, i.e., the current drawn by the two interleaved branches (I_{in}). As portrayed by Figure 13, a current sense resistor (R_{CS}) is practically inserted within the return path to generate a negative voltage (V_{CS}) proportional to I_{in}. The circuit uses V_{CS} to detect when I_{in} exceeds its maximum permissible level. To do so, the circuit incorporates an operational amplifier that sources the current necessary to maintain the CS pin voltage null (refer to Figure 13). By inserting a resistor R_{OCP} between the CS pin and R_{CS}, we adjust the current that is sourced by the CS pin (I_{CS}) as follows:

$$- [R_{CS} I_{COIL}] + [R_{OCP} I_{CS}] = 0 \qquad \text{(eq. 10)}$$

Which leads to:

$$I_{CS} = \frac{R_{CS}}{R_{OCP}} I_{COIL} \qquad \text{(eq. 11)}$$

In other words, the pin 9 current (I_{CS}) is proportional to the coil current.

A negative clamp protects the circuit from the possible negative voltage that can be applied to the pin. This protection is permanently active (even if the circuit off). The clamp is designed to sustain 5 mA. It is recommended not to sink more than 5 mA from the CS pin for a proper operation.

Two functions use I_{CS}: the over current protection and the in−rush current detection.

Over−Current Protection (OCP)

If I_{CS} exceeds I_{ILIM1} (210 μA typical), an over−current is detected and the on−time is decreased proportionally to the difference between the sensed current I_{IN} and the 210 μA OCP threshold.

The on−time reduction is done by injecting a current I_{neg} in the negative input of the "V_{TON} processing circuit" OPAMP. (See Figure 7)

$$I_{neg} = 0.5(I_{CS} - 210\ \mu) \qquad \text{(eq. 12)}$$

This current is injected each time the OCP signal is high.

The maximum coil current is:

$$I_{COIL(max)} = \frac{R_{OCP}}{R_{CS}} I_{ILIM1} \qquad \text{(eq. 13)}$$

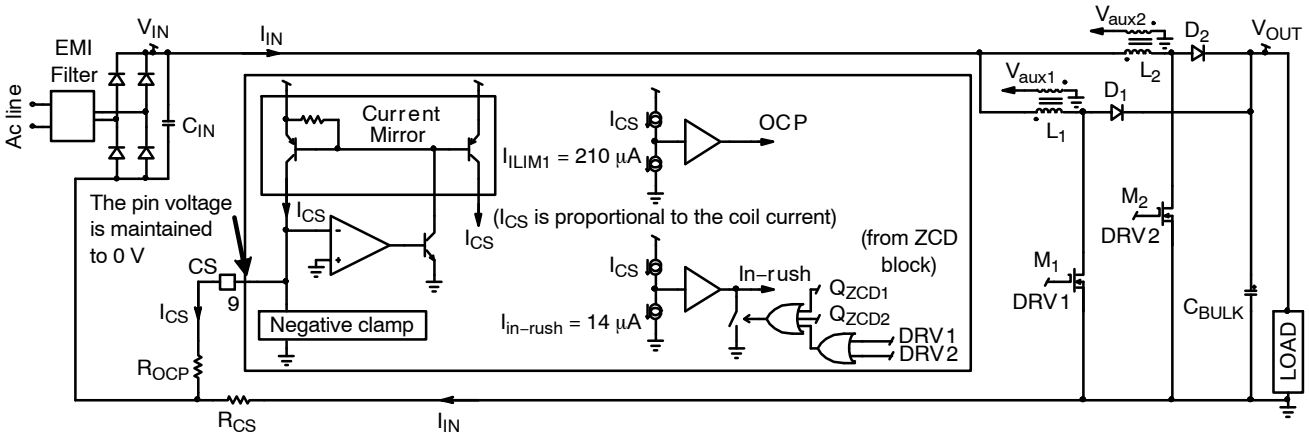
In−rush Current Detection

When the PFC stage is plugged to the mains, the bulk capacitor is abruptly charged to the line voltage. The charge current (named in−rush current) can be very huge

depending on the presence or absence of an effective in−rush limiting circuitry. If the MOSFET turns on during this severe transient, it may be over−stressed and finally damaged. That is why, the NCP1631 permanently monitors the input current and delays the MOSFET turn on until the in−rush current has vanished. This is the function of the I_{CS} comparison to the $I_{in-rush}$ threshold (14 μA typical). When I_{CS} exceeds $I_{in-rush}$, the comparator output (“In−rush”) is high and prevents the PWM latches from setting (see block diagram). Hence, the two drivers cannot turn high and the MOSFETs cannot switch on. This is to guarantee that the MOSFETs remain off as long as if the input current exceeds 10% of its maximum value. This feature protects the MOSFETs from the possible excessive stress it could suffer from if it was allowed to turn on while a huge current flowed through the coil as it can be the case at start−up or during an over−load transient.

The propagation delay (I_{CS} < $I_{in-rush}$) to (drive outputs high) is in the range of few μs.

However when the circuit starts to operate, the NCP1631 disables this protection to avoid that the current produced by one phase and sensed by the circuit prevents the other branch from operating. Practically, some logic grounds the In−rush protection output when it detects the presence of current cycles with a zero current detection signal provided by the auxiliary winding (Figure 13).



The CS block performs the over−current protection and the in−rush current detection.

Figure 13. Current Sense Block

Over−Voltage Protection

While PFC circuits often use one single pin for both the Over−Voltage Protection (OVP) and the feed−back, the NCP1631 dedicates one specific pin for the under−voltage and over−voltage protections. The NCP1631 configuration allows the implementation of two separate feed−back networks (see Figure 15):

1. One for regulation applied to pin 2.
2. Another one for the OVP function (pin 8).

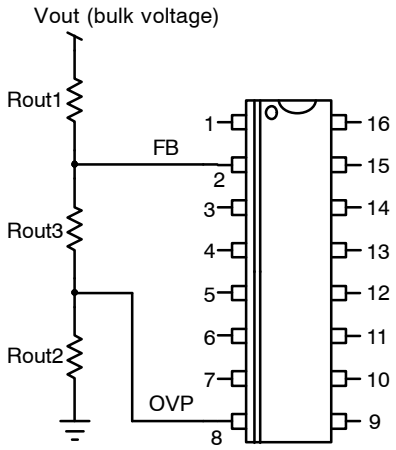


Figure 14. Configuration with One Feed−back Network for Both OVP and Regulation

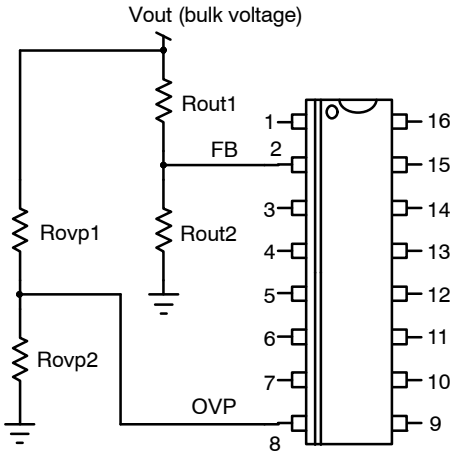


Figure 15. Configuration with Two Separate Feed−back Networks

The double feed−back configuration offers some up−graded safety level as it protects the PFC stage even if there is a failure of one of the two feed−back arrangements.

However, if wished, one single feed−back arrangement is possible as portrayed by Figure 14. The regulation and OVP blocks having the same reference voltage, the resistance ratio R_{out2} over R_{out3} adjusts the OVP threshold. More specifically,

The bulk regulation voltage ("$V_{out(nom)}$") is:

$$V_{out(nom)} = \frac{R_{out1} + R_{out2} + R_{out3}}{R_{out2} + R_{out3}} \cdot V_{ref} \qquad \text{(eq. 14)}$$

The OVP level ("$V_{out(ovp)}$") is:

$$V_{out(ovp)} = \frac{R_{out1} + R_{out2} + R_{out3}}{R_{out2}} \cdot V_{ref} \qquad \text{(eq. 15)}$$

The ratio OVP level over regulation level is:

$$\frac{V_{out(ovp)}}{V_{out(nom)}} = 1 + \frac{R_{out3}}{R_{out2}} \qquad \text{(eq. 16)}$$

For instance, ($V_{out(nom)}$ = 105% x $V_{out(nom)}$) leads to: (R_{out3} = 5% x R_{out2}).

When the circuit detects that the output voltage exceeds the OVP level, it maintains the power switch open to stop the power delivery.

As mentioned previously, the "V_{TON} processing circuit" is "informed" when there is an OVP condition, not to over−dimension V_{TON} in that conditions. Otherwise, an OVP sequence would be viewed as a dead−time phase by the circuit and V_{TON} would inappropriately increase to compensate it (refer to Figure 7).

PfcOK / REF5V Signal

The NCP1631 can communicate with the downstream converter. The signal "pfcOK/REF5V" is high (5 V) when the PFC stage is in normal operation (its output voltage is stabilized at the nominal level) and low otherwise.

More specifically, "pfcOK/REF5V" is low:

- During the PFC stage start−up, that is, as long as the output voltage has not yet stabilized at the right level. The start−up phase is detected by the latch "L_{STUP}" of the block diagram in Figure 2. "L_{STUP}" is set during each "off" phase so that its output ("STUP") is high when the circuit enters an active phase. The latch is reset when the error amplifier stops charging its output capacitor, that is, when the output voltage of the PFC stage has reached its desired regulation level. At that moment, "STUP" falls down to indicate the end of the start−up phase.
- Any time, the circuit is off or a fault condition is detected as described by the "Fault management and OFF mode" section

Finally, "pfcOK/REF5V" is high when the PFC output voltage is properly and safely regulated. "pfcOK/REF5V" should be used to allow operation of the downstream converter.

Oscillator Section – Phase Management

The oscillator generates the clock signal that dictates the maximum switching frequency for the global system (f_{osc}). In other words, each of the two interleaved branches cannot operate above the clamp frequency that is half the oscillator frequency (f_{osc}/2). The oscillator frequency (f_{osc}) is adjusted by the capacitor applied to pin 4. Typically, a **440** pF capacitor approximately leads to a 120−kHz operating frequency, meaning a 60−kHz clamp frequency for each branch. The oscillator frequency should be kept below 500 kHz (which corresponds to a pin4 capacitor in the range of **100 pF**).

As shown by Figure 16, two current sources $I_{OSC(clamp)}$ (35 μA typical) and $I_{OSC(CH)}$ (105 μA typical) charge the pin 4 capacitor until its voltage exceeds $V_{OSC(high)}$ (5 V typically). At that moment, the output of the COMP_OSC comparator ("SYNC" of Figure 16) turns high and changes the COMP_OSC reference threshold that drops from $V_{OSC(high)}$ down to $V_{OSC(low)}$ (hysteresis). The system enters a discharge phase where the I_{CH} current source is disabled and instead a sink current $I_{OSC(DISCH)}$ (105 μA typ.) discharges the pin 4 capacitor. This sequence lasts until V_{pin4} goes below $V_{OSC(low)}$ when the "SYNC" signal turns low and a new charging phase starts. A divider by two uses the "SYNC" information to manage the phases of the interleaved PFC: the first SYNC pulse sets "phase 1", the second one, "phase 2", the third one phase 1 again... etc...

According to the selected phase, the "SYNC" signal sets the relevant "Clock generator latch" that will generate the clock signal ("CLK1" for phase 1, "CLK2" for phase 2) when SYNC drops to zero (falling edge detector). So, the drivers are synchronized to SYNC falling edge.

Actually, the drivers cannot turn on at this very moment if the demagnetization of the coil is not yet complete (CrM operation). In this case, the clock signal is maintained high until the driver turns high (the clock generator latches are reset by the corresponding driver is high − reset on rising edge detector). Also, the discharge time can be prolonged if when V_{pin4} drops below $V_{OSC(low)}$, the driver of the phase cannot turn on because the core is not reset yet (CrM operation). In this case, V_{pin4} decreases until the driver turns high. The further discharge of V_{pin4} below $V_{OSC(low)}$ helps maintain a substantial 180° phase shift in CrM that is in essence, guaranteed in DCM. In the two conditions (CrM or DCM), operation is stable and robust.

Figure 17 portrays the clock signal waveforms in different cases:

- In fixed frequency operation (DCM), the cycle time of the coil current is shorter than an oscillator period. Hence, as soon as the clock signal goes high, the driver can turn on and reset the clock generator latch. The clock signal is then a short pulse.

– However, the coil current can possibly be non zero when the clock signal turns high. The circuit would enter Continuous Conduction Mode (CCM) if the MOSFET turned on in that moment. In order to avoid CCM operation, the clock is prevented from setting the PWM latch until the core is reset (that is as low as "V_{ZCD}" of Figure 8 is low). The clock signal remains high during this waiting phase (refer to Figure 12). Hence the next MOSFET conduction time occurs as soon as the coil current has totally vanished. In other words, critical conduction mode (CrM) operation is obtained.

The clamp frequency can be computed using the following equation:

$$f_{osc} \cong \frac{60\ \mu}{C_{OSC} + 10\ p} \qquad \text{(eq. 17)}$$

where C_{OSC} is the pin 4 external capacitor and C_{pin} the pin 4 parasitic capacitance (about 10 pF).

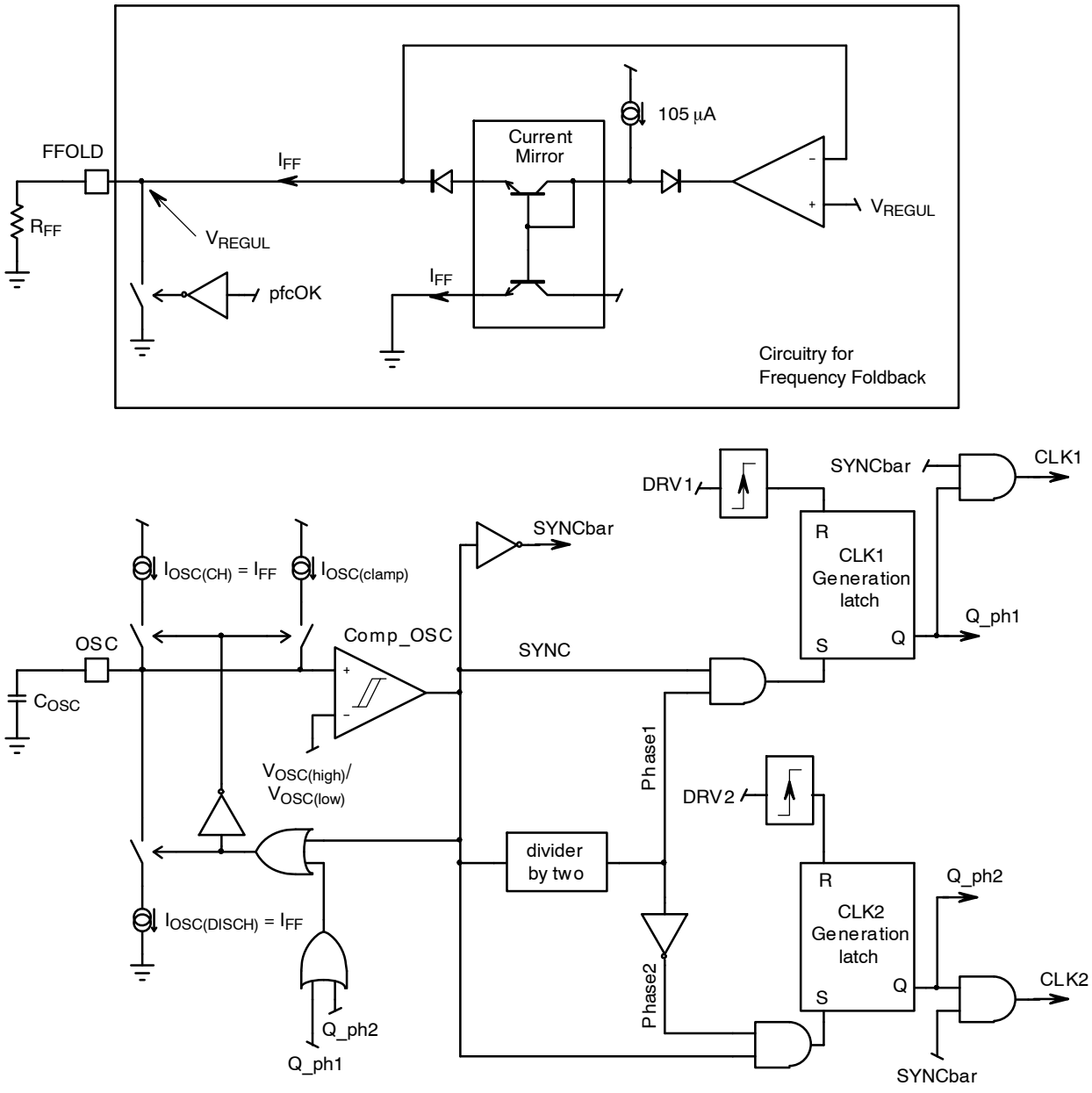


Figure 16. Oscillator Block

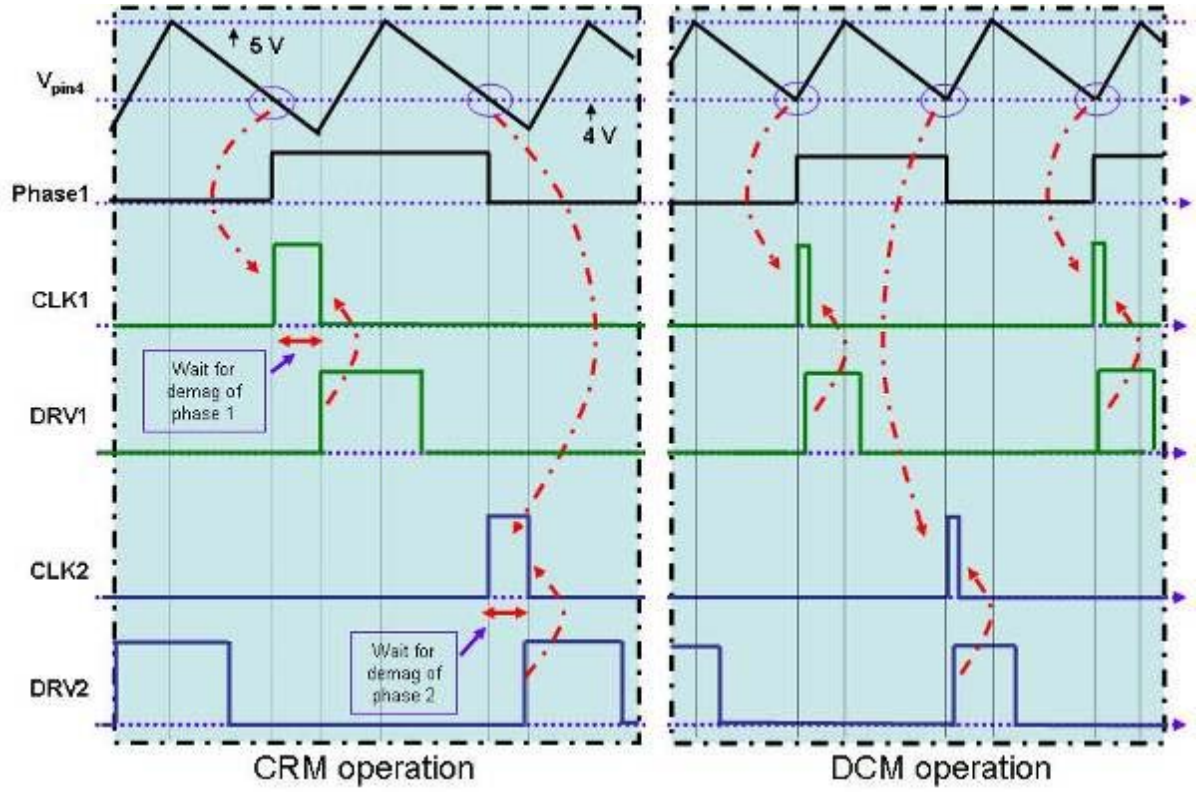


Figure 17. Typical Waveforms (T_{delay} not shown here for the sake of simplicity)

Frequency Foldback

In addition, the circuit features the frequency fold−back function to improve the light load efficiency. Practically, the oscillator charge and discharge currents ($I_{OSC(CH)}$ and $I_{OSC(DISCH)}$ of Figure 16) are not constant but dependent on the power level. More specifically, $I_{OSC(CH)}$ and $I_{OSC(DISCH)}$ linearly vary as a function of $V_{control}$ output of the regulation block that thanks to the feed−forward featured by the NCP1631, is representative of the load.

The practical implementation is portrayed by Figure 16.

"V_{REGUL}" is the signal derived from $V_{control}$ that is effectively used to modulate the MOSFET on−time. V_{REGUL} is buffered and applied to pin 6 ("Frequency fold−back" pin). A resistor R_{FF} is to be connected to pin 6 to sink a current proportional to V_{REGUL}

$$\left(I_{pin6} = I_{FF} = \frac{V_{REGUL}}{R_{FF}} \right).$$

This current is clamped not to exceed 105 μA and copied by a current mirror to form $I_{OSC(CH)}$ and $I_{OSC(DISCH)}$.

As a matter of fact, the oscillator charge current is:

$$\Rightarrow \begin{cases} I_{OSC(CH)} = I_{OSC(clamp)} + \frac{V_{REGUL}}{R_{FF}} & \text{if } \left(\frac{V_{REGUL}}{R_{FF}} \le 105\ \mu A \right) \\ I_{OSC(CH)} = I_{OSC(clamp)} + I_{OSC(CH1)} = I_{OSC(CHT1)} = 140\ \mu A & \text{otherwise} \end{cases} \quad \text{(eq. 18)}$$

The oscillator charge current is then an increasing function of V_{REGUL} and is clamped to 140 μA.

The oscillator discharge current is:

$$\Rightarrow \begin{cases} I_{OSC(DISCH)} = \frac{V_{REGUL}}{R_{FF}} & \text{if } \left(\frac{V_{REGUL}}{R_{FF}} \le 105\ \mu A \right) \\ I_{OSC(DISCH)} = I_{OSC(DISCH1)} = 105\ \mu A & \text{otherwise} \end{cases} \quad \text{(eq. 19)}$$

The oscillator discharge current is also an increasing function of V_{REGUL} and is clamped to105 μA.

As a consequence, the clamp frequency is also an increasing function of V_{REGUL} until it reaches a maximum value for (I_{FF} = 105 μA). If we consider the clamp frequency f_{OSC} computed by Equation 17 as the nominal value obtained at full load and if we name it "$f_{OSC(nom)}$":

$$\Rightarrow \begin{cases} f_{OSC} = f_{OSC(nom)} & \text{if } \left(V_{REGUL} \geq R_{FF} \cdot 105\ \mu A\right) \\ f_{OSC} = \dfrac{V_{REGUL}(R_{FF}I_{OSC(clamp)} + V_{REGUL})}{60\ \mu\ R_{FF}(R_{FF}I_{OSC(clamp)} + 2V_{REGUL})} \cdot f_{OSC(nom)} & \text{if } \left(V_{REGUL} \leq R_{FF} \cdot 105\ \mu A\right) \end{cases} \quad \text{(eq. 20)}$$

Let's illustrate this operation on an example.

V_{REGUL} is the control signal that varies between 0 and 1.66 V, (V_{REGUL} = 1.66 V) corresponding to the maximum power $(P_{in})_{HL}$ that can virtually be delivered by the PFC stage as selected by the timing resistor (for more details, you can refer to the application note AND8407).

If one decides to start to reduce the clamp frequency when the power goes below $(P_{in})_{HL}/2$, the oscillator charge current should start to decrease when V_{REGUL} is 0.83 V.

Hence, the pin 6 resistor ("R_{FF}") must be selected so that pin 6 sources 105 μA when V_{REGUL} equates 0.83 V:

$$R_{FF} = \frac{0.83\ V}{105\ \mu A} = 7.9\ k\Omega \quad \text{(eq. 21)}$$

Let's take (R_{FF} = 8.2 kΩ) which is a normalized value. This selection leads to:

$$\Rightarrow \begin{cases} f_{OSC} = f_{OSC(nom)} & \text{if } \left(V_{REGUL} \geq 8.2\ k \cdot 105\ \mu = 860\ mV\right) \\ f_{OSC} = \dfrac{V_{REGUL}(R_{FF}I_{OSC(clamp)} + V_{REGUL})}{492\ m(R_{FF}I_{OSC(clamp)} + 2V_{REGUL})} \cdot f_{OSC(nom)} & \text{if } \left(V_{REGUL} \leq 860\ mV\right) \end{cases} \quad \text{(eq. 22)}$$

For instance, if the nominal frequency ($f_{OSC(nom)}$) is 120 kHz, the following characteristic is obtained.

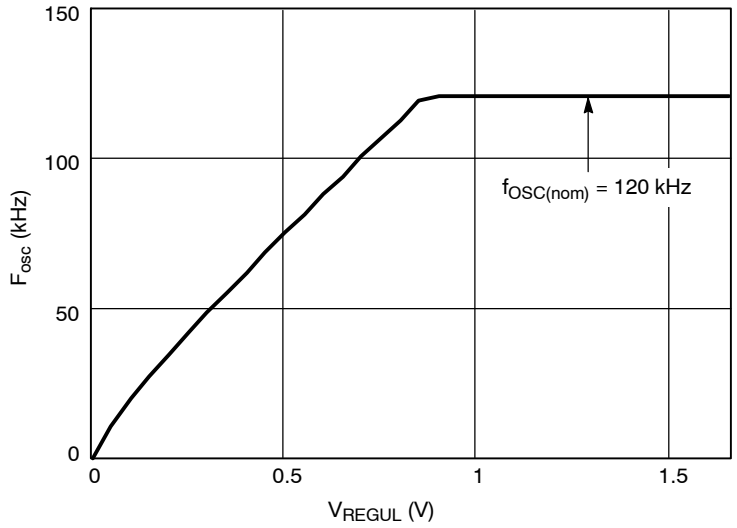


Figure 18. Fold−back Characteristic of the Clamp Frequency with R_{FF} = 8.2 kΩ and $f_{OSC(nom)}$ = 120 kHz

If pin6 is grounded (accidently or not), the circuit operates properly with a constant 140 μA oscillator charge current and a 105 μA discharge current. The clamp frequency equates its nominal value over the whole load range.

If pin6 is open, the oscillator charge current is equal to $I_{OSC(clamp)}$ but the oscillator discharge current is null and hence the PFC stage cannot operate.

A minimum discharge current and hence a minimum clamp frequency can be forced by placing a resistor between pin 4 and ground. For instance, a 1.5−MΩ resistor forces a 3.3−μA discharge current when the oscillator capacitor is fully charged and about 2.6 μA when it is near the oscillator low threshold (4 V).

A transistor pulls the pin 6 down during startup to disable the frequency fold−back function.

Skip Mode

The circuit features the frequency fold−back that leads to a very efficient stand−by mode. In order to ensure a proper regulation in no load conditions even if this feature is not used (pin 6 grounded), the circuit skips cycles when the error amplifier output is at its minimum level. The error amplifier output is maintained between about 0.6 V and 3.6 V thanks to active clamps. A skip sequence occurs as long as the 0.6 V clamp circuitry is triggered and switching operation is recovered when the clamp is inactive.

Brown−Out Protection

The brown−out pin receives a portion of the input voltage (V_{IN}). As V_{IN} is a rectified sinusoid, a capacitor must integrate the ac line ripple so that a voltage proportional to the average value of (V_{IN}) is applied to the brown−out pin.

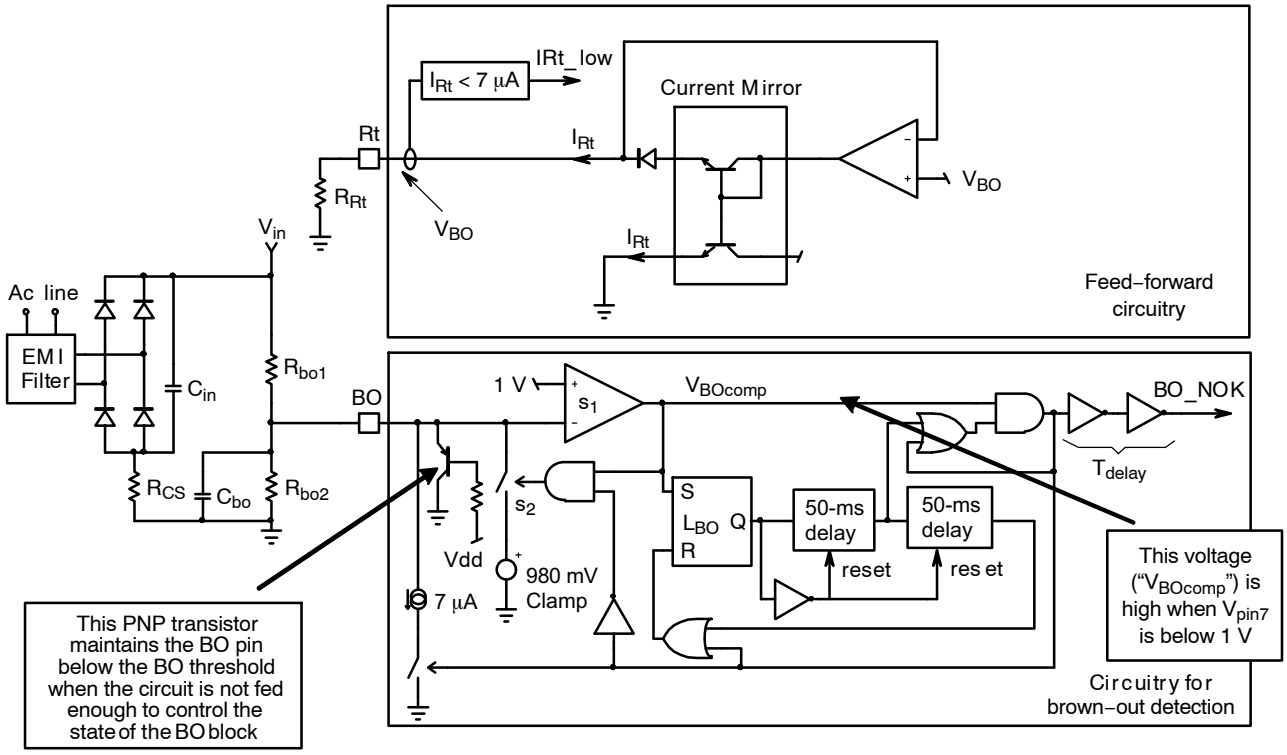


Figure 19. Brown−out Block

The main function of the BO block is to detect too low input voltage conditions. A 7−μA current source lowers the BO pin voltage when a brown−out condition is detected. This is for hysteresis purpose as required by this function.

In nominal operation, the voltage applied to pin7 must be higher than the 1 V internal voltage reference. In this case, the output of the comparator BO_Comp (V_{BOcomp}) is low (see Figure 19).

Conversely, if V_{pin7} goes below 1 V, the BO_Comp output turns high and a 965 mV voltage source is connected to the BO pin to maintain the pin level near 1 V. Then, a 50−ms blanking delay is activated during which no fault is detected. The main goal of the 50−ms lag is to help meet the hold−up requirements. In case of a short mains interruption, no fault is detected and hence, the "pfcOK" signal remains high and does not disable the downstream converter. In addition, pin7 being kept at 965 mV, there is almost no extra delay between the line recovery and the occurrence of a proper voltage applied to pin2, that otherwise would exist because of the large capacitor typically placed between pin7 and ground to filter the input voltage ripple. As a result, the NCP1631 effectively "blanks" any mains interruption that is shorter than 25 ms (minimum guaranteed value of the 50−ms timer).

At the end of this 50−ms blanking delay, another timer is activated that sets a 50−ms window during which a fault can be detected. This is the role of the second 50−ms timer of Figure 19:

- if the output of OPAMP is high at the end of the first delay (50−ms blanking time) and before the second 50−ms delay time is elapsed, a brownout condition is detected
- if the output of OPAMP remains low for the duration of the second delay, no fault is detected.

When the "BO_NOK" signal is high:

- The drivers are disabled, the "$V_{control}$" pin is grounded to recover operation with a soft−start when the fault has gone and the "pfcOK" voltage turns low to disable the downstream converter.
- The OPAMP output is separated from pin7 (Figure 19) to prevent the operational amplifier from maintaining 1 V on pin7 (as done by the switches s_1 and s_2 in the representation of Figure 19). Instead, V_{pin2} drops to the value that is externally forced (by V_{in}, R_{bo1}, R_{bo2} and C_{bo2} in Figure 19). As a consequence, the OPAMP output remains high and the "BO_NOK" signal stays high until the line recovers.

– The 7−μA current source is enabled that lowers the pin7 voltage for hysteresis purpose.

A short delay (T_{delay}) is added to get sure that these three actions are properly done before the PFC driver is disabled and the "$V_{control}$" and "pfcOK" pins are grounded.

At startup (and in UVLO situations that is when the Vcc voltage is not sufficient for operation), a pnp transistor ensures that the BO pin voltage remains below the 1 V threshold until V_{CC} reaches $V_{CC(on)}$. This is to guarantee that the circuit starts operation in the right state, that is, "BONOK" high. When V_{CC} exceeds $V_{CC(on)}$, the pnp transistor turns off and the circuit enables the 7−μA current source (I_{BO}).

Also, (I_{BO}) is enabled whenever the part is in off−mode, but at startup, I_{BO} is disabled until V_{CC} reaches $V_{CC(on)}$.

Brown−out Resistors Calculation

The BO resistors can be calculated with the following equations (for more details, refer to the application note AND8407)

$$R_{bo1} = \frac{(V_{in,avg})_{boH} - \left[(V_{in,avg})_{boL}\left[1 - \frac{\frac{f_{line}}{10}}{3f_{line}}\right]\right]}{I_{HYST}} \quad \text{(eq. 23)}$$

$$R_{bo2} = \frac{R_{bo1}}{\left(\frac{(V_{in,avg})_{boL}}{V_{BO(th)}}\left(1 - \frac{f_{BO}}{3f_{line}}\right)\right) - 1} \quad \text{(eq. 24)}$$

Feed−forward

As shown by Figure 19, The BO circuit also generates an internal current proportional to the input voltage average value (I_{Rt}). The pin7 voltage is buffered and made available on pin 3. Placing a resistor between pin 3 and ground, enables to adjust a current proportional to the average input voltage. This current (I_{Rt}) is internally copied and squared to form the charge current for the timing capacitor of each phase. Since this current is proportional to the square of the line magnitude, the conduction time is made inversely proportional to the line magnitude. This feed−forward feature makes the transfer function and the power delivery independent of the ac line level. Only the regulation output (V_{REGUL}) controls the power amount. If the I_{Rt} current is too low (below 7 μA), the controller goes in OFF mode to avoid damaging the MOSFETs with too long conduction time.

Thermal Shutdown (TSD)

An internal thermal circuitry disables the circuit gate drive and then keeps the power switch off when the junction temperature exceeds 140°C typically. The output stage is then enabled once the temperature drops below about 80°C (60°C hysteresis).

The temperature shutdown keeps active as long as the circuit is not reset, that is, as long as V_{CC} keeps higher than V_{CC}RESET. The reset action forces the TSD threshold to be the upper one (140°C). This ensures that any cold start−up will be done with the right TSD level.

Under−Voltage Lockout Section

The NCP1631 incorporates an Under−Voltage Lockout block to prevent the circuit from operating when the power supply is not high enough to ensure a proper operation. An UVLO comparator monitors the pin 12 voltage (V_{CC}) to allow the NCP1631 operation when V_{CC} exceeds 12 V typically. The comparator incorporates some hysteresis (2.0 V typically) to prevent erratic operation as the V_{CC} crosses the threshold. When V_{CC} goes below the UVLO comparator lower threshold, the circuit turns off.

The circuit off state consumption is very low: < 50 μA.

This low consumption enables to use resistors to charge the V_{CC} capacitor during the start−up without the penalty of a too high dissipation.

Output Drive Section

The circuit embeds two drivers to control the two interleaved branches. Each output stage contains a totem pole optimized to minimize the cross conduction current during high frequency operation. The gate drive is kept in a sinking mode whenever the Under−Voltage Lockout (UVLO) is active or more generally whenever the circuit is off. Its high current capability (−500 mA/+800 mA) allows it to effectively drive high gate charge power MOSFET.

Reference Section

The circuit features an accurate internal reference voltage (V_{REF}). V_{REF} is optimized to be ±2.4% accurate over the temperature range (the typical value is 2.5 V). V_{REF} is the voltage reference used for the regulation and the over−voltage protection. The circuit also incorporates a precise current reference (I_{REF}) that allows the Over−Current Limitation to feature a ±6% accuracy over the temperature range.

Fault Management and OFF Mode

The circuit detects a fault if the R_t pin is open (Figure 20). Practically, if the pin sources less than 7 μA, the "I_{Rt_Low}" signal sets a latch that turns off the circuit if its output ($R_{t(open)}$) is high. A 30−μs blanking time avoids parasitic fault detections. The latch is reset when the circuit is in UVLO state (too low V_{CC} levels for proper operation).

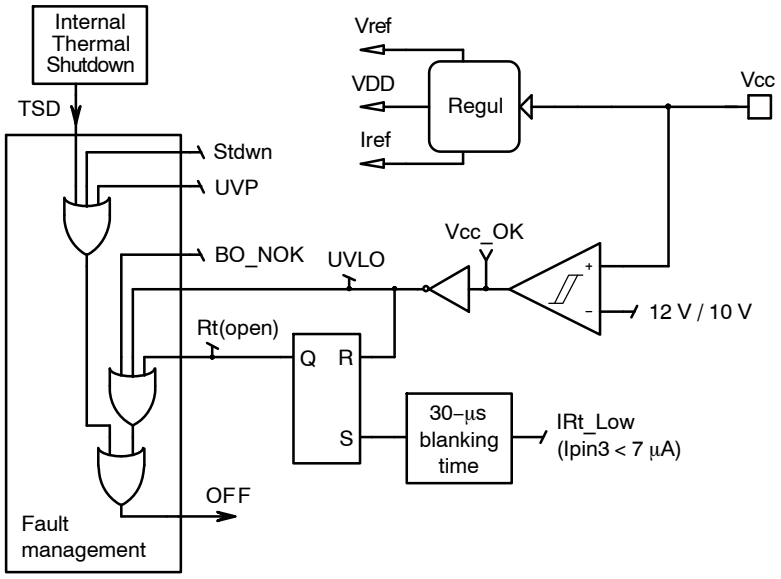


Figure 20. Fault Management Block

When any of the following faults is detected:
- brown−out (“BO_NOK”)
- Under−Voltage Protection (“UVP”)
- Latch−off condition (“Stdwn”)
- Die over−temperature (“TSD”)
- Too low current sourced by the R_t pin (“$R_{t(open)}$”)
- “UVLO” (improper Vcc level for operation)

The circuit turns off. In this mode, the controller stops operating. The major part of the circuit sleeps and its consumption is minimized (< 500 μA). More specifically, when the circuit is in OFF state:
- The two drive outputs are kept low
- The 7−μA current source of the brown−out block is enabled to set the proper start−up BO threshold if Vcc is high enough for proper operation. If not, the brown-out pin is pulled down by a pnp transistor for a proper input voltage sensing when the circuit recovers operation (see brown-out section).
- The pin5 capacitor ($V_{control}$) is discharged and kept grounded along the OFF time, to initialize it for the next operating sequence, where it must be slowly and gradually charged to offer some soft−start.
- The “pfcOK” pin is grounded.
- The output of the “V_{TON} processing block” is grounded

When the circuit recovers after a fault, the first watchdog time is around 20 μs instead of 200 μs to allow a faster re−start.

In OFF mode at startup, the consumption is very low (< 50 μA). The brown−out block is initialized not to allow operation (“BO_NOK” high) by default. The PNP clamp is active and maintains the BO pin level below 1 V. The 7−μA current source is enabled only when V_{CC} reaches $V_{CC(on)}$ threshold.

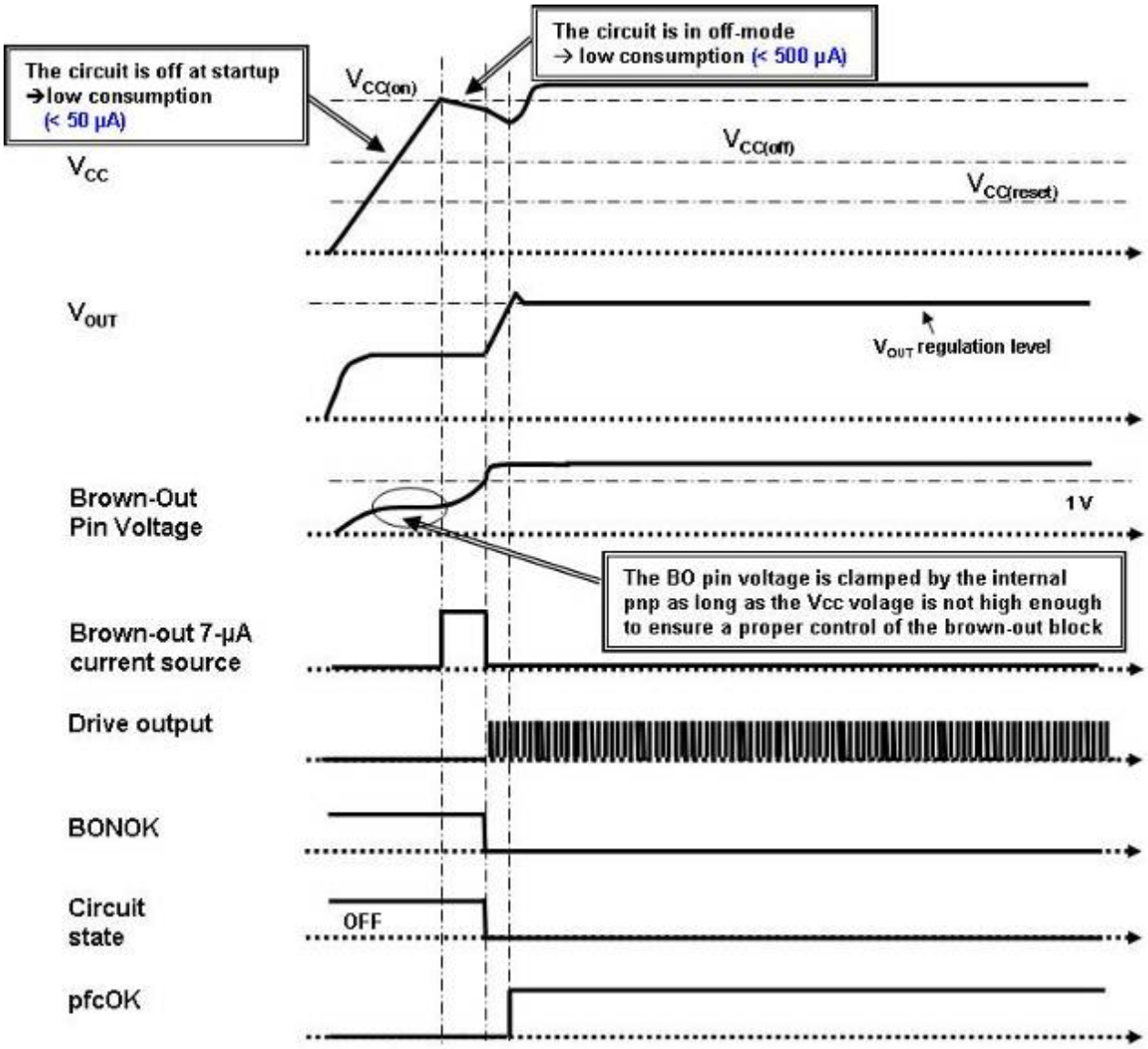
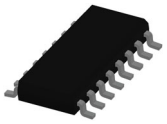


Figure 21. Start−up and Brown Out Conditions

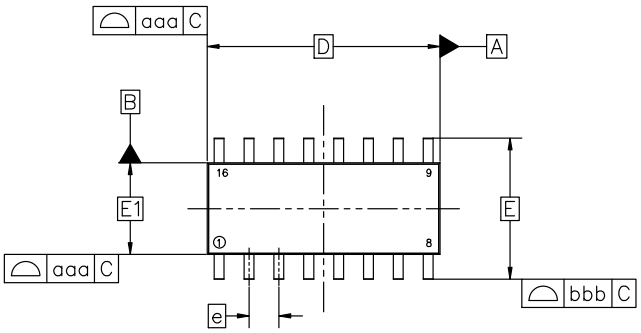
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



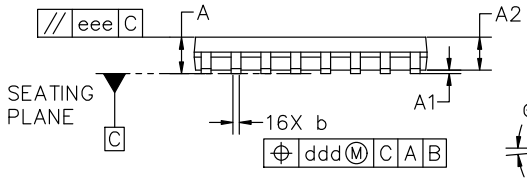
SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

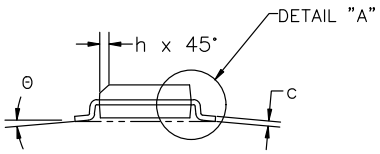
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



TOP VIEW

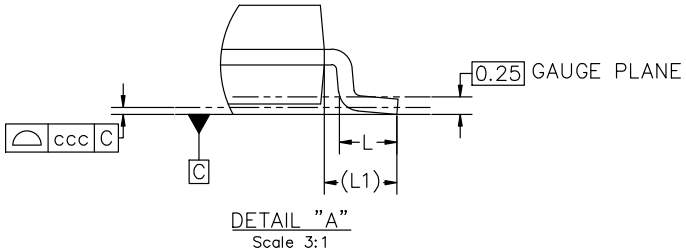


SIDE VIEW

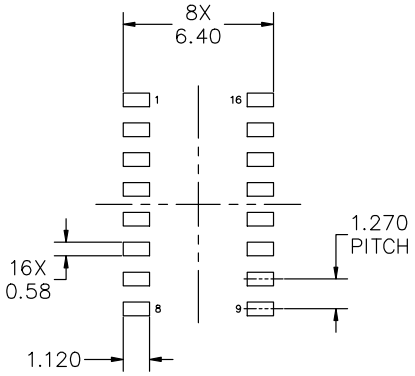


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



DETAIL "A"
Scale 3:1



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

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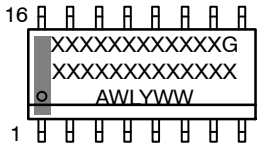
DESCRIPTION:	SOIC−16 9.90X3.90X1.50 1.27P	PAGE 1 OF 2

SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:		STYLE 2:		STYLE 3:		STYLE 4:	
PIN 1.	COLLECTOR	PIN 1.	CATHODE	PIN 1.	COLLECTOR, DYE #1	PIN 1.	COLLECTOR, DYE #1
2.	BASE	2.	ANODE	2.	BASE, #1	2.	COLLECTOR, #1
3.	EMITTER	3.	NO CONNECTION	3.	EMITTER, #1	3.	COLLECTOR, #2
4.	NO CONNECTION	4.	CATHODE	4.	COLLECTOR, #1	4.	COLLECTOR, #2
5.	EMITTER	5.	CATHODE	5.	COLLECTOR, #2	5.	COLLECTOR, #3
6.	BASE	6.	NO CONNECTION	6.	BASE, #2	6.	COLLECTOR, #3
7.	COLLECTOR	7.	ANODE	7.	EMITTER, #2	7.	COLLECTOR, #4
8.	COLLECTOR	8.	CATHODE	8.	COLLECTOR, #2	8.	COLLECTOR, #4
9.	BASE	9.	CATHODE	9.	COLLECTOR, #3	9.	BASE, #4
10.	EMITTER	10.	ANODE	10.	BASE, #3	10.	EMITTER, #4
11.	NO CONNECTION	11.	NO CONNECTION	11.	EMITTER, #3	11.	BASE, #3
12.	EMITTER	12.	CATHODE	12.	COLLECTOR, #3	12.	EMITTER, #3
13.	BASE	13.	CATHODE	13.	COLLECTOR, #4	13.	BASE, #2
14.	COLLECTOR	14.	NO CONNECTION	14.	BASE, #4	14.	EMITTER, #2
15.	EMITTER	15.	ANODE	15.	EMITTER, #4	15.	BASE, #1
16.	COLLECTOR	16.	CATHODE	16.	COLLECTOR, #4	16.	EMITTER, #1

STYLE 5:		STYLE 6:		STYLE 7:	
PIN 1.	DRAIN, DYE #1	PIN 1.	CATHODE	PIN 1.	SOURCE N-CH
2.	DRAIN, #1	2.	CATHODE	2.	COMMON DRAIN (OUTPUT)
3.	DRAIN, #2	3.	CATHODE	3.	COMMON DRAIN (OUTPUT)
4.	DRAIN, #2	4.	CATHODE	4.	GATE P-CH
5.	DRAIN, #3	5.	CATHODE	5.	COMMON DRAIN (OUTPUT)
6.	DRAIN, #3	6.	CATHODE	6.	COMMON DRAIN (OUTPUT)
7.	DRAIN, #4	7.	CATHODE	7.	COMMON DRAIN (OUTPUT)
8.	DRAIN, #4	8.	CATHODE	8.	SOURCE P-CH
9.	GATE, #4	9.	ANODE	9.	SOURCE P-CH
10.	SOURCE, #4	10.	ANODE	10.	COMMON DRAIN (OUTPUT)
11.	GATE, #3	11.	ANODE	11.	COMMON DRAIN (OUTPUT)
12.	SOURCE, #3	12.	ANODE	12.	COMMON DRAIN (OUTPUT)
13.	GATE, #2	13.	ANODE	13.	GATE N-CH
14.	SOURCE, #2	14.	ANODE	14.	COMMON DRAIN (OUTPUT)
15.	GATE, #1	15.	ANODE	15.	COMMON DRAIN (OUTPUT)
16.	SOURCE, #1	16.	ANODE	16.	SOURCE N-CH

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