NCP1578

Synchronous Step-Down Controller with 50 mA Linear Regulator

The NCP1578 is a voltage mode synchronous step−down controller for high performance systems intended to be used in battery−powered systems. The NCP1578 includes a high efficiency PWM controller with adjustable output, and a 5 V/50 mA linear regulator. A pin is provided to enable or disable forced PWM mode of operation. An internal power good voltage monitor tracks the SMPS output. NCP1578 also features soft−start sequence, UVLO for linear regulator and switcher, overvoltage protection, overcurrent protection, and thermal shutdown. The IC is packaged in QFN20.

Features

- Fixed 5.0 V/50 mA Internal Linear Regulator
- Adjustable PWM Output Voltage
- 1.5% Accuracy 0.8 V Reference
- 4.5 V to 24 V Battery/Adaptor Voltage Range
- Selectable Force PWM Mode
- Lossless, Programmable High Side MOSFET's $R_{DS(ON)}$ Current Sensing
- Soft−start and Power−Up Sequencing
- Overvoltage Protection, Undervoltage Protection
- Programmable Delay Power Good Output
- Thermal Shutdown
- Housed in QFN20
- This is a Pb−Free Device

Typical Applications

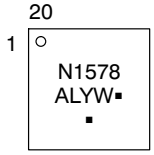
- Network HUB, Switchers and Routers
- 3−Cell and 4−Cell Li−ion Battery−Powered Devices
- Personal Computer Peripherals
- Microprocessors Power Supply
- Embedded Controller
- DSP and Core Processor
- Supply for LCD Display

ON Semiconductor®

http://onsemi.com

QFN20
MN SUFFIX
CASE 485E

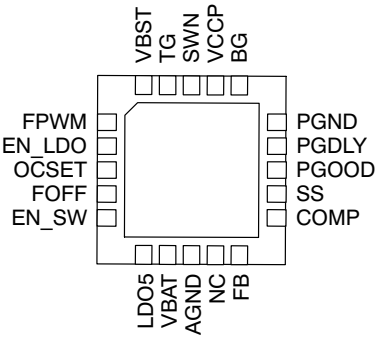
MARKING DIAGRAM



N1578	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping
NCP1578MNR2G	QFN20 (Pb−Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

DETAILED BLOCK DIAGRAM

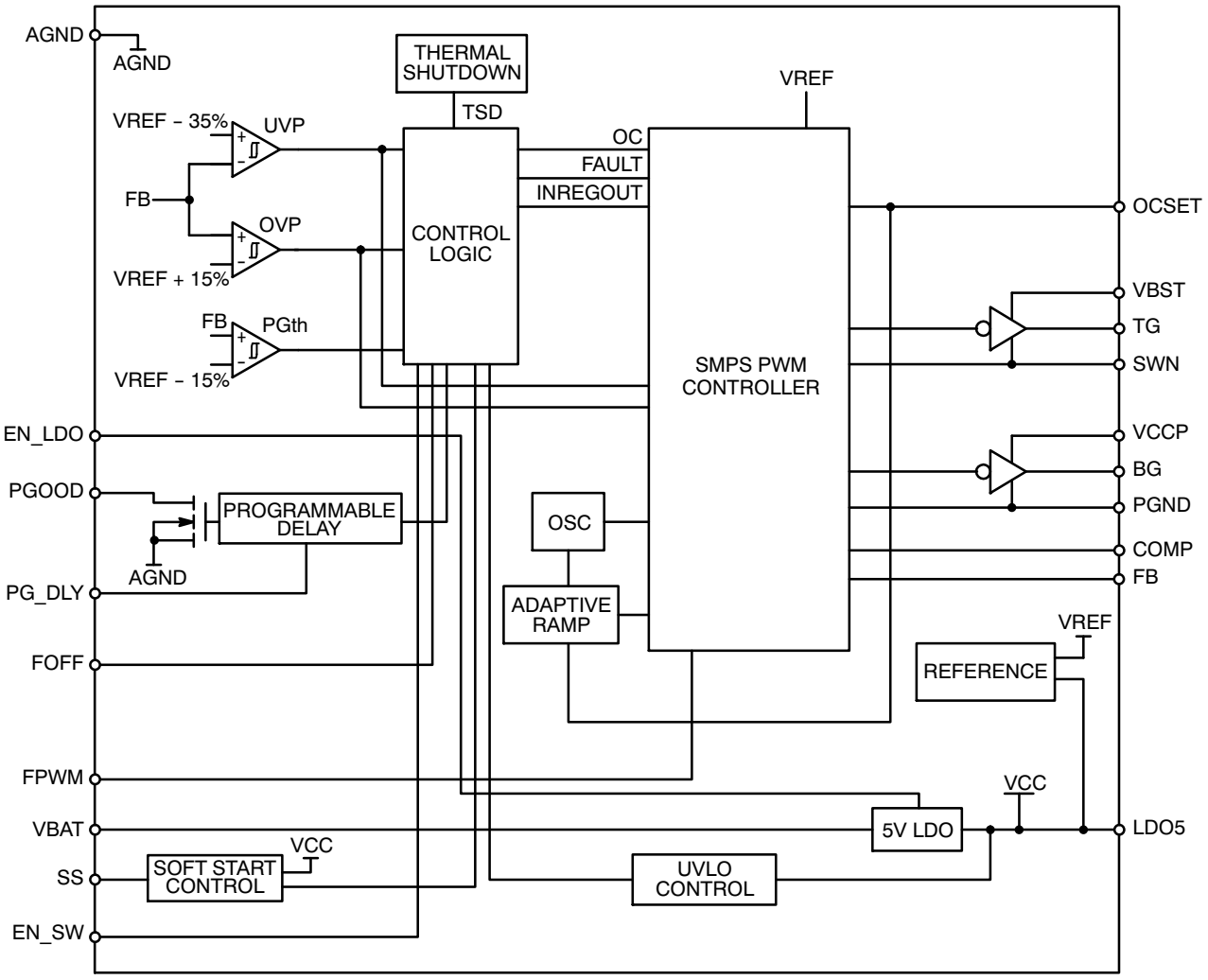


Figure 1. Detailed Block Diagram

TYPICAL APPLICATION CIRCUITS

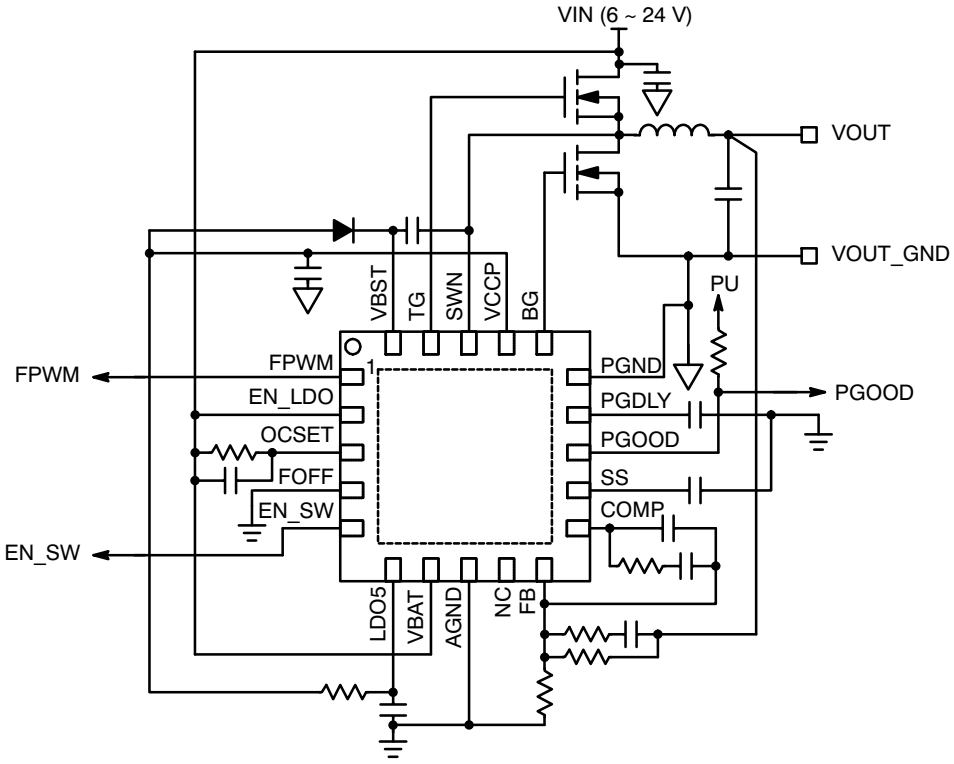


Figure 2. Single Supply VBAT Configuration

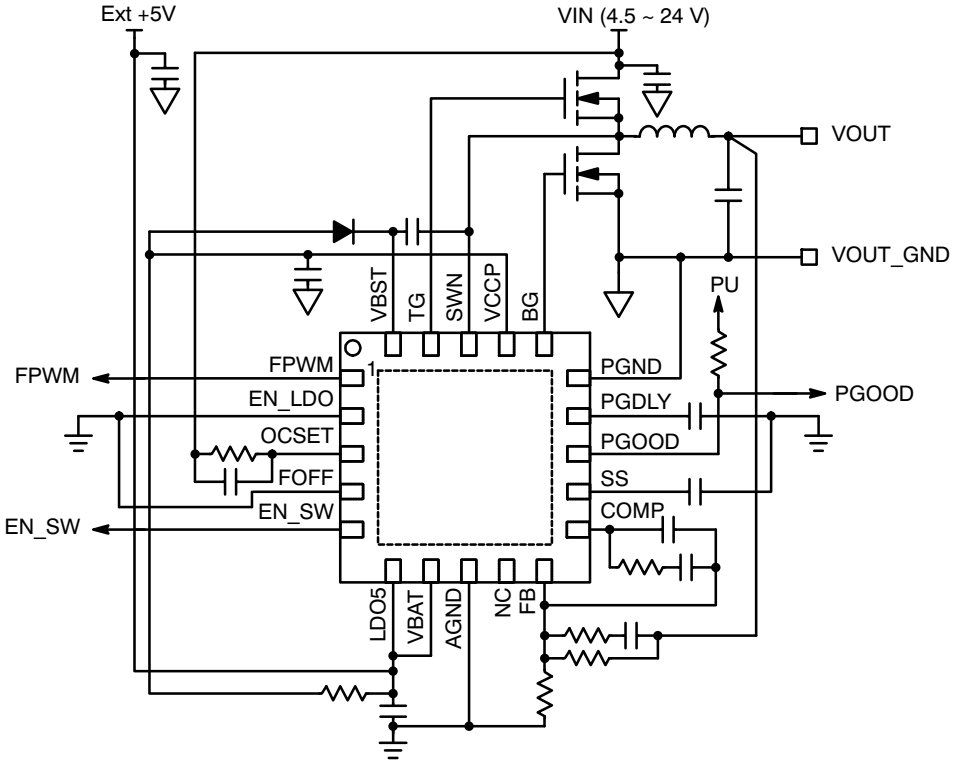


Figure 3. External 5 V and VIN Configuration

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Description
1	FPWM	FPWM or Power Saving Control. Logic high enables force PWM. Logic low enables power saving operation.
2	EN_LDO	LDO enable input. The 5 V LDO is enabled if EN_LDO is high and disabled if it is low. This pin can sustain voltage as high as VBAT.
3	OCSET	Input pin for over current threshold setting for high side gate driver. Also it is for the internal ramp generator to implement the voltage feed forward rejection to the input voltage variation
4	FOFF	Fault OFF. If it pulls to high, it disables the features of OCP, UVLO and OVP. Normally it should be tied to ground. This pin is internally pulled down.
5	EN_SW	PWM controller's enable input. The switching controller is enabled if EN_SW is high and disabled if EN is low.
6	LDO5	5.0 V linear regulator output.
7	VBAT	Battery/adaptor voltage input.
8	AGND	Analog ground.
9	NC	Not connected
10	FB	Feedback input from controller's output voltage.
11	COMP	Error amplifier output pin.
12	SS	Soft−start (for switcher) capacitor connection to ground.
13	PGOOD	Power good signal open drain output. High impedance (open drain) if power is good (in regulation). Low impedance if power is not good.
14	PGDLY	Power good delay capacitor connection to ground.
15	PGND	Power ground.
16	BG	Gate driver output for low−side N−Channel power FET.
17	VCCP	Power Input voltage pin.
18	SWN	Inductor driven node of the SMPS, the return for high−side gate driver, and also serve as the lower supply rail of the high−side gate driver of the SMPS.
19	TG	Gate driver output for high−side N−Channel power FET.
20	VBST	Positive supply of high−side gate driver of the SMPS. Connect boost capacitor between this pin and switching node SWN of the SMPS.
21	THPAD	Copper pad on bottom of IC used for heatsinking. This pin should be connected to the ground plane under the IC.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage to AGND (V_{CC} internally connects to LDO5)	V_{LDO5}	−0.3, 6.0	V
High−side Gate Drive Supply: BST to SWN High−side FET Gate Drive Voltage: TG to SWN	V_{BST}−V_{SWN}, V_{TG}−V_{SWN}	−0.3, 6.0	V
Input / Output Pins (except EN_LDO and OCSET) to AGND	V_{IO}	−0.3, 6.0	V
VBAT Input to AGND	V_{VBAT}	−0.3, 27	V
EN_LDO Input to AGND OCSET Input to AGND	V_{EN_LDO} V_{OCSET}	−0.3, 27	V
Switch Node SWN	V_{SWN}	−4 (< 100 ns), −0.3 (dc), 32	V
PGND	V_{GND}	−0.3, 0.3	V
Thermal Characteristics QFN20 Plastic Package Thermal Resistance Junction−to−Ambient	$R_{\theta JA}$	47	°C/W
Operating Junction Temperature Range	T_J	−40 to +150	°C
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Moisture Sensitivity Level	MSL	1	−

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device is ESD sensitive. Use standard ESD precautions when handling
   This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ≤ 2.0 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ≤ 200 V per JEDEC standard: JESD22−A115 for all pins.
2. Latch−up Current Maximum Rating: ≤ 150 mA per JEDEC standard: JESD78.

ELECTRICAL CHARACTERISTICS

(V_{BAT} = 12 V, LDO5 = V_{CCP} = 5 V, T_A = −40 to 85°C, for min/max values unless otherwise noted. Typical values are at T_A = 25°C.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
SUPPLY SECTION						
Input Voltage	V_{BAT}	Single Supply Configuration, See Figure 2 Ext +5 V and V_{IN} Configuration, See Figure 3	6.0 4.5	–	24	V
VBAT Operating Supply Current	I_{BAT}	LDO5 & SMPS are Enabled, See Figure 2 TG and BG are 3 nF Capacitor Load V_{BAT} = 12 V	–	2	3	mA
		V_{BAT} = LDO5 See Figure 3 TG and BG are 3 nF Capacitor Load V_{BAT} = 5 V	–	–	3	mA
VBAT Shutdown Current	I_{BATSD}	V_{BAT} = 6 V to 24 V, EN_LDO = 0 V, EN_SW = 0 V	–	10	30	μA
UNDERVOLTAGE MONITOR						
LDO5 UVLO Lower Threshold	VLDO5UV−	Falling Edge	–	4.1	–	V
LDO5 Undervoltage Lockout Hysteresis	VLDO5UVHYS		–	330	–	mV
LINEAR REGULATOR						
LDO5 Input Voltage Range	LDO5_IN	V_{BAT} = LDO5 for 5 V Configuration See Figure 3	4.5	5.0	5.5	V
LDO5 Output Voltage	LDO5	V_{BAT} = 6 V to 24 V, EN_LDO > 1.4 V, I_{LDO5} = 0 to 50 mA	4.85	5.0	5.15	V
LDO5 Maximum Output Current	I_{LDO5_MAX}	V_{BAT} = 6 V to 24 V, EN_LDO > 1.4 V	50	–	–	mA
SMPS CONTROLLERS						
FB Feedback Voltage, Control Loop in Regulation	V_{FB}	T_A = 25°C T_A = −40 to 85°C	0.792 0.788	0.8 0.8	0.808 0.812	V
Operating Frequency	F_{SW}		270	300	330	kHz
Ramp Amplitude	V_{RAMP}	VOCSET = 12 V (Note 3)	–	1.02	–	V
Ramp Amplitude to VIN Ratio	ΔVRAMP/ΔVIN	VOCSET = 4.5 V to 24 V (Note 3)	–	83	–	mV/V
Minimum Duty Cycle	D_{min}		–	–	0	%
Maximum Duty Cycle	D_{max}	VOCSET = 4.5 V to 24 V	90	–	–	%
Voltage Error Amplifier DC Gain	Gain	(Note 3)	–	70	–	dB
Error Amplifier Unity Gain Bandwidth	Ft	COMP to GND = 100 pF, 1.0 Ω in Series (Note 3)	–	2	–	MHz
Voltage Error Amplifier Slew Rate	SR	(Note 3)	–	3.0	–	V/is
OCSET Pin Current Sink	I_{OC}	OCSET = 4.0 V	34	40	50	μA
OCSET Pin Current Sink Temperature Coefficient	TC_{IOC}			3200		ppm/°C
TG Gate Driver Pull−High Resistance	R_{H_TG}	V_{BST} − V_{SWN} = 5 V, V_{TG} − V_{SWN} = 4 V	–	1.5	4.0	Ω
TG Gate Driver Pull−Low Resistance	R_{L_TG}	V_{BST} − V_{SWN} = 5 V, V_{TG} − V_{SWN} = 1 V	–	1.5	4.0	Ω
BG Gate Driver Pull−High Resistance	R_{H_BG}	V_{CCP} = 5 V, V_{BG} = 4 V	–	1.5	4.0	Ω
BG Gate Driver Pull−Low Resistance	R_{L_BG}	V_{CCP} = 5 V, V_{BG} = 1 V	–	0.9	3.0	Ω
Soft−start Current	I_{ss}	EN_SW = 5.0 V; Vss = 0 V	2.8	4.0	5.2	μA
PGDLY Delay Current	I_{PG_DLY}	EN_SW = 5.0 V, V_{PG_DLY} = 0 V	1.4	2.0	2.6	μA
PGDLY Threshold	Vth_{PG_DLY}		–	1.25	–	V

3. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS

(V_{BAT} = 12 V, LDO5 = V_{CCP} = 5 V, T_A = −40 to 85°C, for min/max values unless otherwise noted. Typical values are at T_A = 25°C.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
FAULT DETECTION						
Overvoltage Trip Threshold	OVPth	With Respect to FB Voltage	110	–	120	%
Undervoltage Trip Threshold	UVPth	With Respect to FB Voltage		65	–	%
PGOOD Lower Threshold	VPG–	With Respect to FB Voltage	–20	–	–10	%
PGOOD Pin ON Resistance	PGOOD_R	I_PGOOD = 5.0 mA	–	70	–	Ω
PGOOD Pin Leakage Current	PGOOD_LK		–	–	1.0	μA
Thermal Shutdown Trip Point	T_{SD}	(Note 3)	–	150	–	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	(Note 3)	–	25	–	°C
LOGIC INPUT LEAKAGE						
EN_LDO Threshold High	V_{ENLDO_H}	LDO ON	1.4	–	–	V
EN_LDO Threshold Low	V_{ENLDO_L}	LDO OFF	–	–	0.5	V
EN_LDO Input Current	I_{INLDO_EN1}	EN_LDO = 5.0 V	–	–	1	μA
	I_{INLDO_EN2}	EN_LDO = 24.0 V	–	–	10	μA
EN_SW Threshold High	V_{ENSW_H}	SMPS ON	1.4	–	–	V
EN_SW Threshold Low	V_{ENSW_L}	SMPS OFF	–	–	0.6	V
EN_SW Input Current	I_{INSW_EN}	EN_SW = 5.0 V	–	–	1.0	μA
FPWM Threshold High	FPWM_H	Set as Force PWM Mode	1.4	–	–	V
FPWM Threshold Low	FPWM_L	Set as Power Saving Mode	–	–	0.6	V
FPWM Input Current	I_{IN_FPWM}	FPWM = 5.0 V	–	–	1.0	μA
FOFF Threshold High	FOFF_H	Disable OCP, UVLO & OVP	1.4	–	–	V
FOFF Threshold Low	FOFF_L	OCP, UVLO & OVP are in function	–	–	0.6	V
FOFF Input Current	I_{IN_FOFF}	FOFF = 5.0 V (Internal Pull Down by 1 MΩ)	–	5.0	–	μA

3. Guaranteed by design, not tested in production.

TYPICAL OPERATING CHARACTERISTICS

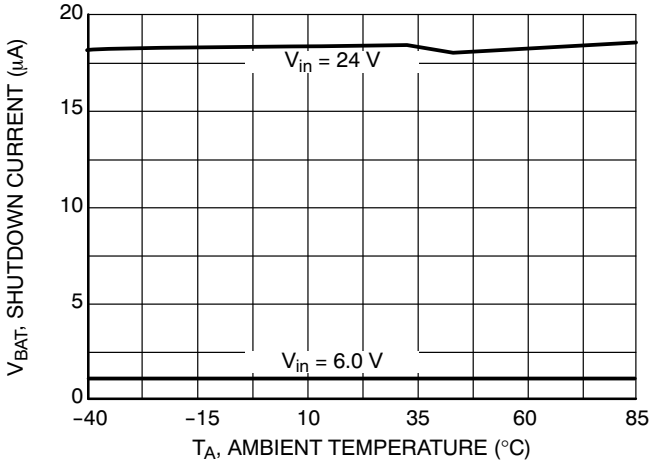


Figure 4. V_{BAT} Shutdown Current vs. Ambient Temperature

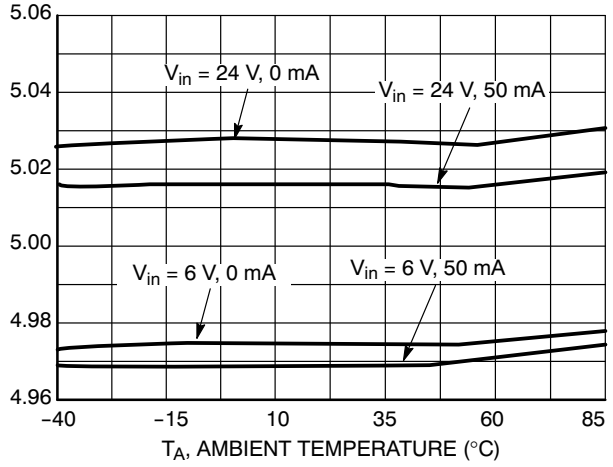


Figure 5. LDO5 Output Voltage vs. Ambient Temperature

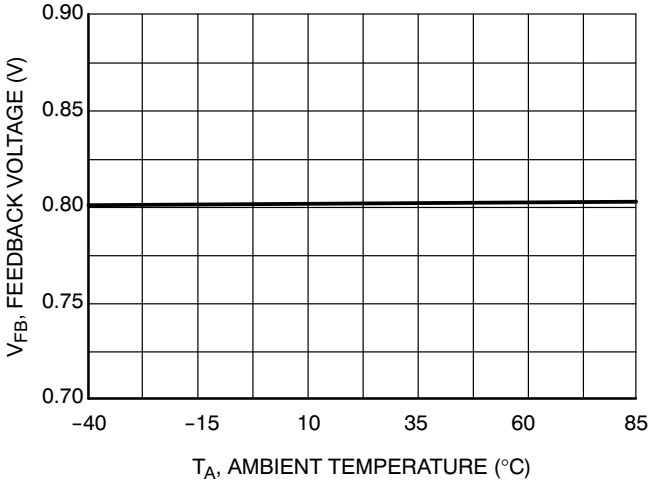


Figure 6. V_{FB} Feed Back Voltage vs. Ambient Temperature

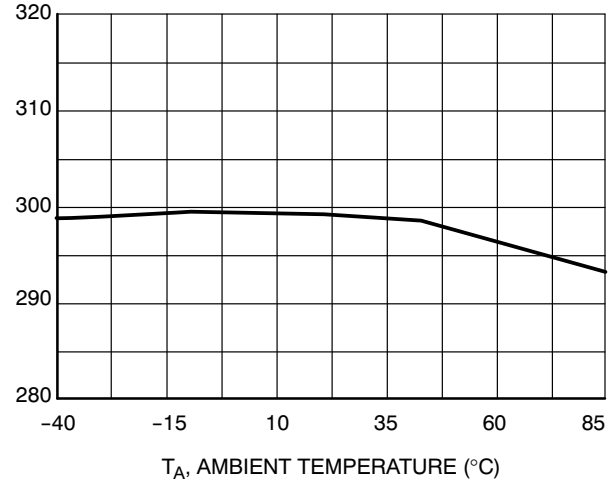


Figure 7. Switching Frequency vs. Ambient Temperature

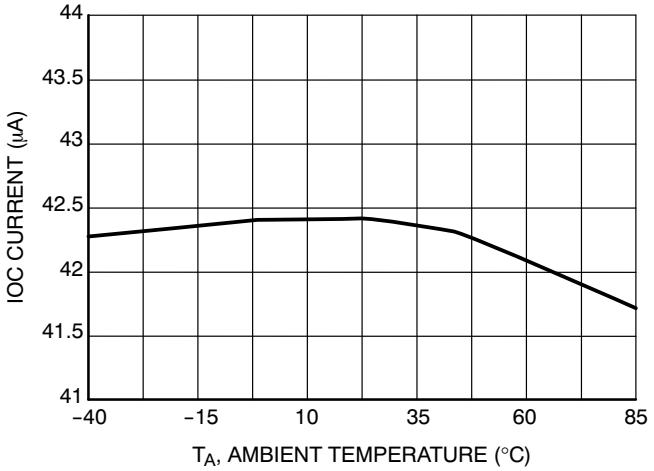


Figure 8. IOC Current vs Ambient Temperature

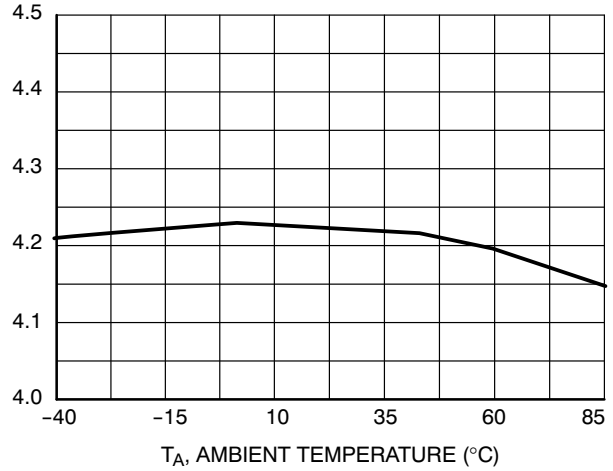


Figure 9. Soft−Start Current vs. Ambient Temperature

TYPICAL OPERATING CHARACTERISTICS

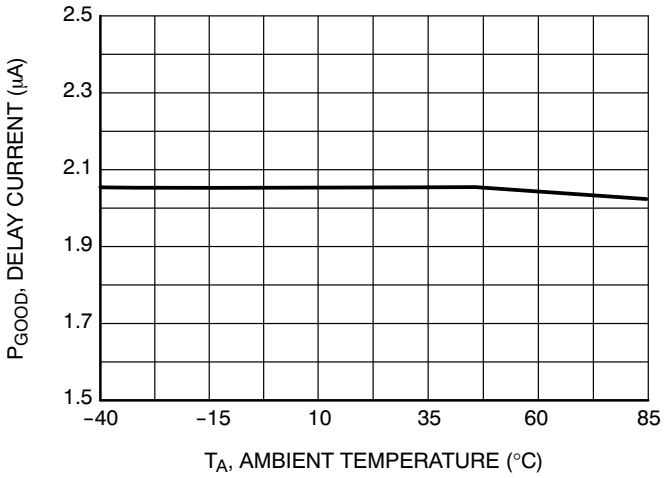


Figure 10. P_{GOOD} Delay Current vs. Ambient Temperature

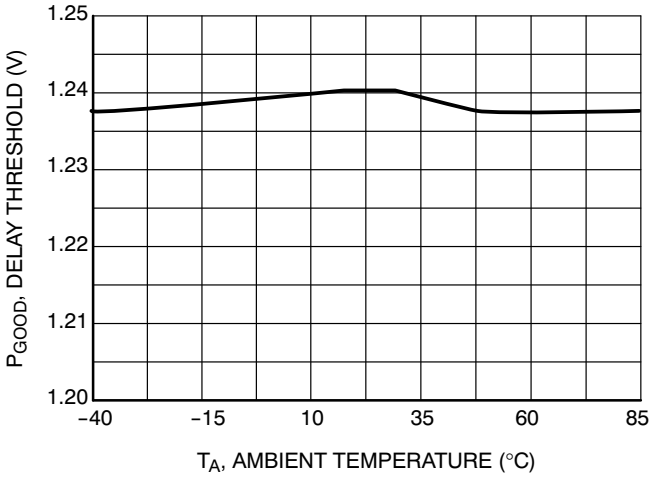


Figure 11. P_{GOOD} Delay Threshold vs. Ambient Temperature

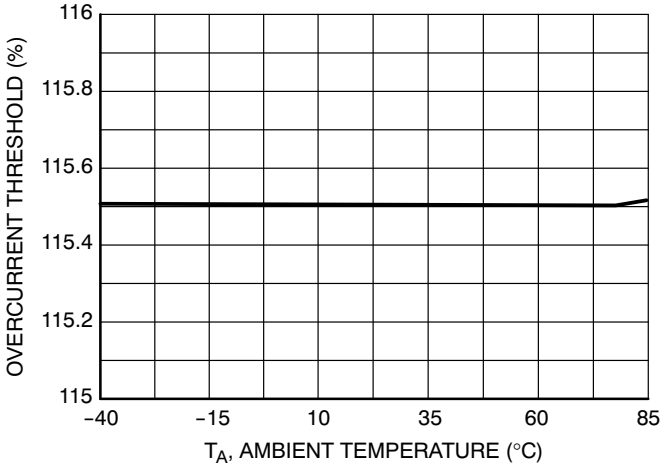


Figure 12. Overcurrent Threshold vs. Ambient Temperature

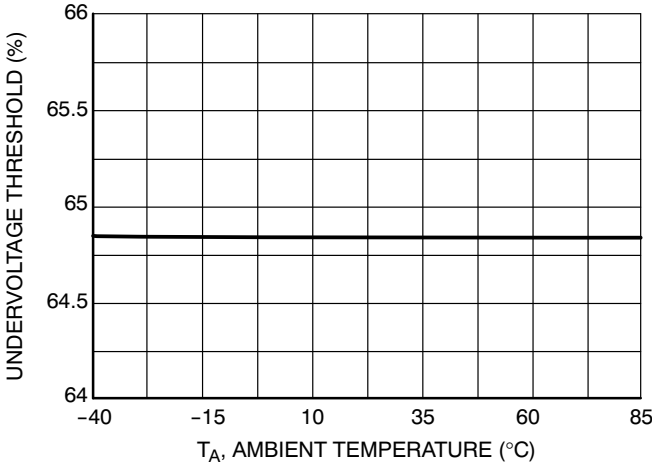


Figure 13. Undervoltage Threshold vs. Ambient Temperature

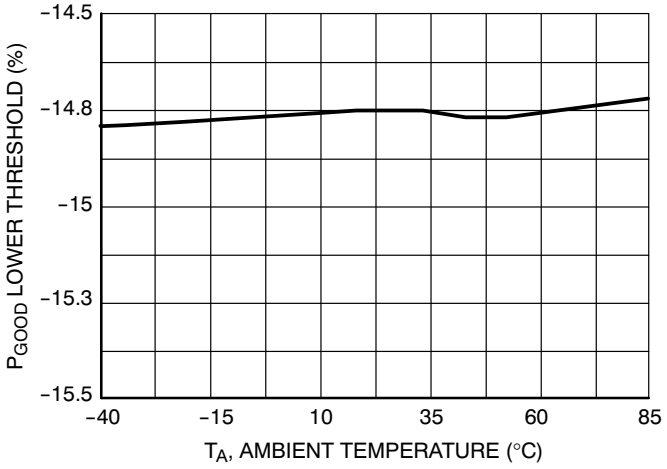


Figure 14. P_{GOOD} Lower Threshold vs. Ambient Temperature

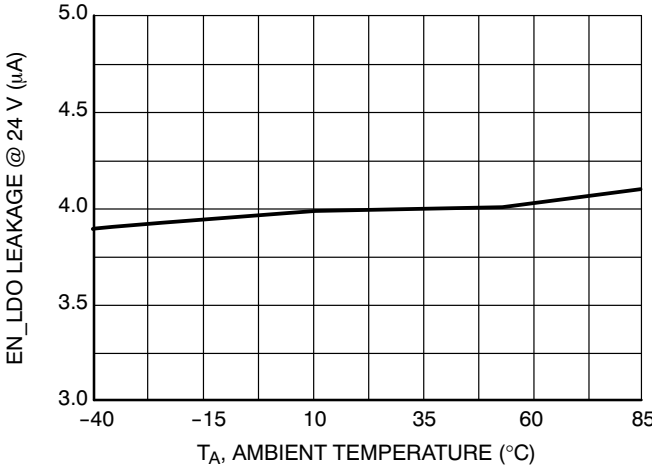


Figure 15. EN_LDO Leakage Current vs. Ambient Temperature

TYPICAL OPERATING CHARACTERISTICS

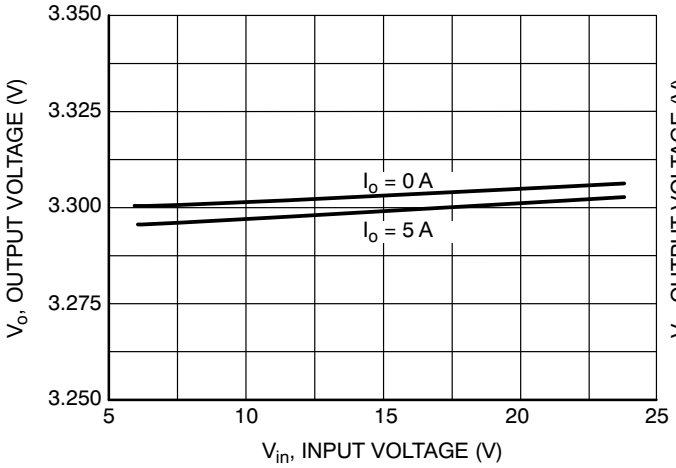


Figure 16. V_o Output Voltage vs. Input Voltage

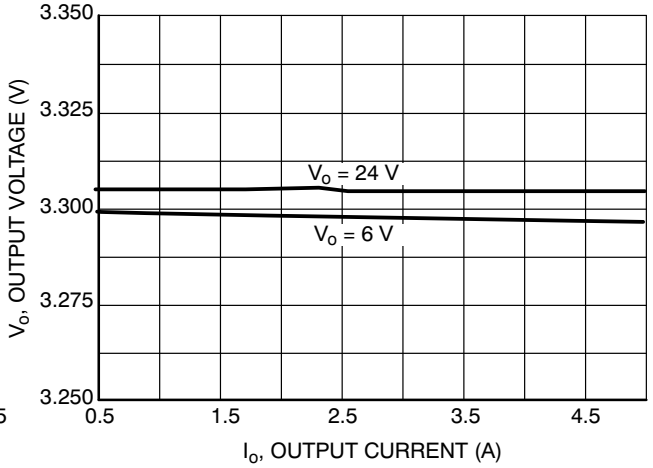


Figure 17. V_o Output Voltage vs. Output Current

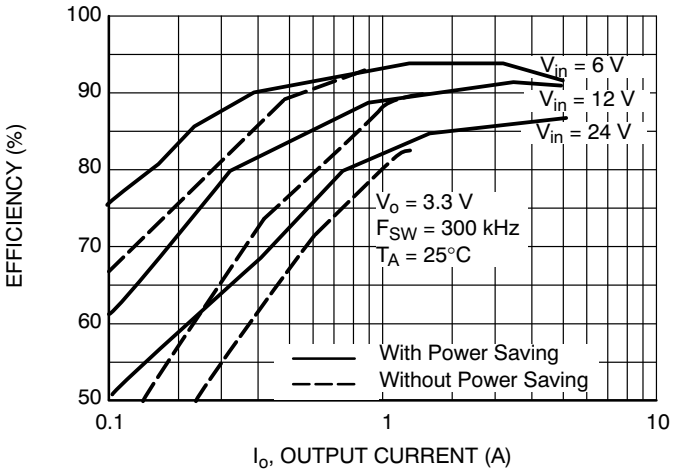


Figure 18. V_o Efficiency vs. Output Current (Single Supply)

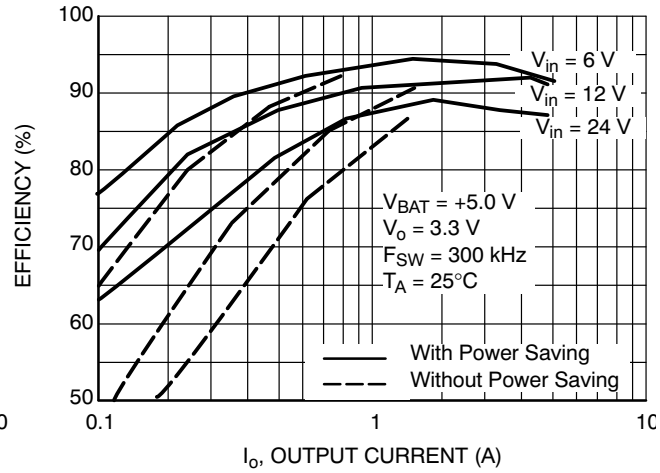


Figure 19. V_o Efficiency vs. Output Current (Separate Supply)

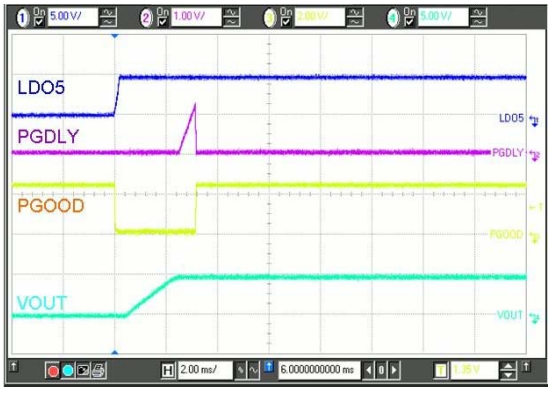


Figure 20. Power Up Sequence

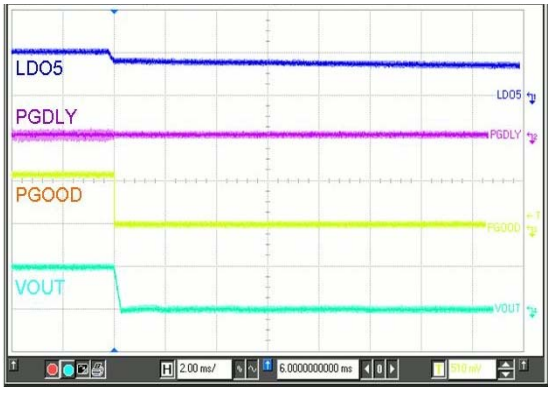


Figure 21. Power Down Sequence

TYPICAL OPERATING CHARACTERISTICS

Figure 22. Switcher Operation – CCM Mode

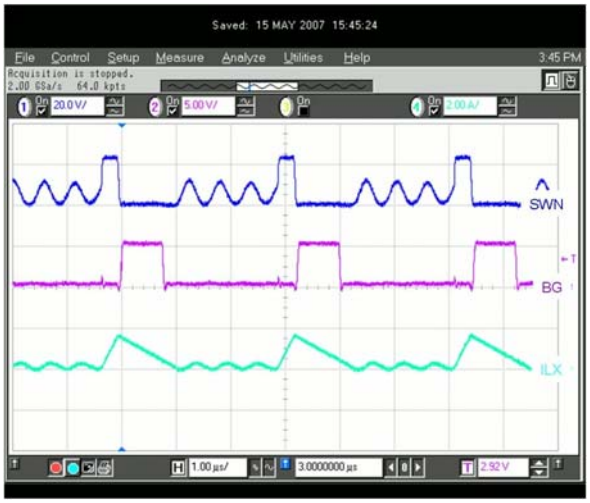


Figure 23. Switcher Operation – DCM Mode

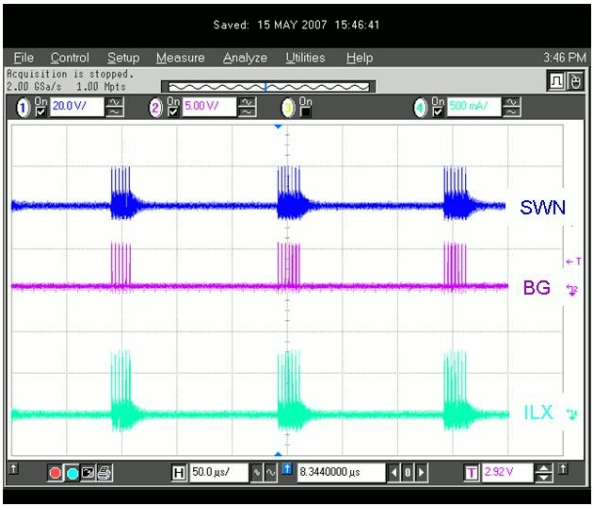


Figure 24. Switcher Operation – Pulse SkippingMode (PSM)

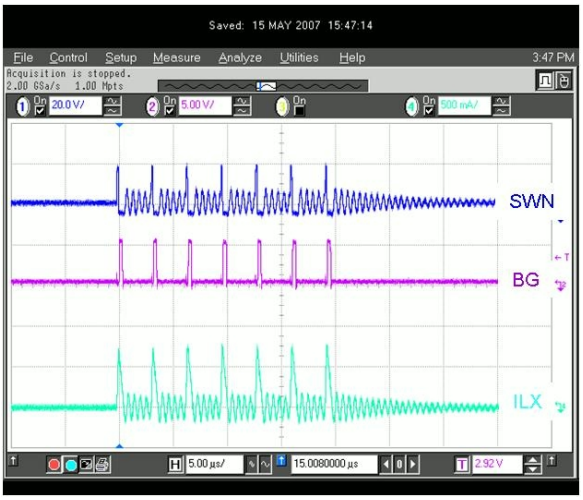


Figure 25. Switcher Operation – PSM Zoom–In

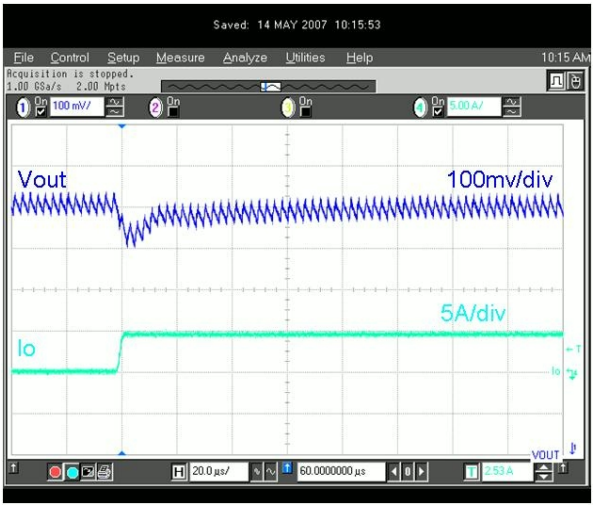


Figure 26. Load Transient – Load Step Up

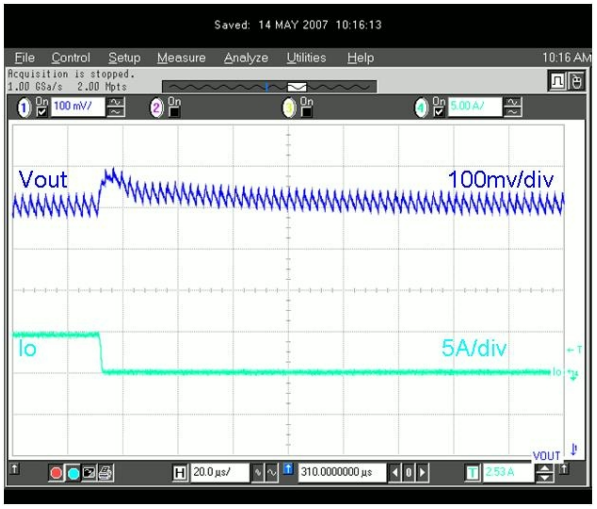


Figure 27. Load Transient – Load Release

TYPICAL OPERATING CHARACTERISTICS

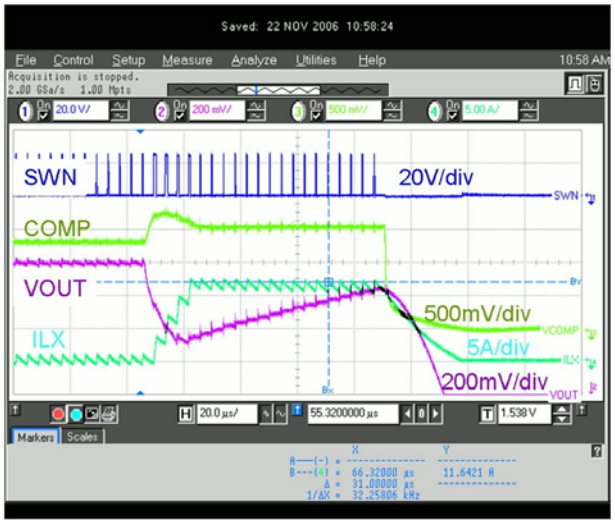


Figure 28. V_{out} OCP by Short Circuit to Ground

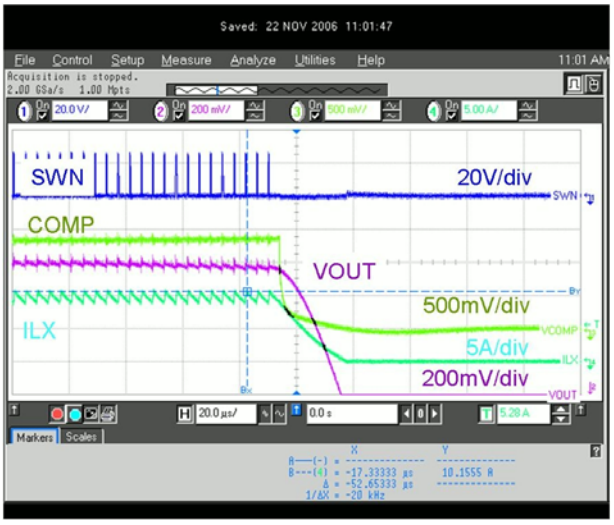


Figure 29. V_{out} OCP by Steady I_{out} Increases

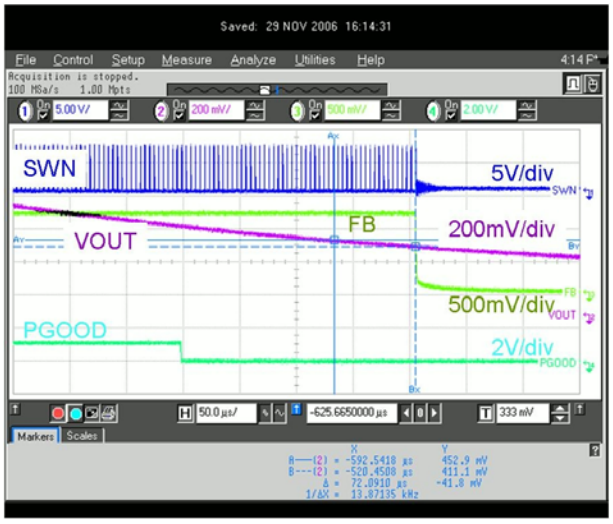


Figure 30. Undervoltage Protection

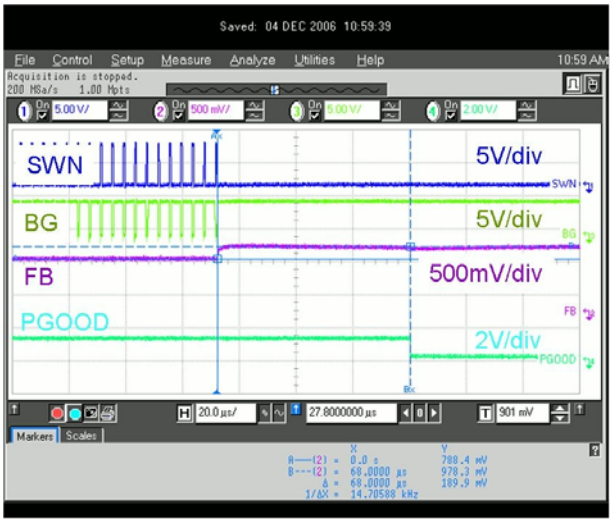


Figure 31. Overvoltage Protection

DETAILED OPERATING DESCRIPTION

General

The NCP1578 synchronous step−down power controller contains a PWM controller and a 5 V/50 mA linear regulator for wide battery/adaptor voltage range applications

The NCP1578 includes power good voltage monitor, soft−start, over current protection, undervoltage protection, overvoltage protection, LDO5 UVLO and thermal shutdown. The NCP1578 allows for improved efficiency at light loads by allowing the synchronous MOSFET to turn off automatically making this device a ideal for battery operated systems. The IC is packaged in QFN20.

Control Logic

The LDO5 is enabled when EN_LDO is high. The PWM controller is enabled when EN_SW is high. The internal V_{ref} is activated whenever the output of LDO5 rises above the UVLO threshold of 65% of V_{FB} volts, power−on reset occurs which resets all the protection faults. The device's control logic is powered by LDO5 internally. Once V_{ref} reaches its regulation voltage, an internal signal will wake up the supply undervoltage monitor which will assert a "GOOD" condition if LDO5 voltage is within certain preset levels.

Linear Regulator

The 5 V linear regulator can supply total 50 mA current for both internal and external loads. It can be enabled or disabled independently by the control pin EN_LDO. When EN_LDO = 1, the UVLO voltage is set as 4.5 V with hystersis 330 mV typical. It is recommended to bypass LDO5 output with 1 μF (min) ceramic capacitors.

Switching Controller

The controller directly drives two external N−Channel power FETs. An external resistor divider sets the nominal output voltage. The control architecture is voltage mode fixed frequency with input voltage feedforward PWM. The part is compensated externally. The switching frequency is fixed at 300 kHz ± 10%. The SMPS output voltage is divided down via resistor network and fed back to the inverting input of an internal error amplifier through FB pin to close the loop at V_{out}. This amplifier compares the feedback voltage with an internal V_{ref} to generate an error signal for the PWM comparator. This error signal is further compared with a fixed frequency RAMP waveform derived from the internal oscillator to generate a pulse−width−modulated signal. This PWM signal drives the external N−Channel Power FETs via the TG and BG pins. External inductor and capacitor filter the output waveform. The SMPS output voltage ramps up at a pre−defined soft−start rate when the EN_SW pin goes HIGH from LOW after V_{ref} is ready.

Input voltage feedforward is implemented to the RAMP signal generation to reject the effect of wide input voltage variation. With input voltage feedforward, the amplitude of the RAMP is proportional to the input voltage.

For enhanced efficiency, an active synchronous switch is used to eliminate the conduction loss contributed by the forward voltage of a Schottky diode rectifier. Adaptive nonoverlap timing control of the complementary gate drive output signals is provided to reduce large shoot−through current that degrades efficiency.

When the forced PWM is disabled, the low−side MOSFET is allowed to turn off after the detection of negative inductor current.

Overcurrent Protection of SMPS Controllers

An external resistor connected between the input voltage and OCSET sets the current limit for the high−side switch. An internal 40 μA current sink (IOC) at OCSET pin establishes a voltage drop across this resistor and develops a voltage at input and is compared to the voltage at SWN pin when the high−side gate drive is high after a fixed period of blanking time (~150 ns) to avoid false current limit triggering. When the voltage at SWN is lower than that at the input for 16 consecutive internal clock cycles, an over current condition occurs. Those 16 consecutive cycles will be operating as cycle by cycle condition in the way such that for each cycle, TG is OFF once the inductor current hits the preset threshold value. The SMPS output will be latched off after those 16 cycles to protect against a short−to−ground condition on SWN or OUT. The IC will be reset once LDO5 or EN_SW is cycled.

Output Voltages Sensing

The SMPS output voltage is sensed across the FB and AGND pins. FB should be connected through a feedback resistor divider to the output voltage point of regulation. The AGND should be connected directly through a sense trace to the remote ground sense point which is usually the ground of local bypass capacitor for load.

Supply Voltage Under−Voltage Monitor

The IC continuously monitors LDO5 output pin. The IC will shutdown if the voltage is below 4.5 V.

Thermal Shutdown

The IC will shutdown if the die temperature exceeds 150°C. The IC restarts operation only after the junction temperature drops below 125°C.

Power Good

The PGOOD is an open−drain output of a comparator which continuously monitors SMPS output voltage. The Power Good time delay can be programmable by connecting an external capacitor. The PGOOD is true (high impedance) when the FB pin is within ±15% of the preset nominal regulation voltage. The PGOOD is false (pulled low) when FB rises above 15% or falls below 15% the nominal regulation point. PGOOD pin also pulls low when protection fault occurs (OVP, UVP, OTP, and UVLO), or

SMPS is disabled by EN_SW. Note that the PGOOD pin is valid providing LDO5 is high enough to maintain the internal logic state.

Overvoltage Protection

When SMPS output voltage is above 115% (typ) the preset nominal regulation voltage for 16 consecutive internal clock cycles, the SMPS output will be latch off and it can be restarted by toggling EN_SW or LDO5.

Undervoltage Protection

When SMPS output falls below 65% (typ) of the nominal regulation voltage for 16 consecutive internal clock cycles, the undervoltage fault is set, the SMPS is latched off. Cycling EN_SW or LDO5 can reset the undervoltage fault latch and restart the controller.

Soft−Start

The switcher V_{OUT} soft−start feature is incorporated in the device to prevent surge current from power supply and output voltage overshot during power up. When EN_SW, LDO5 rises above their respective upper threshold voltages, the external soft start capacitor C_{ss} is charged by a constant current source I_{ss}. When the soft−start voltage reaches the V_{ref} voltage, the soft start process is finished. The soft−start time Tss can be programmed by the soft−start capacitor according to the following equation: $T_{ss} \approx (0.8 \times C_{ss}) / I_{ss}$.

OPERATION TABLE 1 (Single Supply V_{BAT} Configuration)

Input Condition			Operating Condition		Output Condition
FPWM	**EN_LDO**	**EN_SW**	**SMPS**	**LDO5**	**PGOOD**
X	Low	X	Off	Off	H−Z
X	High	Low	Off	On	Low
High	High	High	On (FPWM)	On	H−Z
Low	High	High	On (DCM or Pulse Skipping)	On	H−Z

OPERATION TABLE 2 (External +5 V and V_{IN} Configuration (Note 4))

Input Condition			Operating Condition	Output Condition
FPWM	**EN_LDO** (Note 5)	**EN_SW**	**SMPS**	**PGOOD**
X	Low	Low	Off	Low
High	Low	High	On (FPWM)	H−Z
Low	Low	High	On (DCM or pulse skipping)	H−Z

4. External +5 V is connecting to V_{BAT} and LDO5 pin.
5. For this configuration, it is recommended to pull EN_LDO to GND at any time.

TIMING DIAGRAMS

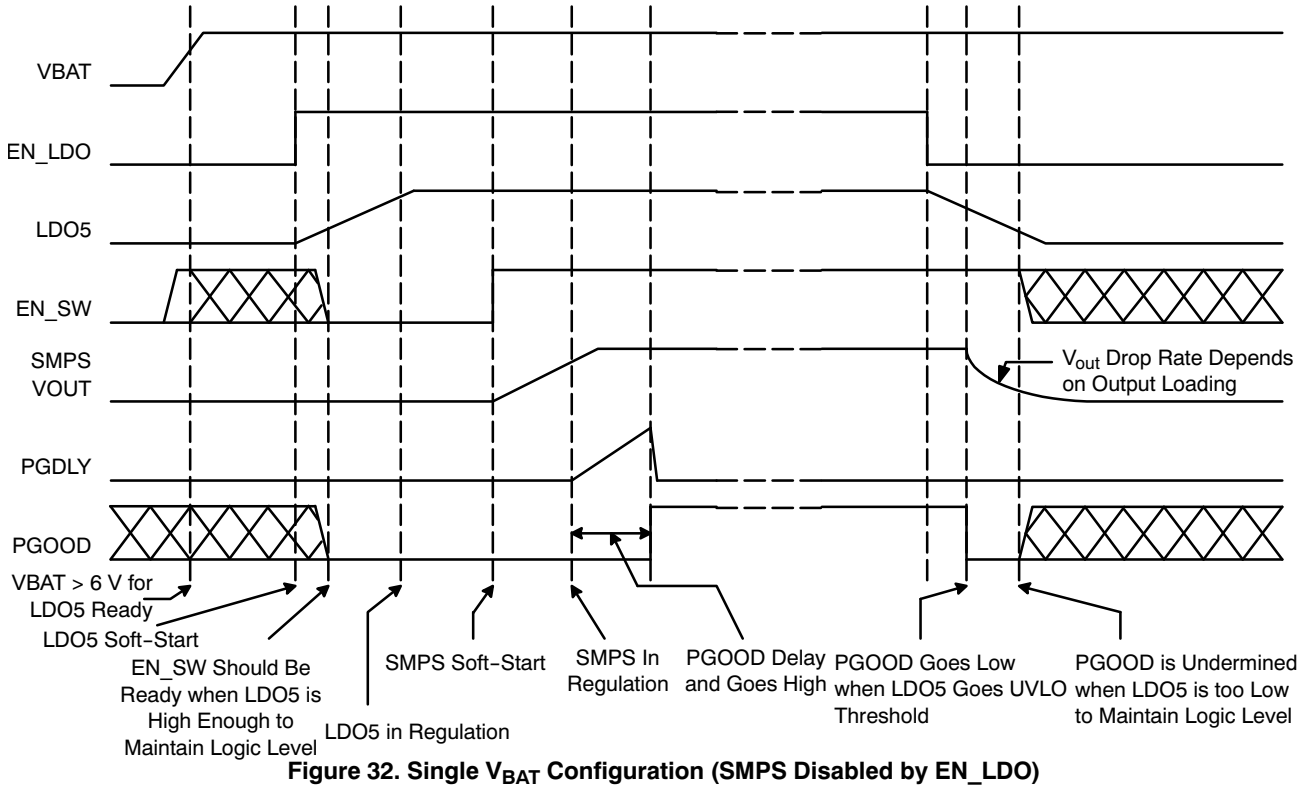


Figure 32. Single V_{BAT} Configuration (SMPS Disabled by EN_LDO)

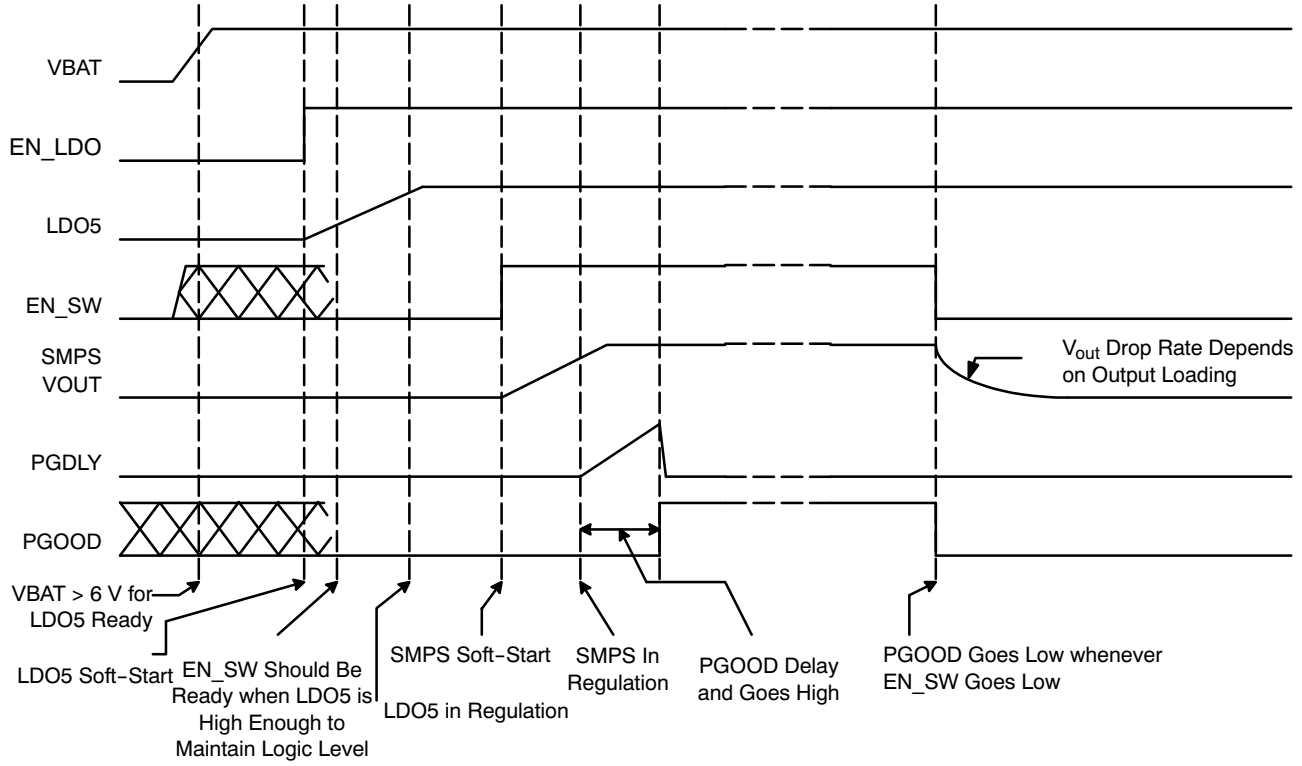


Figure 33. Single V_{BAT} Configuration (SMPS Disabled by EN_SW)

TIMING DIAGRAMS (Continuous)

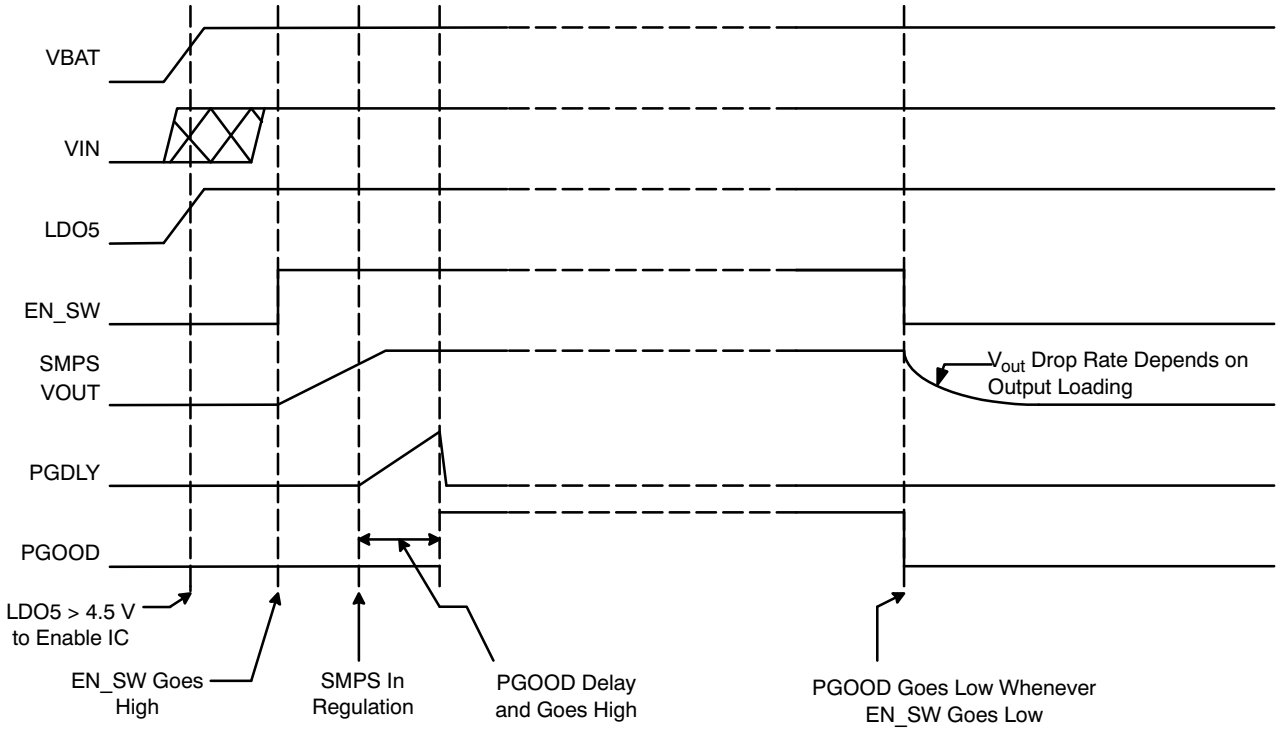


Figure 34. External 5 V (Connect to V_{BAT} and LDO5) and V_{in} Configuration

GENERAL APPLICATION INFORMATION

Introduction

Figure 35 depicts the general control blocks of voltage mode control loop for a synchronous−rectified buck converter. The voltage output V_{out} is regulated to a reference level which is basically governed by the following formula

$$V_{out} = \left(1 + \frac{R1}{R2}\right) \times V_{FB} \quad \text{(eq. 1)}$$

In order to provide proper regulation, the error amplifier is compared with the internal reference voltage and the output of the error amplifier is used to provide pulse−width modulated (PWM) wave.

Loop Compensation

Since NCP1578 is a voltage mode PWM controller with LC output filter, type III compensation network is recommended to provide the good closed loop bandwidth and phase boot with stability under any circumstances. The purpose of compensation is to obtain a stable close loop system with the highest possible bandwidth. In another word, we need to obtain a ”fast and stable” system.

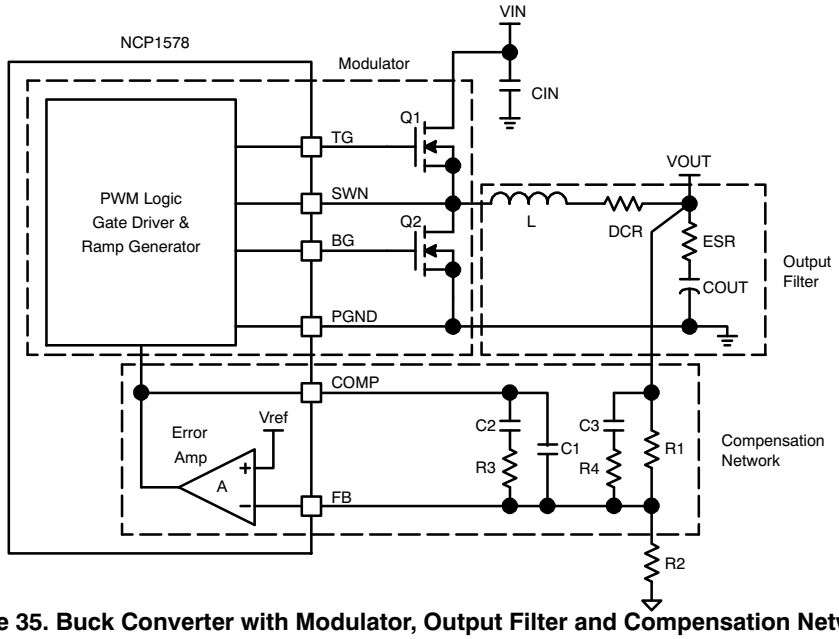


Figure 35. Buck Converter with Modulator, Output Filter and Compensation Network

Equations Involved in Compensation Network

The following equations are provided as general guidelines for defining the positions of poles and zeros of the compensation network.

Output Filter Break Frequency

$$F_{LC} = \frac{1}{2\pi\sqrt{L \times C_{out}}} \quad \text{(LC Double Pole)} \quad \text{(eq. 2)}$$

$$F_{ESR} = \frac{1}{2\pi \times ESR \times C_{out}} \quad \text{(ESR Zero)} \quad \text{(eq. 3)}$$

Compensation Network Break Frequency

$$F_{Z1} = \frac{1}{2\pi \times R3 \times C2} \quad \text{(1st Zero)} \quad \text{(eq. 4)}$$

$$F_{P1} = \frac{1}{2\pi \times R3 \times \left(\frac{C1 \times C2}{C1 + C2}\right)} \quad \text{(1st Pole)} \quad \text{(eq. 5)}$$

$$F_{Z2} = \frac{1}{2\pi \times (R1 + R4) \times C3} \quad \text{(2nd Zero)} \quad \text{(eq. 6)}$$

$$F_{P2} = \frac{1}{2\pi \times R4 \times C3} \quad \text{(2nd Pole)} \quad \text{(eq. 7)}$$

Guidelines for selecting compensation component

1. Select a value of R1 between 2 kΩ and 5 kΩ
2. Target for close loop bandwidth should be less than 50% of switching frequency
3. Place 1st zero at 50% of filter double pole.
4. Place 1st pole at ESR zero
5. Place 2nd zero at filter double pole
6. Place 2nd pole at half the switching frequency.

Figure 36 shows an asymptotic plot of the converter gain against frequency. It gives the general trend of how system and its individual components behave. Actually, the Modulator and Filter Gain has a high peak due to the high Q factor of the output filter. The Open Loop Error Amplifier Gain bounds the Compensation Gain. The Converter Gain is constructed on the graph by summing up the Modulator and Filter Gain (in dB) and the Compensation Gain (in dB). The Compensation Gain uses the external impedance network (R1, R4, C3, C1, C2, R3 at Figure 35) to provide a

stable and high bandwidth overall loop. Worst case component variation should be considered when selecting the components of impedance network such that the control loop phase margin should be greater than 45°.

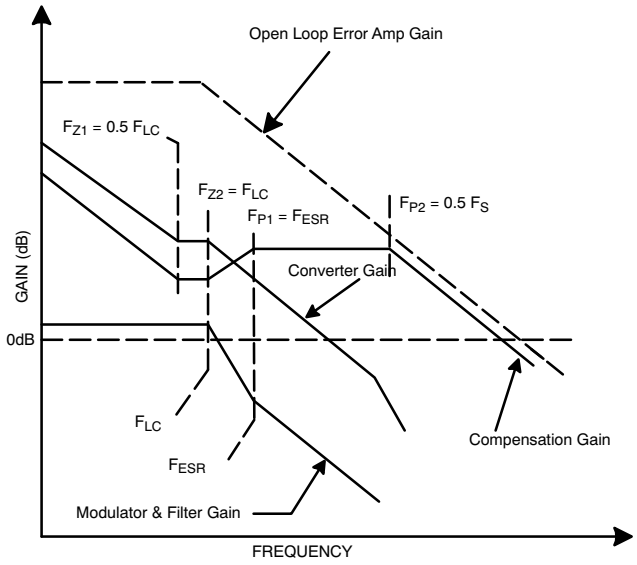


Figure 36. Bode Plot of the Converter Gain

Input Capacitor Selection

It is used to minimize the input voltage ripple from the power supply source. The input capacitors should be placed as close as possible to the drain of the high−side MOSFET and source of the low−side MOSFET. The PCB trace style should be in form of short and wide ones. The voltage rating and the RMS current rating are the important parameters for the bulk input capacitor. In typical application, the bulk capacitor should be selected such that the voltage and current ratings must above the maximum input voltage and largest RMS current required by system. As a safety guideline, the capacitor voltage rating should be at least 1.5 times greater than the maximum input voltage. And the RMS current rating requirement is approximately half of the DC load current. The required input capacitor RMS ripple current rating may be estimated by the following equation:−

$$I_{Cin(RMS)} \geq I_{out} \sqrt{\frac{V_{out}}{V_{in(min)}} - \left(\frac{V_{out}}{V_{in(min)}}\right)^2} \qquad \text{(eq. 8)}$$

Ceramic capacitor is the good choice of the input capacitor for notebook application due to its low ESR and good ripple current rating and high voltage rating. Aluminum electrolytic capacitors are also good choice. They are relatively low cost but they should be used in parallel connection to lower the ESR which is intrinsically high compared with ceramic capacitors.

Output Capacitor Selection

The output capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew−rate transient. So, only specialized low−ESR capacitors should be used for switching regulator applications. For steady state ripple, both ESR and capacitance of the output capacitor contribute output ripple voltage. Normally, ESR is the dominant factor for output ripple voltage. The output ripple voltage ΔV_o can be estimated by the following equation:

$$\Delta V_o = \Delta I_L \times ESR + \frac{\Delta I_L}{8 \times C_{out} \times F_S} \qquad \text{(eq. 9)}$$

and

$$\Delta I_L = \frac{(V_{in} - V_o) \times V_o}{L \times F_S \times V_{in}} \qquad \text{(eq. 10)}$$

$\Delta V_o = \Delta I_L$ X ESR if C_{out} is large enough.

Where:
ΔI_L = Inductor ripple current
ESR = Effective Series Resistance of the output capacitor
L = Inductance
C_{out} = Output capacitance
F_S = Switching frequency
V_{in} = Input Voltage
V_o = Regulated output voltage

From the above equations, it can be seen that the output ripple voltage can be reduced by either using the inductor with larger inductance or the output capacitor with smaller ESR value. In general rule of thumb, the inductor ripple current is typically 30% of the maximum load current and the ripple voltage is typically 2% of the output voltage.

The output capacitor also plays an important role in response of load step up or release transients. The voltage

undershoot ΔV^- due to load step up ΔI can be estimated by the following equation:

$$\Delta V^- = \Delta I \times ESR + \frac{\Delta I}{C_{out}} \times \left(\frac{I - \frac{V_o}{V_{in}}}{F_S} \right) \quad \text{(eq. 11)}$$

and the voltage overshoot ΔV^+ due to load release can be estimated by the following equation:

$$\Delta V^+ = \sqrt{\frac{L \times \left(I_o + \frac{\Delta I_L}{2} \right)^2 + C_{out} \times V_o^2}{C_{out}}} - V_{OUT} \quad \text{(eq. 12)}$$

Where:

I_O = Load current step

Other parameters for selection of output capacitor are the voltage rating and ripple current rating. In general, the voltage rating should be at least 1.25 times the output voltage and the RMS ripple current rating should be greater then the inductor ripple current.

Output Inductor Selection

Basically, a physical inductor can be simply modeled as two components: an ideal inductance L and an ideal resistor DCR. The value of L determines the output ripple voltage, inductor ripple current and performance of load transients. And DCR contributes the system loss. Hence, the higher the DCR, the lower the efficiency of the system will be.

In general, the typical inductor ripple current is 30% of the maximum load current. So based on this criteria, by simple rearrangement of Equation 10, the required inductance can be estimated as follow:-

$$L \geq \frac{(V_{in} - V_o) \times V_o}{0.3 \times I_{O(max)} \times V_{in} \times F_S} \quad \text{(eq. 13)}$$

Where:

$I_{O(max)}$ = Maximum load current

In addition, The DC current rating of the inductor should be about 1.2 times of the peak inductor current at maximum output load current and in order to achieve the good system efficiency, DCR should be minimized. In general, inductor with about 2 mΩ to 3 mΩ per μH should be used. In some cases, larger inductor value can be selected to achieve higher efficiency as long as it still meets the required voltage overshoot at load release and inductor DC current rating.

MOSFET Selection

For selection of MOSFET, gate drive voltage (V_{GS}), ON-Resistance (R_{DSON}), gate input capacitance (C_{GS}) and gate charges (Q_G, Q_{GD} and Q_{GS}) are the key parameters to be considered.

For ON-resistance, in consideration of efficiency and power dissipation, it should be the lower the better. In general, for the buck converter, the R_{DSON} of low side MOSFET is usually lower than that of high side MOSFET. It is because the switching on time of lower side MOSFET is longer than that of high side MOSFET especially at the high V_{in} and low V_o case. For practical application, high side MOSFET and low side MOSFET with RDSON about 7.0 mΩ and 5.0 mΩ respectively can achieve good efficiency.

In order to have better immunity to low side MOSFET false switching on due to high dV/dt switching slew rate of the high side MOSFET, the low side MOSFET should be selected such that the ratio Q_{GD}/Q_{GS} should be low enough.

Overcurrent Protection Component Selection

The overcurrent protection will trip when a peak inductor current hit the I_{LIM} which is determined by the equation:-

$$Isubs_{LIM} = \frac{R_{OC} \times I_{OC}}{R_{DS(on)\_HS}} \quad \text{(eq. 14)}$$

Where:

R_{OC} = Resistor across OCSET pin and V_{in}

I_{OC} = Constant current flowing into the OCSET pin

$R_{DS(on)\_HS}$ = On resistance of the high side MOSFET

Since I_{OC} is varying with device to device and high side MOSFET's $R_{DS(on)}$ varies with temperature, so in order to prevent from mis-triggering the over current protection in normal operating condition, R_{OC} should be determined based on the following corner conditions:-

1. The minimum I_{OC} value from the electrical table.
2. The maximum high side MOSFET's $R_{DS(on)}$ used at the highest junction temperature.
3. Estimate I_{LIM} such that $I_{LIM} > I_{o\_max} + \Delta I_L/2$ where I_{o_max} = Maximum output current rating, ΔI_L = Inductor ripple current.

In addition, a decoupling capacitor Coc should be added in parallel with R_{OC} for noise filtering purpose.

PCB Layout Guidelines

The following items should be considered when preparing PCB layout:

1. All high current traces should be kept as short and wide as possible to reduce power loss. For example the input voltage terminal to the drain of high-side MOSFET, trace from inductor to the output terminal, etc. Power handling and heat sinking capability of power traces can be improved by multiple trace routing at different layer and join them together with multiple vias.
2. Power components which include the input capacitor, MOSFETs, inductor and output capacitor must be placed close together to minimize the current loop.
3. The thermal pad of the QFN20 package should be connected to the ground planes for providing good heat dissipation. It is recommended to use PCB with 1 oz or 2 oz copper foil. The thermal pad can

be connected to either PGND or AGND but not on the both.

4. The ground terminals of input and output capacitors, and the low−side MOSFET's source pin should be connected to PGND ground plane through (if necessary) multiple vias.
5. Noise sensitive traces such as traces of FB, COMP and OCSET should be placed in order to prevent from interference of high voltage switching signal traces like SWN, VBST, TG and BG.
6. The feedback resistor divider should be placed as close as possible to FB pin. The output voltage sensing signal should be come up from the separated noise free signal trace.
7. To minimize the effect of parasitic impedance, traces between gate drivers to MOSFET's gates should be as shortest as possible.

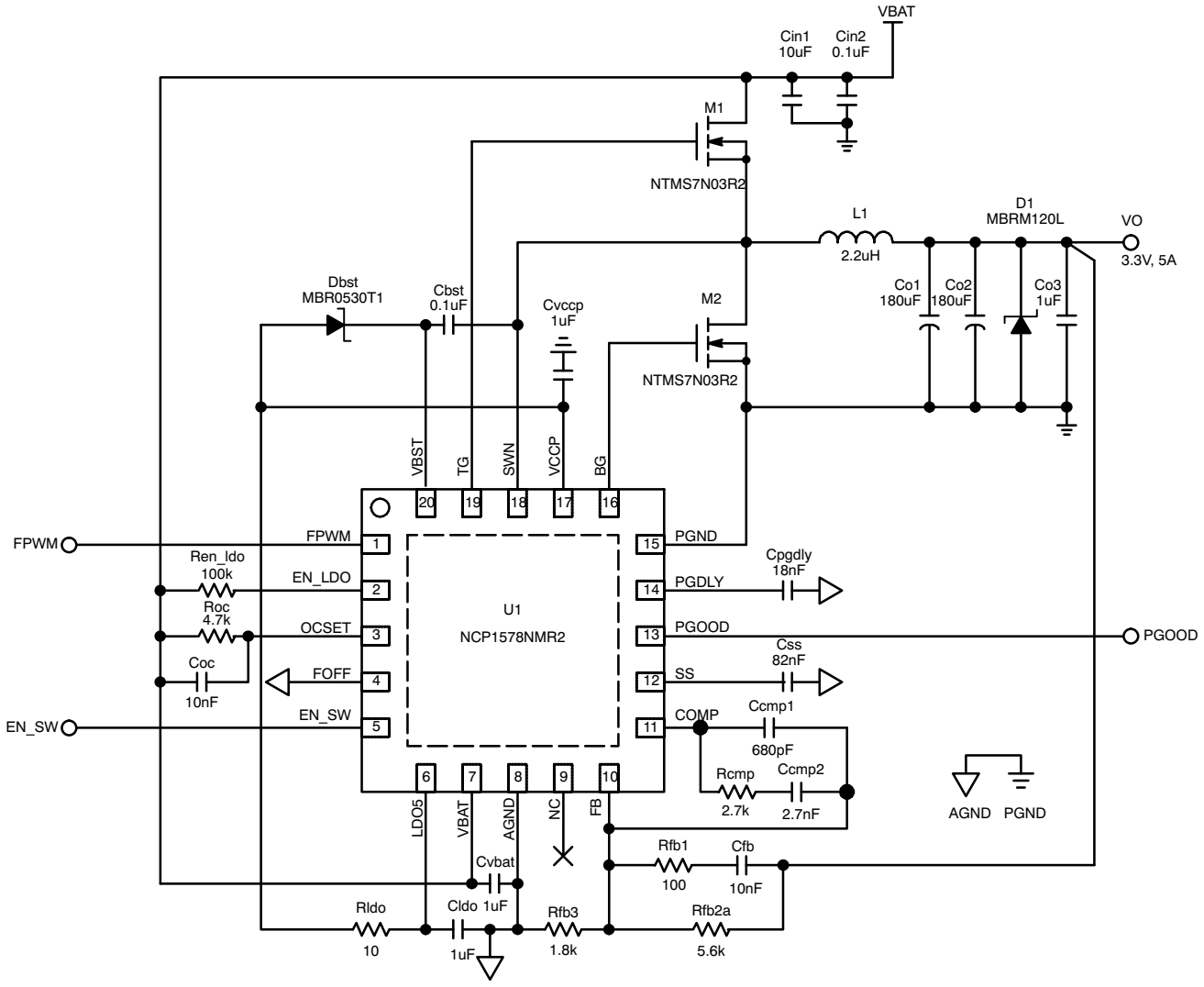


Figure 37. Typical Application Schematic Diagram

BILL OF MATERIAL (BOM) FOR THE TYPICAL APPLICATION SCHEMATIC

Item	Qty	Designator	Part Description	Vendor
1	1	U1	NCP1578 Buck Controller	ON Semicondutor
2	2	M1, M2	NTMS7N03R2 MOSFET N−Ch 7A, 30V, 23mΩ @ 4.5V	ON Semicondutor
3	1	D1	MBRM120L Schottky Diode 1A, 20V, POWERMITE	ON Semicondutor
4	1	Dbst	MBR0530T1 Schottky Diode 0.5A, V_F=0.375V @ 0.1A, SOD−123	ON Semicondutor
5	1	L1	FDA1055−2R2M 2.2uH, 4.8mΩ max	TOKO
6	2	Co1, Co2	SP−CAP, 180uF, 6.3V, ESR=10mΩ SIZE−D	Panasonic
7	1	Cin1	Ceramic Capacitor 10uF/25V, 2512	
8	4	Co3, Cvbat, Cldo, Cvccp	Ceramic Capacitor 1uF/10V, 0805	
9	2	Cin2, Cbst	Ceramic Capacitor 0.1uF/25V, 0603	
10	1	Cpgdly	Ceramic Capacitor 18nF/50V, 0603	
11	1	Css	Ceramic Capacitor 82nF/50V, 0603	
12	1	Ccmp1	Ceramic Capacitor 680pF/50V, 0603	
13	1	Ccmp2	Ceramic Capacitor 2.7nF/50V, 0603	
14	2	Cfb, Coc	Ceramic Capacitor 10nF/50V, 0603	
15	1	Rcmp	Resistor 2.7kΩ, 0603	
16	1	Rfb1	Resistor 100Ω, 0603	
17	1	Rfb2a	Resistor 5.6kΩ, 0603	
18	1	Rfb3	Resistor 1.8kΩ, 0603	
19	1	Rldo	Resistor 10Ω, 0603	
20	1	Ren_ldo	Resistor 100kΩ, 0603	
21	1	Roc	Resistor 4.7kΩ, 0603	

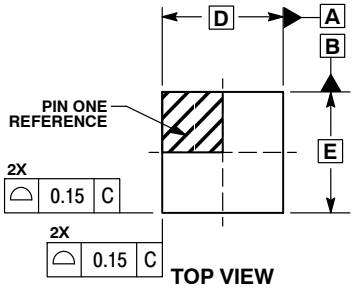
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

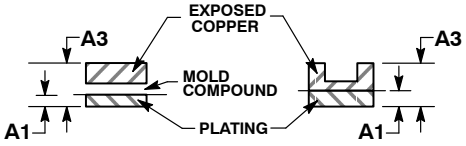
ON Semiconductor®

QFN20, 4x4, 0.5P
CASE 485E
ISSUE C

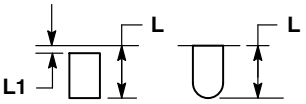
DATE 13 FEB 2018

SCALE 2:1

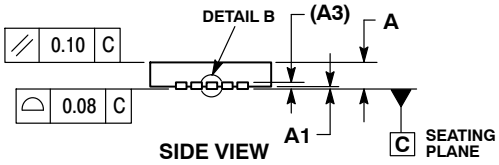




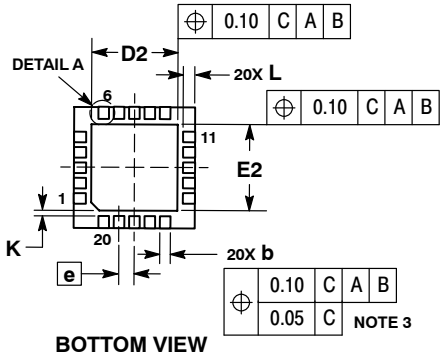
DETAIL B
ALTERNATE CONSTRUCTIONS



DETAIL A
OPTIONAL CONSTRUCTIONS

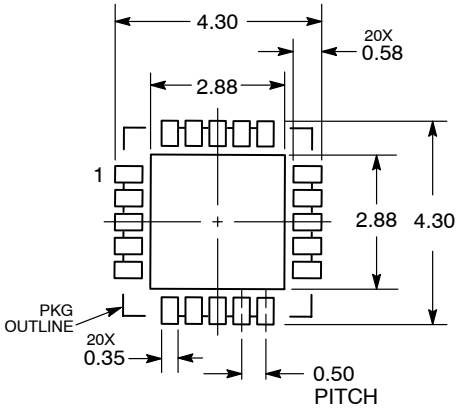


SIDE VIEW



BOTTOM VIEW

SOLDERING FOOTPRINT*



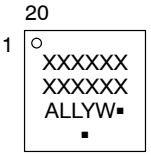
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.60	2.90
E	4.00 BSC	
E2	2.60	2.90
e	0.50 BSC	
K	0.20 REF	
L	0.35	0.45
L1	0.00	0.15

GENERIC MARKING DIAGRAM*



XXXXXX= Specific Device Code
A = Assembly Location
LL = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**QFN20, 4X4, 0.5P**	**PAGE 1 OF 1**

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