NCL30100

Fixed Off Time Switched Mode LED Driver Controller

The NCL30100 is a compact switching regulator controller intended for space constrained constant current high−brightness LED driver applications where efficiency and small size are important. The controller is based on a peak current, quasi fixed−off time control architecture optimized for continuous conduction mode step−down (buck) operation. This allows the output filter capacitor to be eliminated. In this configuration, a reverse buck topology is used to control a cost effective N−type MOSFET. Moreover, this controller employs negative current sensing thus minimizing power dissipation in the current sense resistor. The off time is user adjustable through the selection of a small external capacitor, thus allowing the design to be optimized for a given switching frequency range. The control loop is designed to operate up to 700 kHz allowing the designer the flexibility to use a very small inductor for space constrained applications.

The device has been optimized to provide a flexible inductive step−down converter to drive one or more high power LED(s). The controller can also be used to implement non−isolated buck−boost driver topologies.

Features

- Quasi−Fixed OFF Time, Peak Current Control Method
- N−FET Based Controller Architecture
- Up to 700 kHz Switching Frequency
- Up to >95% Efficiency
- No Output Capacitor Needed
- V_{CC} Operation from 6.35 – 18 V
- Adjustable Current Limit with Negative Sensing
- Inherent Open LED Protected
- Very Low Current Consumption at Startup
- Undervoltage Lockout
- Compact Thin TSOP−6 Pb−Free Package
- −40 to + 125°C Operating Temperature Range
- This is a Pb−Free Device

Typical Applications

- Low Voltage Halogen LED Replacement (MR 16)
- LED Track Lighting
- Landscape Lighting
- Solar LED Applications
- Transportation Lighting
- 12 V LED Bulb Replacement
- Outdoor Area Lighting
- LED Light Bars

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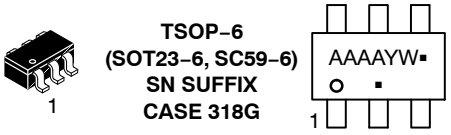
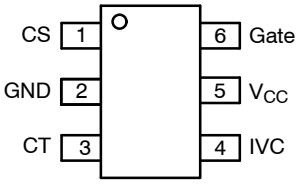
MARKING DIAGRAM



AAA = Specific Device Code
A =Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCL30100SNT1G	TSOP−6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

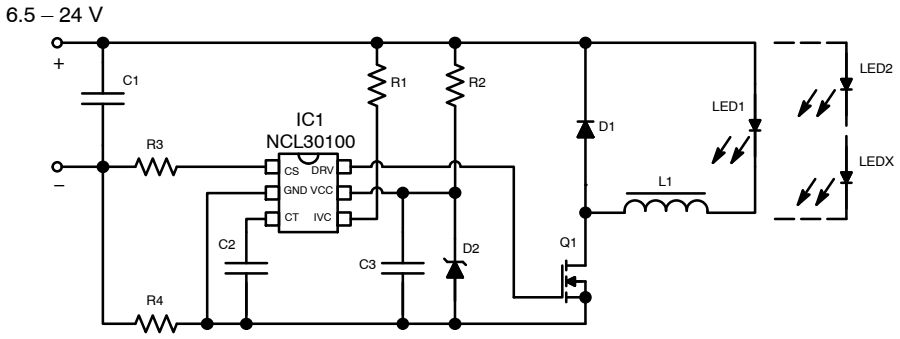


Figure 1. Typical Application Example of the LED Converter

PIN FUNCTION DESCRIPTION

Pin N°	Pin Name	Function	Pin Description
1	CS	Current sense input	A resistor divider consisting of R3 and R4 is used to set the peak current sensed through the MOSFET switch
2	GND	Ground	Power ground.
3	C_T	Timing capacitor	Capacitor to establish the off time duration
4	IVC	Input voltage compensation	The current injected into the input varies the switch off time and I_{PK} allowing for feedforward compensation.
5	V_{CC}	Input supply	Supply input for the controller. The input is rated to 18 V but as illustrated Figure 1, a simple zener diode and resistor can allow the LED string to be powered from a higher voltage
6	DRV	Driver output	Output drive for an external power MOSFET

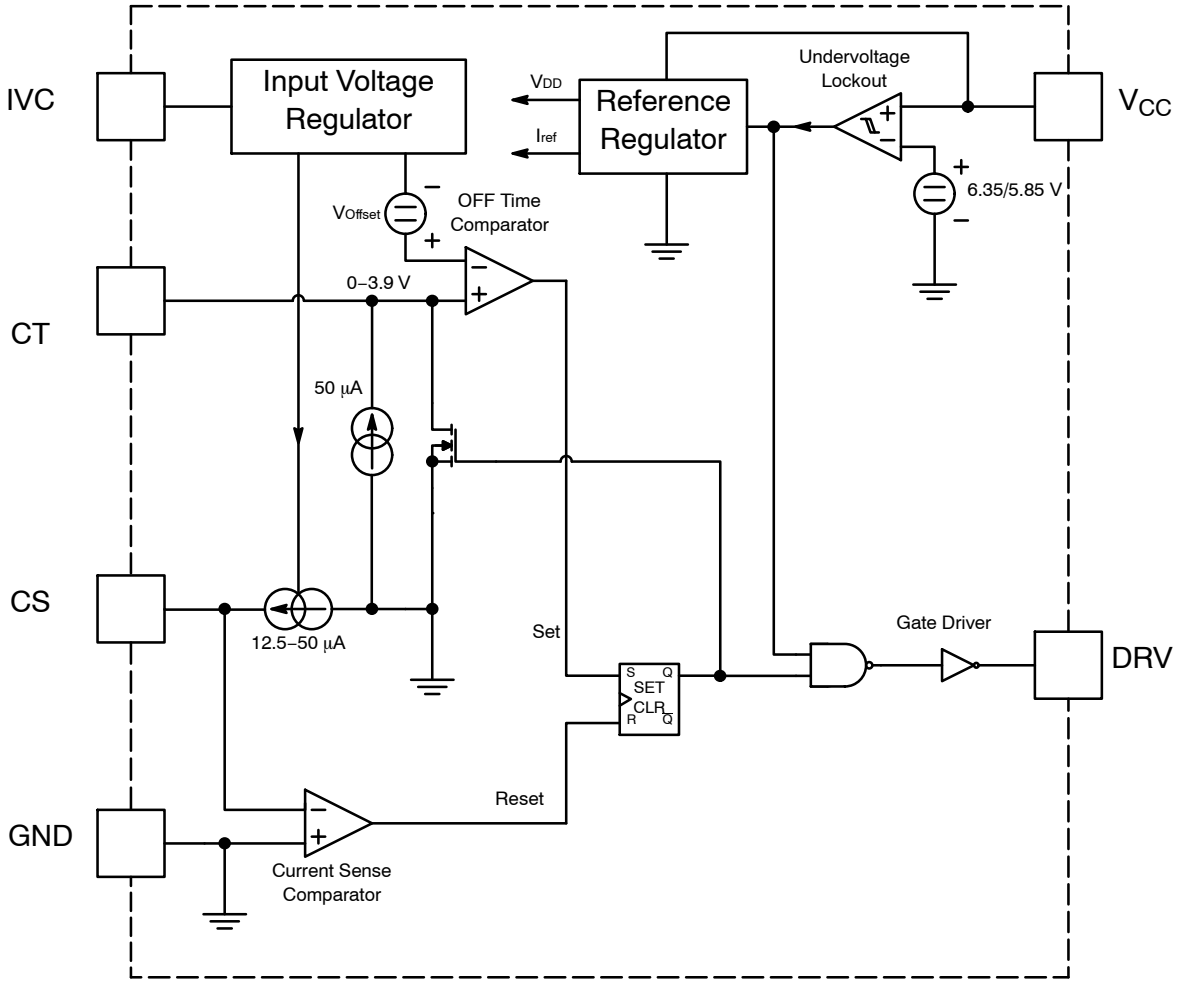


Figure 2. Simplified Circuit Architecture

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	18	V
IVC Pins Voltage Range	IVC	−0.3 to 18	V
CS and C_T Pin Voltage Range	V_{in}	−0.3 to 10	V
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	178	°C/W
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C
ESD Voltage Protection, Human Body Model (HBM)	$V_{ESD-HBM}$	2	kV
ESD Voltage Protection, Machine Model (MM)	V_{ESD-MM}	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device(s) contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per JEDEC Standard JESD22−A114E
   Machine Model 200 V per JEDEC Standard JESD22−A115−A
2. This device meets latchup tests defined by JEDEC Standard JESD78.
3. Moisture Sensitivity Level (MSL) 1.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, unless otherwise noted)

SUPPLY SECTION

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
INPUT VOLTAGE COMPENSATION						
Offset Voltage		$V_{(offset)}$	1.10	1.30	1.45	V
C_T Pin Voltage	IVC Current = 25 μA (Including $V_{(offset)}$)	$V_{CT-25\mu A}$	1.69	2.08	2.47	V
C_T Pin Voltage	IVC Current = 50 μA (Including $V_{(offset)}$)	$V_{CT-50\mu A}$	2.12	2.6	3.05	V
IVC pin internal resistance (Note 4)		R_{IVC}		17		kΩ
C_T PIN – OFF TIME CONTROL						
Source Current	C_T Pin Grounded, 0 ≤ T_J ≤ 85°C	I_{CT}	47.25	50	52.75	μA
Source Current	C_T Pin Grounded, −40 ≤ T_J ≤ 125°C	I_{CT}	45.25	50	52.75	μA
Source Current Maximum Voltage Capability (Note 4)		$V_{CT(max)}$	–	4.3	–	V
Minimum C_T Pin Voltage (Note 4)	Pin Unloaded, Discharge Switch Turned on	$V_{CT(min)}$	–	–	20	mV
Pin to ground capacitance (Note 4)		C_{CT}	–	8	–	pF
Propagation Delay (Note 4)	CT Reach V_{CT} Threshold to Gate Output	CT_{delay}	–	220	–	ns
CURRENT SENSE						
Minimum Source Current	IVC = 180 μA, C_T Pin Grounded, 0 ≤ T_J ≤ 85°C	$I_{CS(min)}$	11. 75	12.5	13.25	μA
Minimum Source Current	IVC = 180 μA, C_T Pin Grounded, −40 ≤ T_J ≤ 125°C	$I_{CS(min)}$	11.35	12.5	13.25	μA
Maximum Source Current	IVC = 0 μA, C_T Pin Grounded, 0 ≤ T_J ≤ 85°C	$I_{CS(max)}$	47.25	50	52.75	μA
Maximum Source Current	IVC = 0 μA, C_T Pin Grounded, −40 ≤ T_J ≤ 125°C	$I_{CS(max)}$	45.25	50	52.75	μA
Comparator Threshold Voltage (Note 4)		V_{th}	–	38	–	mV
Propagation Delay	CS Falling Edge to Gate Output	CS_{delay}	–	215	310	ns
GATE DRIVER						
Sink Resistance	I_{sink} = 30 mA	R_{OL}	5	15	40	Ω
Source Resistance	I_{source} = 30 mA	R_{OH}	20	60	100	Ω
POWER SUPPLY						
Startup Threshold	V_{CC} increasing	$V_{CC(on)}$	–	6.35	6.65	V
Minimum Operating Voltage	V_{CC} decreasing	$V_{CC(off)}$	5.45	5.85	–	V
Vcc Hysteresis (Note 4)		$V_{CC(hyst)}$	–	0.5	–	V
Startup Current Consumption	V_{CC} = 6 V	I_{CC1}	–	22	35	μA
Steady State Current Consumption (Note 4)	C_{DRV} = 0 nF, f_{SW} = 100 kHz, IVC = open, V_{CC} = 7 V	I_{CC2}		300		μA
Steady State Current Consumption	C_{DRV} = 1 nF, f_{SW} = 100 kHz, IVC = open, V_{CC} = 7 V	I_{CC2}	0.5	1	1.15	mA

4. Guaranteed by design

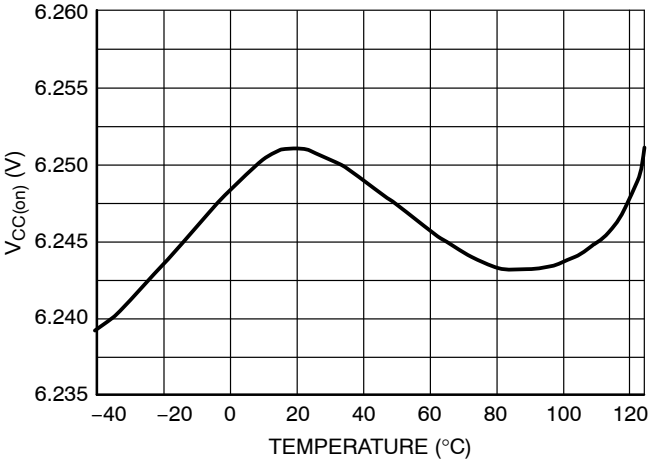


Figure 3. $V_{startup}$ Threshold vs. Junction Temperature

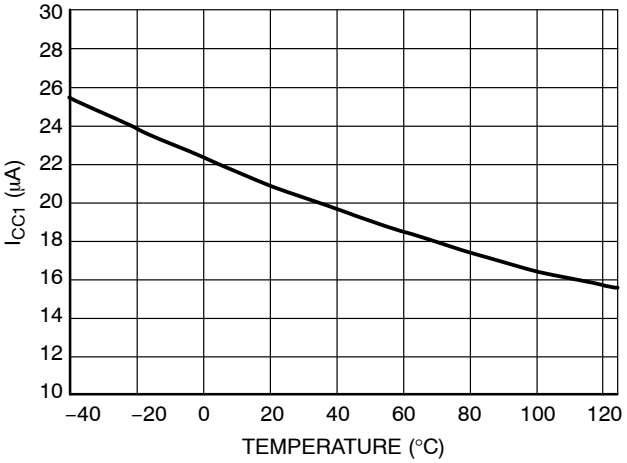


Figure 4. Startup Current Consumption vs. Junction Temperature

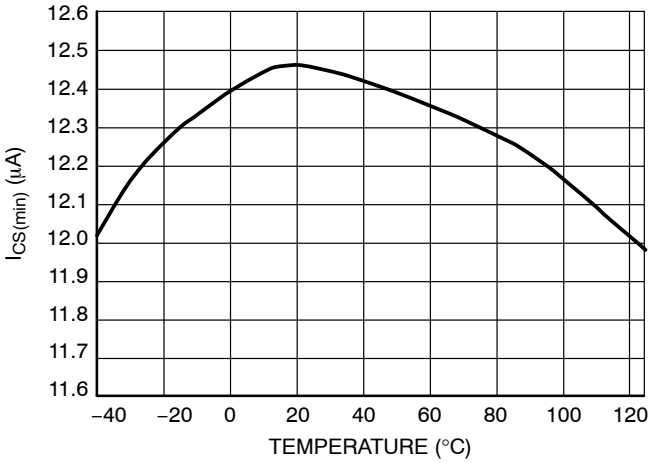


Figure 5. Minimum Source Current vs. Junction Temperature

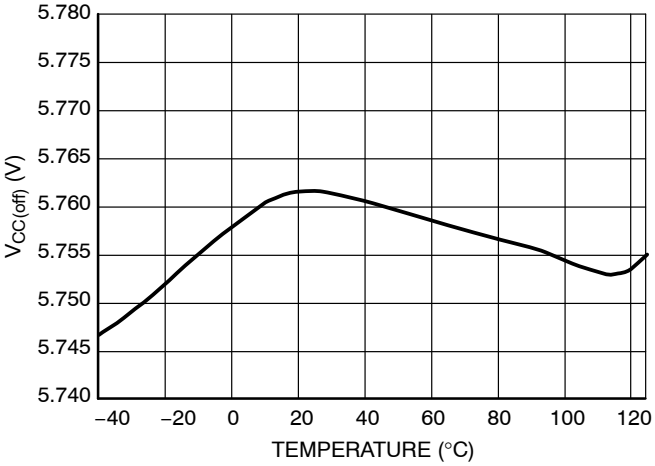


Figure 6. Minimum Operating Voltage Threshold vs. Junction temperature

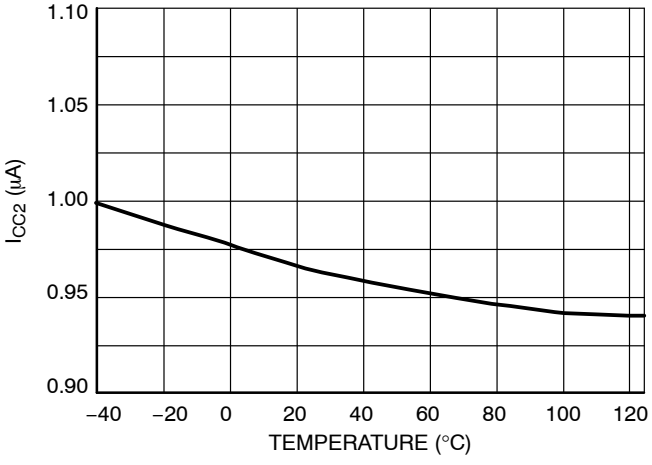


Figure 7. Steady State Current Consumption vs. Junction Temperature

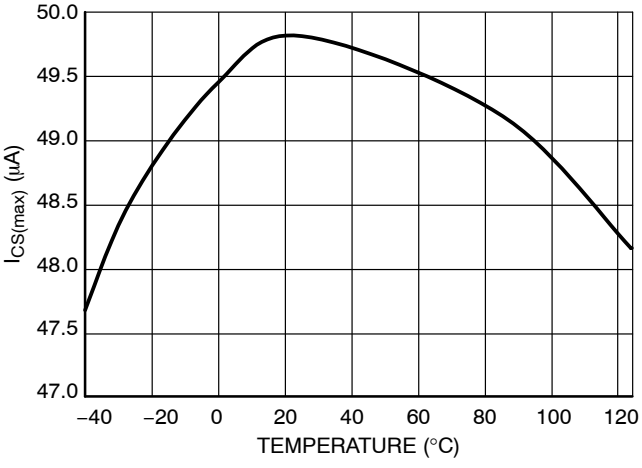


Figure 8. Maximum Source Current vs. Junction Temperature

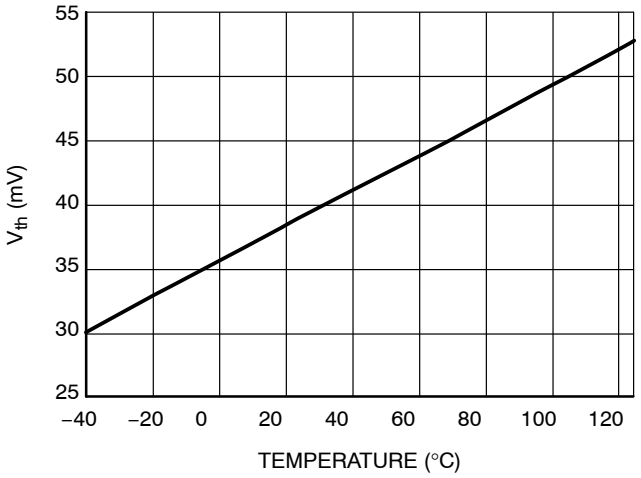


Figure 9. Comparator Threshold Voltage vs. Junction Temperature

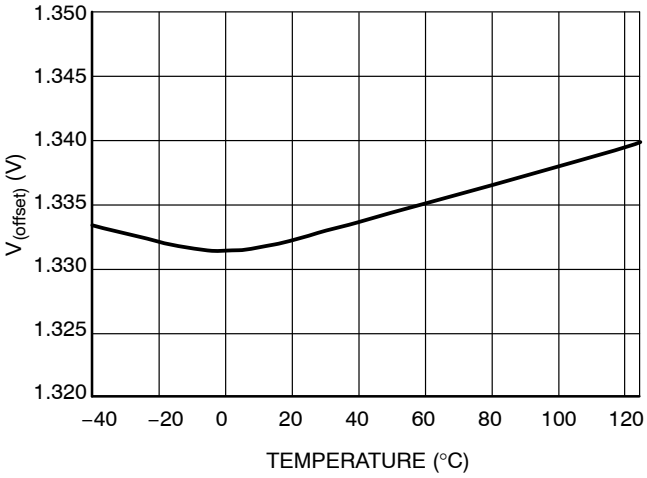


Figure 10. Offset Voltage vs. Junction Temperature

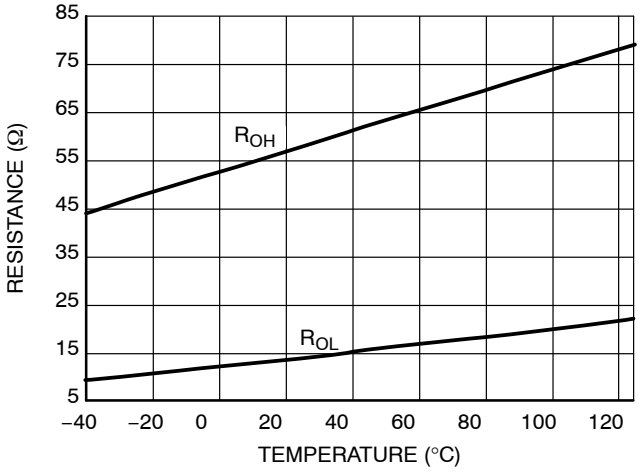


Figure 11. Drive Sink and Source Resistance vs. Junction Temperature

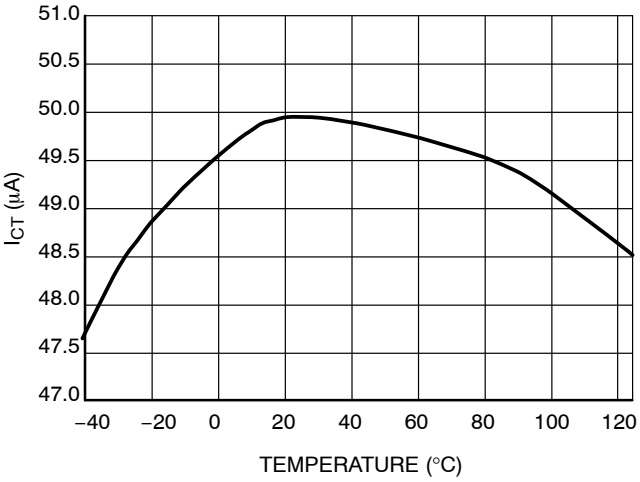


Figure 12. C_T Source Current vs. Junction Temperature

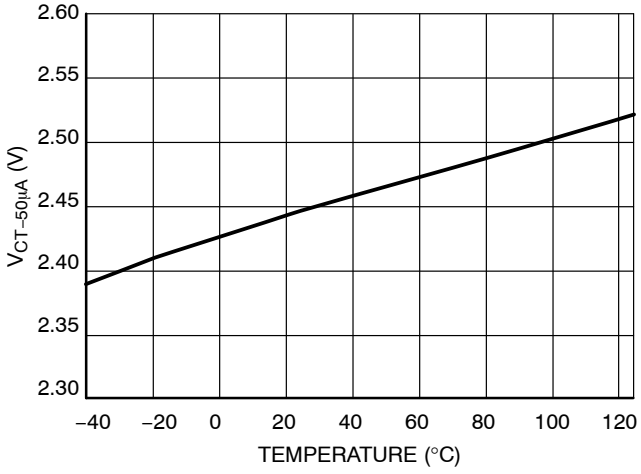


Figure 13. C_T Pin Voltage vs. Input Voltage Compensation Current

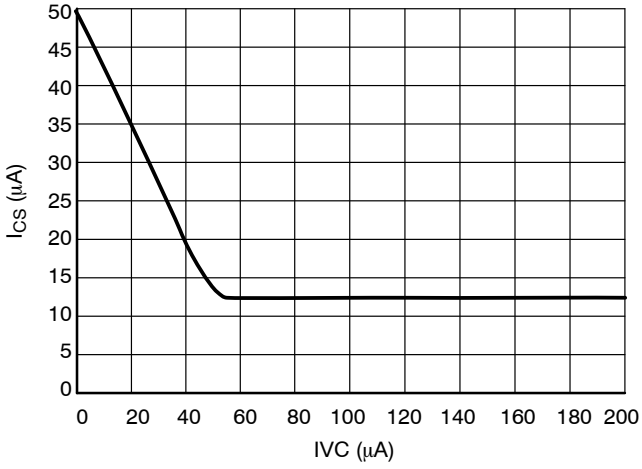


Figure 14. I_{CT} Dependence on IVC Current

APPLICATION INFORMATION

The NCL30100 implements a peak current mode control scheme with a quasi−fixed OFF time. An optional input feedforward voltage control is provided to enhance regulation response with widely varying input voltages. Only a few external components are necessary to implement the buck converter. The NCL30100 incorporates the following features:

- Very Low Startup Current: The patented internal supply block is specially designed to offer a very low current consumption during startup.
- Negative Current Sensing: By sensing the total current, this technique does not impact the MOSFET driving voltage (V_{GS}) during switching. Furthermore, the programming resistor together with the pin capacitance forms a residual noise filter which blanks spurious spikes. This approach also supports a flexible resistor selection. Finally unlike a positive sensing approach, there is virtually no power dissipation in the current sense resistor thus improving efficiency.
- Controller architecture supports high brightness LED drive current requirements: Selection of the external n−channel MOSFET can be easily optimized based on operation voltage, drive current and size giving the designer flexibility to easily make design tradeoffs.
- Typical ±5.5% Current Regulation: The I_{CS} pin offers ±5.5% from 0 to 85°C (+5.5% −9.5% across −40°C to 125°C) accuracy of the current typically, so the LED peak current is precisely controlled
- No output capacitor is needed: By operating the controller in continuous conduction mode, it is possible to eliminate the bulky output filter capacitor.

The following section describes in detail each of the control blocks

Current Sensing Block

The NCL30100 utilizes a technique called negative current sensing which is used to set the peak current through the switch and the inductor. This approach offers several benefits over traditional positive current sensing.

- Maximum peak voltage across the current sense resistor is user controlled and can be optimized by changing the value of the shift resistor.
- The gate drive capability is improved because the current sense resistor is located out of the gate driver loop and does not deteriorate the switch on and also switch off gate drive amplitude.
- Natural leading edge blanking is filter switching noise at FET turn−in
- The CS pin is not exposed to negative voltage, which could induce a parasitic substrate current within the IC and distort the surrounding internal circuitry.

The current sensing circuit is shown in Figure 15.

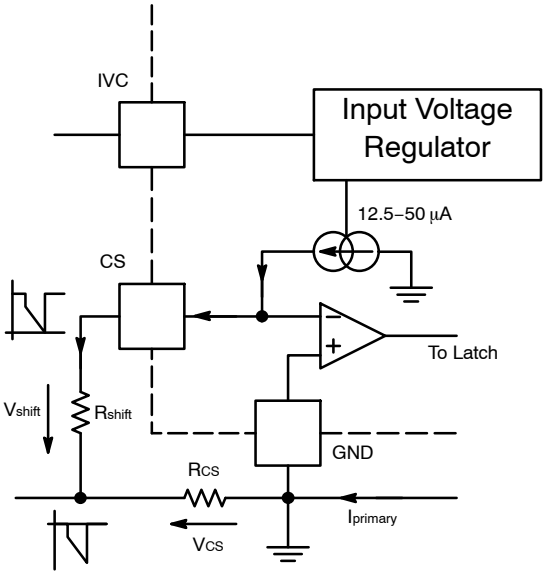


Figure 15. Primary Current Sensing

Once the external MOSFET is switched on, the inductor current starts to flow through the sense resistor R_{CS}. The current creates a voltage drop V_{CS} on the resistor R_{CS}, which is negative with respect to GND. Since the comparator connected to CS pin requires a positive voltage, a voltage V_{shift} is developed across the resistor R_{shift} by a current source which level−shifts the negative voltage V_{CS}. The level−shift current is in the range from 12.5 to 50 μA depending on the optional input voltage compensation loop control block signal (see more details in the input voltage compensation section). The peak inductor current is equal to:

$$I_{pk} = \frac{I_{CS} \cdot R_{shift} - V_{th}}{R_{CS}} \qquad \text{(eq. 1)}$$

To achieve the best I_{pk} precision, higher values of I_{CS} should be used. The Equation 1 shows the higher drop on R_{CS} reduces the influence of the V_{th} tolerance. Vth is the comparator threshold which is nominally 38 mV.

A typical CS pin voltage waveform for continuous condition mode is shown in Figure 16.

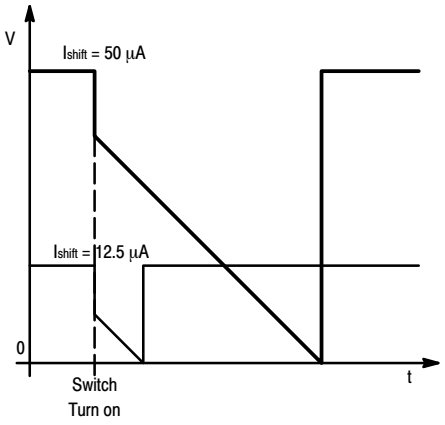


Figure 16. CS Pin Voltage

Figure 16 also shows the effect of the inductor current based on the range of control possible via the IVC input.

OFF Time Control

The internal current source, together with an external capacitor, controls the switch−off time. In addition, the optional IVC control signal can modulate the off time based on input line voltage conditions. This block is illustrated in Figure 17.

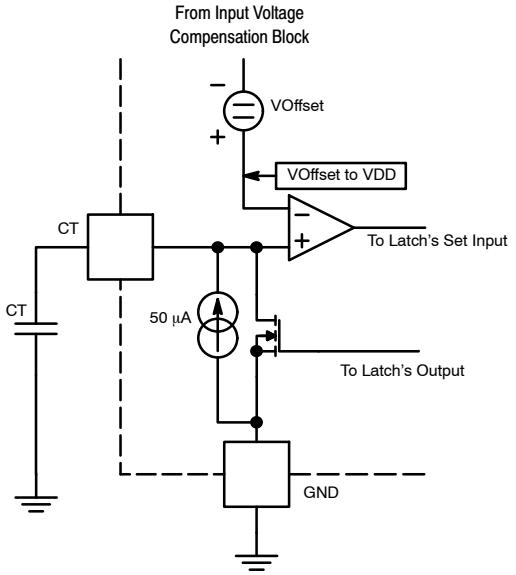


Figure 17. OFF Time Control

During the switch−on time, the C_T capacitor is kept discharged by an internal switch. As soon as the latch output changes to a low state, the I_{source} is enabled and the voltage across C_T starts to ramp−up until its value reaches the threshold given by the V_{offset}. The current injected into IVC can change this threshold. The IVC operation will be discussed in the next section.

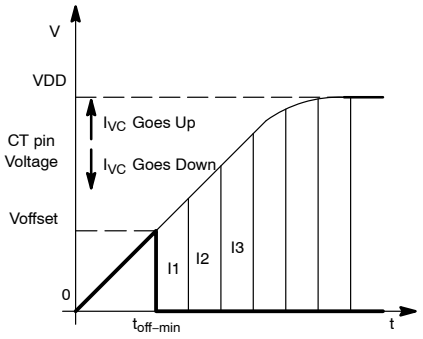


Figure 18. CT Pin Voltage

The voltage that can be observed on C_T pin is shown in Figure 18. The bold line shows the minimum IVC current when the off time is at its minimum. The amount of current injected into the IVC input can increase the off time by changing the turn off comparator switching threshold. I1, I2,

and I3 represent different delays depending on the magnitude of IVC.

Gate Driver

The Gate Driver consists of a CMOS buffer designed to directly drive a power MOSFET. It features unbalanced source and sink capabilities to optimize switch on and off performance without additional external components. The power MOSFET is switched off at high drain current, to minimize its switch off losses the sink capability of the gate driver is increased for a faster switch off. On the other hand, the source capability of the driver is reduced to slow−down the power MOSFET at switch on in order to reduce EMI generation. Whenever the IC supply voltage is lower than the under voltage threshold, the Gate Driver is low, pulling down the gate to ground thus eliminating the need for an external resistor.

Input Voltage Compensation:

The Input Voltage Compensation block gives the user optional flexibility to sense the input voltage and modify the current sense threshold and off time. This function provides a feed forward mechanism that can be used when the input voltage of the controller is loosely regulated to improve output current regulation. If the input voltage is well regulated, the IVC input can also be used to adjust the offset of the off time comparator and the current sense control to achieve the best current regulation accuracy.

An external resistor connected between IVC and the input supply results in a current being injected into this pin which has an internal 17 kΩ resistor connected to a current mirror. This current information is used to modify V_{offset} and I_{CS}. By changing V_{offset} the off time comparator threshold is modified and the off time is increased. A small capacitor should be connected between the IVC pin and ground to filter out noise generated during switching period. Figure 19 shows the simplified internal schematic:

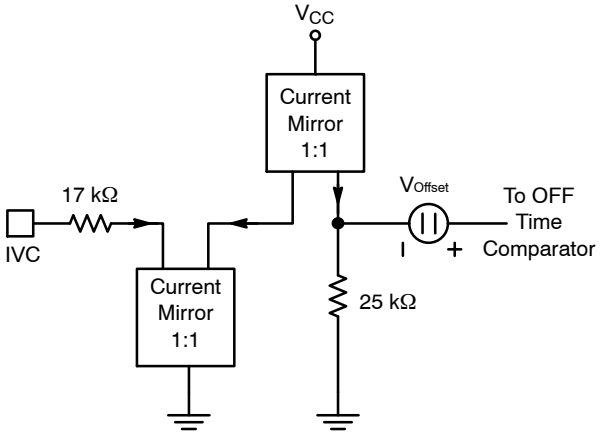


Figure 19. Input Voltage Compensation, OFF Time Control

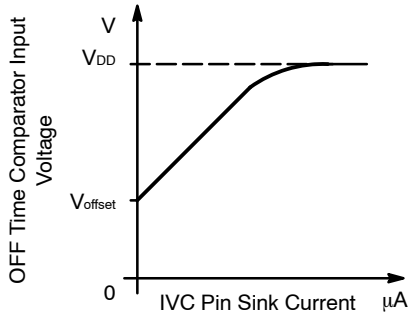


Figure 20. IVC Loop Transfer Characteristic

The transfer characteristic (output voltage to input current) of the input voltage compensation loop control block can be seen in Figure 20. V_{DD} refers to the internal stabilized supply. If no IVC current is injected, the off time comparator is set to V_{offset}.

The value of the current injected into IVC also change Ics. This is accomplished by changing the voltage drop on R_{shift}. The corresponding block diagram of the IVC pin can be seen in Figure 21.

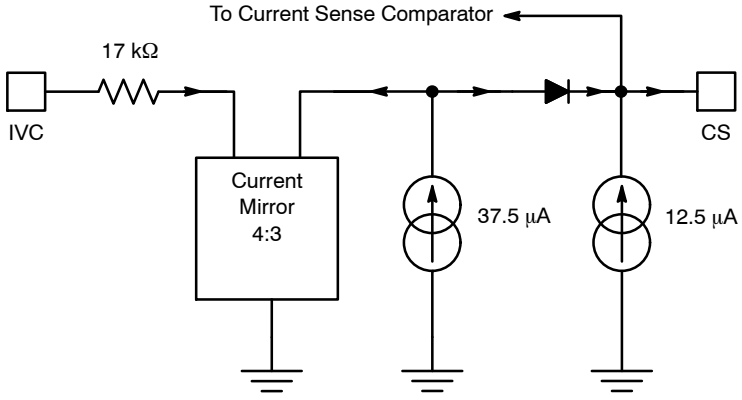


Figure 21. Input Voltage Compensation Loop – Current Sense Control

The current sense characteristic can be seen in Figure 22. As illustrated, by varied the IVC current between 0 – 50 μA, the sourcing current can range from 12.5 to 50 μA.

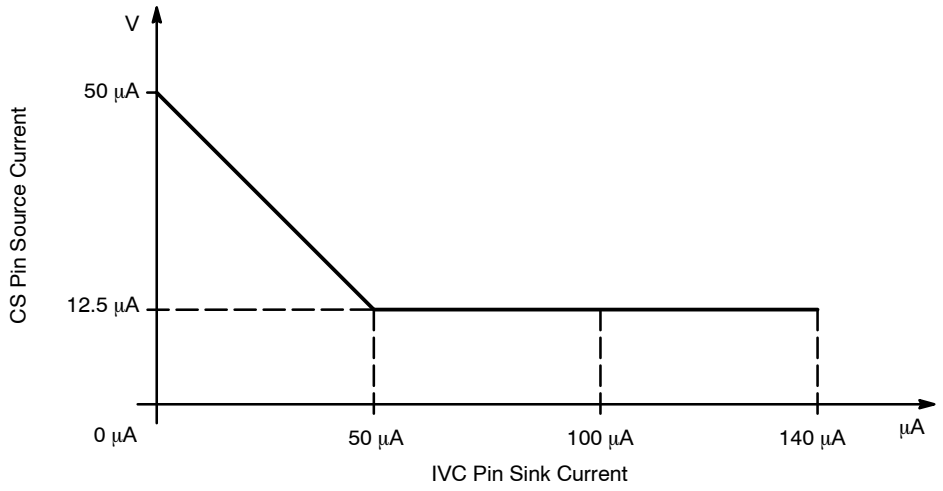


Figure 22. Current Sense Regulation Characteristic

Biasing the controller

The NCL30010 Vcc input can range up to 18 V. For applications that have an input voltage that is greater than that level, an external resistor should be connected between V_{in} and the V_{CC} supply capacitor. The value of the resistor can be calculated as follows:

$$R_2 = \frac{V_{in} - V_{CC}}{I_{CC2}} \quad \text{(eq. 2)}$$

Where:
V_{CC} – Voltage at which IC operates (see spec.)
I_{CC2} – Current at steady state operation
V_{in} – Input voltage

The I_{CC} current is composed of two components: The quiescent current consumption (300 μA) and the switching current consumption. The driver consumption depends on the MOSFET selected and the switching frequency. Total current consumption can be calculated using following formula:

$$I_{CC} = 300 \cdot 10^{-6} + C_{MOSFET} \cdot V_{CC} \cdot f_{switching} \quad \text{(eq. 3)}$$

In applications where the input voltage Vin is varying dramatically, a zener can be used to limit the voltage going into V_{CC}, thus reducing the switching current contribution.

Switching Frequency

The switching frequency varies with the output load and input voltage. The highest frequency appears at highest input voltage. Since the peak inductor current is fixed, the on−time portion of the switching period can be calculated:

$$t_{on} = L \cdot \frac{I_{pk}}{V_{in}} + CS_{delay} \quad \text{(eq. 4)}$$

Where:
L – Inductor inductance
I_{pk} – Peak current

As seen from the above equation, the turn on time depends on the input voltage. In the case of a low voltage AC input where there is ripple due to the time varying input voltage and input rectifier, natural frequency dithering is produced to improve the EMI signature of the LED driver.

The turn off time is determined by the charging of the external capacitor connected to the CT pin. The minimum t_{off} value can be computed as:

$$t_{off} = C_T \cdot \frac{V_{offset}}{I_{CT}} + CT_{delay} \quad \text{(eq. 5)}$$

Where:
V_{offset} – Offset voltage (see parametric table)
I_{CT} – C_T pin source current (see parametric table)

Finally, the switching frequency then can be evaluated by:

$$F_{SW} = \frac{1}{t_{on} + t_{off}} = \frac{1}{\frac{L \cdot I_{pk}}{V_{in}} + \frac{C_T \cdot V_{offset}}{50 \cdot 10^{-6}} + 435 \cdot 10^{-9}} \quad \text{(eq. 6)}$$

The sum of the nominal CS_{delay} and CT_{delay} is approximately 435 nsec.

Reverse Buck Operating Description

Figure 23 illustrates a typical application schematic and Figure 24 displays simplified waveforms illustrate the converter in steady state operation for critical circuit nodes.

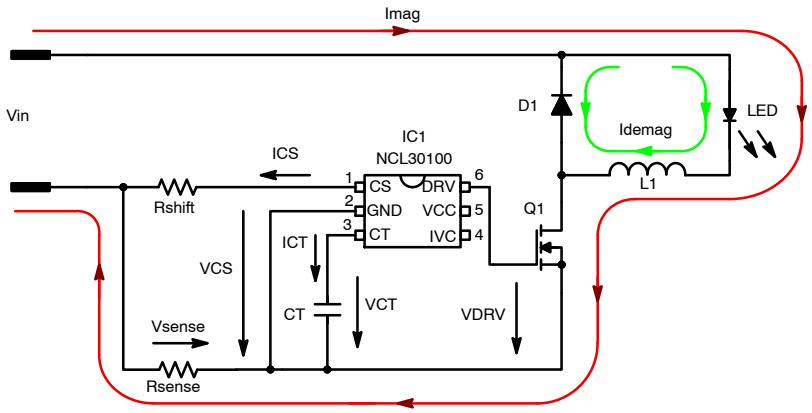


Figure 23. Simplified Application Schematic

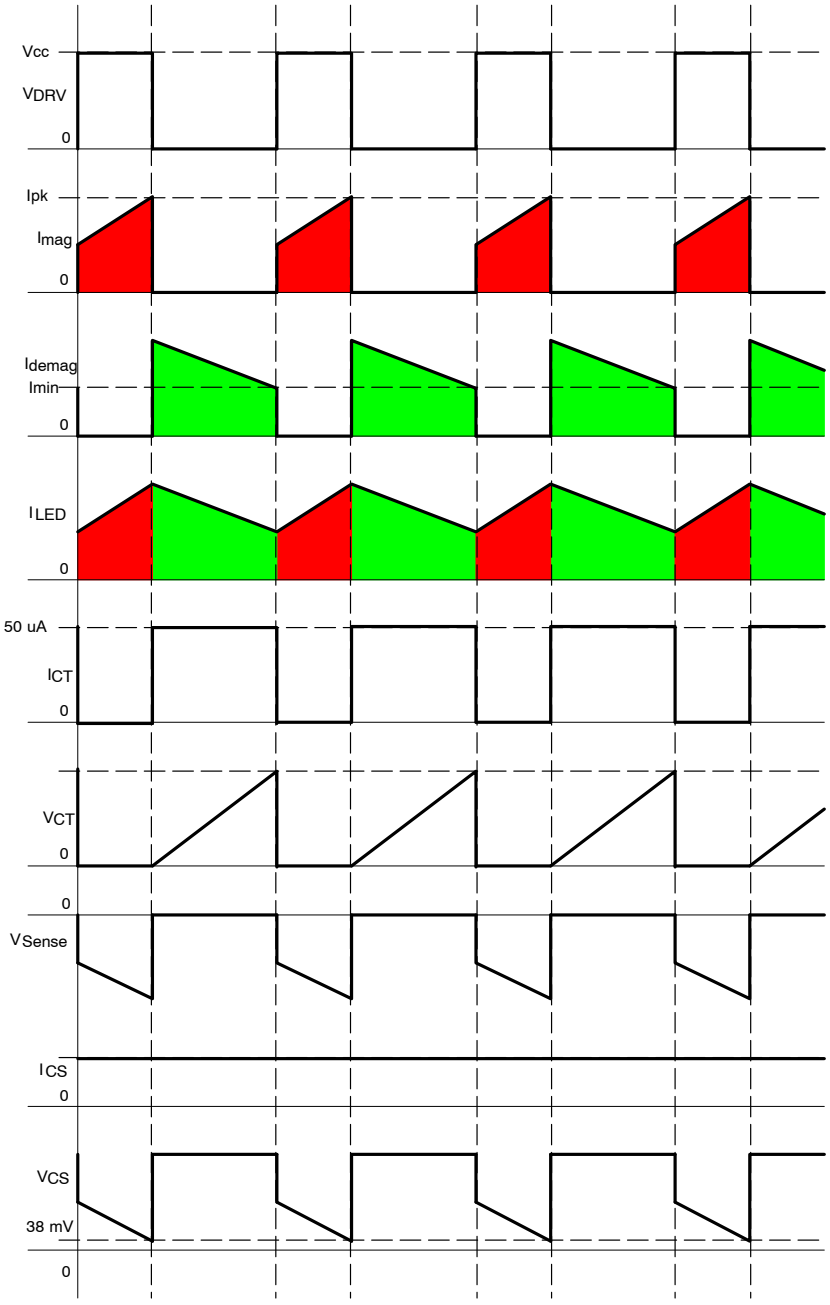


Figure 24. Voltage and Current Nodes in the Application Circuit

The current follows the red line in Figure 23 when Q1 is turned on. The converter operates in continuous conduction mode therefore the current through the inductor never goes to zero. When the switch is on, the current creates a negative voltage drop on the R_{sense} resistor. This negative voltage can not be measured directly by the IC so an R_{shift} resistor is connected to CS pin. Inside the IC there is a current source connected to this pin. This current source creates constant voltage drop on resistor R_{sense} which shifts the negative voltage drop presented on R_{sense} positive. The magnetizing current I_{mag} increases linearly, the negative voltage on R_{sense} increased as well. Thus the voltage on CS pin approaching zero. On the CS pin there is a comparator with a reference level of 38 mV. Once the voltage on the CS pin reaches this reference level, the DRV output is turned off and current path I_{mag} disappears. Energy stored in the inductor as a magnetic field keeps current flowing in the same direction. The current path is now closed via diode D1 (green line). Once the DRV is turned off, the internal current source starts to charge the CT capacitor and the voltage on this node increases. Once the CT capacitor voltage reaches the V_{CT} level, Q1 is turned on and an internal switch discharges the CT capacitor to be ready for the next switching cycle.

Application Design Example:

A typical step down application will be used to illustrate the basic design process based on nominal design parameters:

- Input voltage: V_{in} − 12 Vac (12 V dc after the bridge)
- Nominal LED current: 700 mA (rms)
- LED_{ripple}: 120 mA (peak−to−peak)
- V_{LED}: 3.2 V
- Freewheel diode V_f: 0.5 V
- Target Switching Frequency: 450 kHz

Dimming using PWM signal 1 kHz with duty cycle 0 – 99%

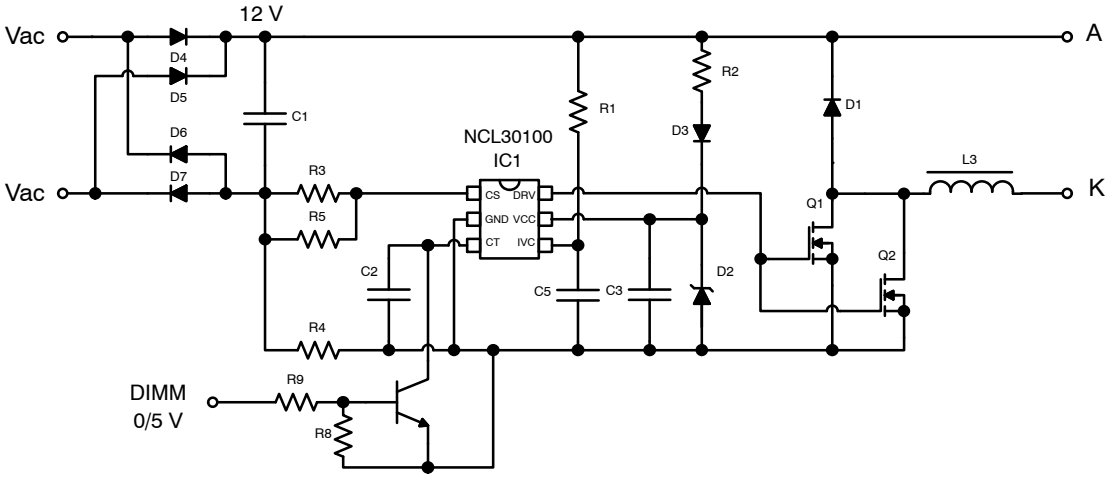


Figure 25. Example Design Schematic

Note this simplified step−by−step design process neglects any parasitic contribution of the PCB.

First, we need to determine the nominal t_{ON}/t_{OFF} ratio:

$$\frac{t_{on}}{t_{off}} = \frac{V_{LED} + V_f}{V_{in} - V_{LED}} = \frac{3.2 + 0.5}{12 - 3.2} = \frac{3.7}{8.8} \quad \text{(eq. 7)}$$

Next the typical duty cycle (DC) will be calculated:

$$DC = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{3.7}{3.7 + 8.8} = 0.296 \quad \text{(eq. 8)}$$

Target switching frequency is set at 450 kHz, now we need to determine the period:

$$T = \frac{1}{f_{op}} = \frac{1}{450 \cdot 10^3} = 2.222\ \mu s \quad \text{(eq. 9)}$$

Combination the previous equation we can calculate the t_{ON} and t_{OFF} durations:

$$t_{ON} = DC \cdot T = 0.296 \cdot 2.222 \cdot 10^{-6} = 658\ ns \quad \text{(eq. 10)}$$

$$t_{OFF} = (1 - DC) \cdot T = (1 - 0.296) \cdot 2.222 \cdot 10^{-6} = 1.564\ \mu s$$

Now all the parameters are defined to calculate inductor value:

$$V = \frac{di \cdot L}{dt} \Rightarrow L = \frac{(V_{IN} - V_{LED}) \cdot t_{ON}}{I_{ripple}} = \frac{(12 - 3.2) \cdot 658 \cdot 10^{-9}}{0.12} \cong 48.3\ \mu H \quad \text{(eq. 11)}$$

A standard value 47 μH is chosen.

Next the CT capacitor can be calculated, but we need to first determine the IVC current which can be simply calculated.

$$I_{IVC} = \frac{V}{R + R_{IVC}} = \frac{12}{1.5 \cdot 10^6 + 17 \cdot 10^3} \cong 7.91\ \mu A \quad \text{(eq. 12)}$$

The IVC current controls the dependence of the peak current to the input voltage. If the input voltage is well regulated, the IVC pin should be grounded. The value for IVC resistor should be chosen based on graphs below.

Note as well that the IVC can be used to implement analog dimming since increasing the current into IVC pin will decrease the I_{peak} of the LED).

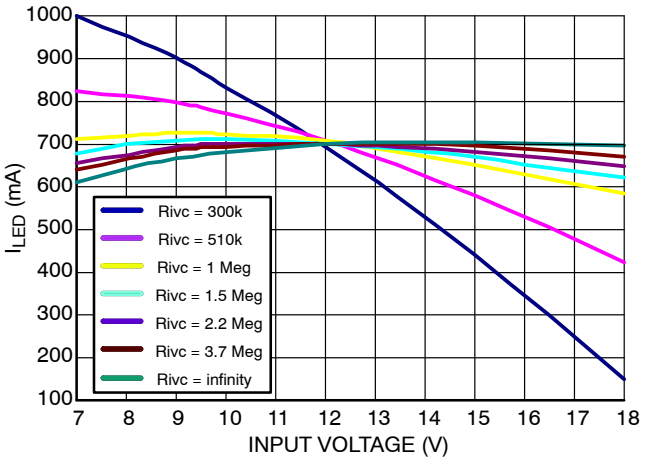


Figure 26. R_{ivc} Impact versus V_{in} for I_{LED} = 700 mA Nominal

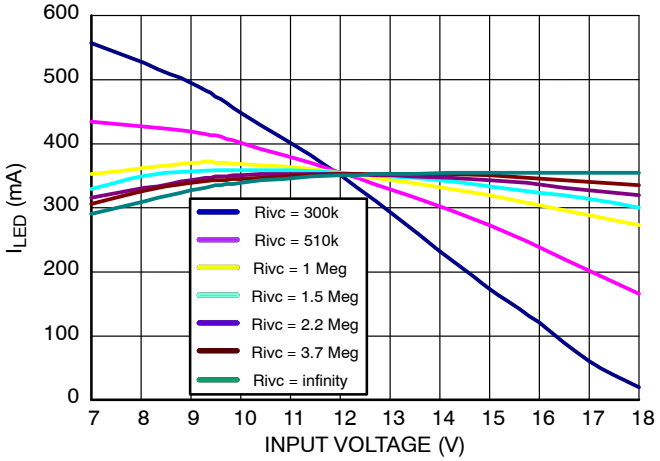


Figure 27. Rivc Impact versus V_{in} for I_{LED} = 350 mA Nominal

A value 1.5 MΩ was used since the input voltage has a sinusoidal component due to the low voltage AC input and desires to have a small bulk capacitance, thus compensating for part of this variation.

The dependence of V_{CT} on IVC current is described by the following equation:

$$V_{CT} = \frac{-0.097 \cdot X^2 + 24.5 \cdot X + 1358.1}{976.8} \text{ [V]} \quad \text{(eq. 13)}$$

Using the result from Equation 12 and put it to Equation 13 the V_{CT} threshold will be calculated:

$$V_{CT} = \frac{-0.097 \cdot 7.91^2 + 24.5 \cdot 7.91 + 1358.1}{976.8} \cong 1.58 \text{ V} \quad \text{(eq. 14)}$$

The CT capacitance can be calculated using the equations above:

$$I = \frac{dv \cdot C}{dt} \Rightarrow C_{CT} = \frac{I_{CT} \cdot \left(t_{OFF} - CT_{delay}\right)}{V_{CT}} \quad \text{(eq. 15)}$$

$$= \frac{50 \cdot 10^{-6} \cdot \left(1.654 \cdot 10^{-6} - 220 \cdot 10^{-9}\right)}{1.58} \cong 45.8 \text{ pF}$$

The intrinsic pin capacitance CT pin (~8 pF) in conjunction with the dimming transistor (~10 pF) in this schematic approximately 18 pF so this value must be subtracted from the calculated value in Equation 15. The calculated value is not standard, so the nearest value 33 pF has been selected.

Now we can calculate the I_{PK} of LED. The average value is set to 700 mA and the target ripple is set at 120 mA, the I_{PK} equals 760 mA. R_{shift} has been chosen to be as small a voltage drop as possible to minimize power dissipation so an R_{shift} of 100 mΩ has been selected.

Before calculation of R_{shift} we need to know the I_{CS} current, which affects the offset on R_{shift}. The I_{CS} value dependents on the IVC current and for IVC currents between 0 – 50 μA, it can be described by this formula:

$$I_{CS} = -0.75 \cdot IVC + 50 \cdot 10^{-6} \text{ [μA]} \quad \text{(eq. 16)}$$

Therefore:

$$I_{CS} = -0.75 \cdot IVC + 50 \cdot 10^{-6} \quad \text{(eq. 17)}$$

$$= -0.75 \cdot 7.91 \cdot 10^{-6} + 50 \cdot 10^{-6} \cong 44.07 \text{ μA}$$

To calculate R_{shift} it is necessary to know the I_{pk} current through the inductor. From the time that the current sense comparator detects that the peak current threshold has been crossed to the time that the external MOSFET switch is turned off there is a propagation delay. Depending on the value of the inductor selected (which is based on the target switching frequency), there is a current error between the intended peak current and the actual peak current, this is illustrated in Figure 28.

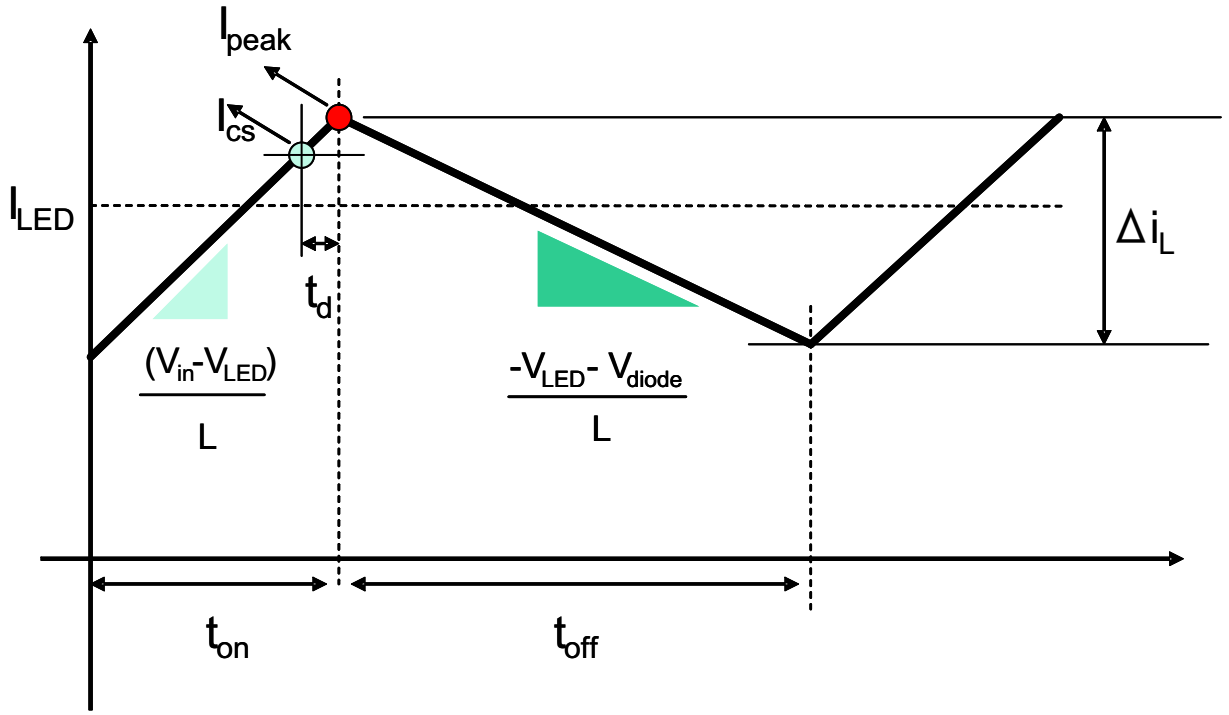


Figure 28. A Current Error Between the Intended Peak Current and the Actual Peak Current

$$V = \frac{di \cdot L}{dt} \Rightarrow I_{delay} = \frac{V \cdot t}{L} = \frac{8.8 \cdot 215 \cdot 10^{-9}}{47 \cdot 10^{-6}} \cong 0.0402\ A \quad \text{(eq. 18)}$$

V/L is simply the slew rate through the inductor and t_d is the internal propagation delay so the current overshoot from target is approximately 40 mA as calculated in Equation 18.

All values necessary for R_{shift} calculation are known, the R_{shift} value is described by this formula:

$$R_{shift} = \frac{R_{sense} \cdot \left(I_{pk} - I_{delay}\right) + V_{th}}{I_{CS}} = \frac{0.1 \cdot (0.76 - 0.0402) + 0.038}{44.07 \cdot 10^{-6}} \cong 2496\ \Omega \quad \text{(eq. 19)}$$

This value of resistance can be a parallel combination of 2.7 kΩ and 30 kΩ.

To understand the operating junction temperature, we calculate the die power dissipation:

$$P_{DIE} = V_{CC} \cdot \left(300 \cdot 10^{-6} + C_{MOSFET} \cdot V_{CC} \cdot f_{switching}\right) = 12 \cdot \left(300 \cdot 10^{-6} + 560 \cdot 10^{-12} \cdot 12 \cdot 450 \cdot 10^{3}\right) = 39.8\ mW \quad \text{(eq. 20)}$$

Using the P_{DIE}, we can calculate junction temperature:

$$Temp_{IC} = T_A + P_{DIE} \cdot R_{\theta JA} = T_A + 0.0399 \cdot 178 = T_A + 7.1^{\circ}C \quad \text{(eq. 21)}$$

A design spreadsheet to aid in calculating the external components necessary for a specific set of operating conditions is available for download at the ON Semiconductor website.

For a low voltage AC input diode D3 is placed into the Vcc line. Since Capacitor C3 is charged from a sinusoidal voltage. If the input voltage approaches zero, the IC is still supplied from C3. Due to this diode, the IC keeps the LED driver operating even if the sinusoidal voltage is lower than $V_{CC(min)}$ until V_{in} is lower than V_{LED}. The use of this diode make sense only if a single LED is used and the converter is supplied by sinusoidal voltage 12 Vac. For two LEDs in series their forward voltage is almost as high as $V_{CC(min)}$ of the IC.

Parasitic capacitance and inductance are presented in real applications which will have an influence on the circuit operation. They are depending on the PCB design which is user dependent. The BOM, PCB and some plots are enclosed for better understanding of the system behavior.

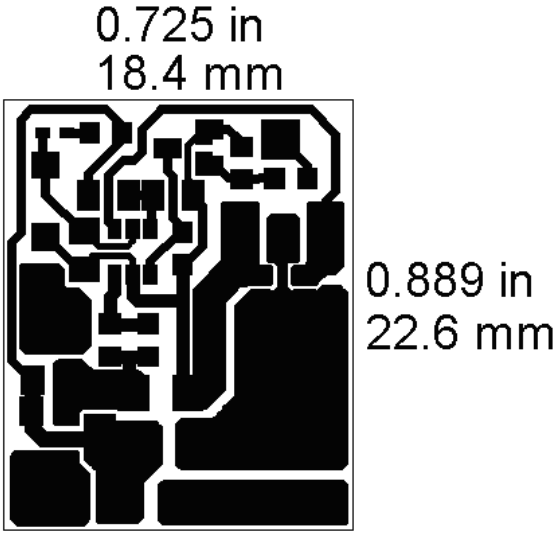


Figure 29. PCB Design the Circuit Calculated Above. Only Single Layer PCB is Used for the Application.

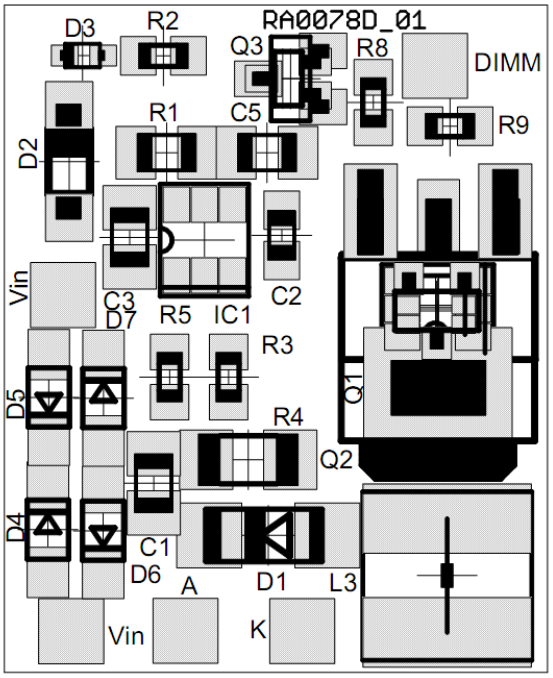


Figure 30. The Component Side (Several Transistor Packages are Possible to Use)

BILL OF MATERIALS FOR THE SINGLE LAYER EVALUATION BOARD (NCL30100ASLDGEVB)

Des-ignat-or	Qty	Descrip-tion	Value	Tol	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Pb−Free	Com-ments
C1	1	Capacitor	2.2 μF / 25 V	10%	0805	AVX	08053C225KAT2A	Yes	Yes	
C2	1	Capacitor	33 pF	5%	0603	Kemet	C0603C330J5GACTU	Yes	Yes	
C3	1	Capacitor	4.7 μF / 25 V	10%	0805	AVX	08053D475KAT2A	Yes	Yes	
C5	1	Capacitor	1 nF	10%	0603	Kemet	C0603C104K5RACTU	Yes	Yes	
D1	1	Surface Mount Schottky Power Rectifier	MBR130T3G	–	SOD−123	ON Semiconductor	MBR130T3G	No	Yes	
D2	1	Zener Diode	16 V	5%	SOD−123	ON semiconductors	MMSZ16T1G	No	Yes	
D3	1	Schottky Diode	NSR0520V2T1G	–	SOD−523	ON semiconductors	NSR0520V2T1G	No	Yes	
D4, D5, D6, D7	4	Schottky Diode	NSR0340HT1G	–	SOD−323	ON semiconductors	NSR0340HT1G	No	Yes	
IC1	1	LED Driver	NCL30100	–	TSOP−6	ON semiconductors	NCL30100SNT1G	No	Yes	
L3	1	Inductors	47 μH	10%	WE−PD2_M	Wurth Electronik	744774147	No	Yes	
Q1	1	Power MOSFET	NTGS4141NT1G	–	TSOP−6	ON semiconductors	NTGS4141NT1G	No	Yes	
Q2	1	Power MOSFET	NU	–	SOT−223	ON semiconductors	NTF3055−100T1G	No	Yes	Option
Q2	1	Power MOSFET	NU	–	DPAK	ON semiconductors	NTD23N03RT4G	No	Yes	Option
Q2	1	Power MOSFET	NU	–	SOT−363	ON semiconductors	NTJS4160NT1G	No	Yes	Option
Q2	1	Power MOSFET	NU	–	SOT−23	ON semiconductors	NTR4170NT1G	No	Yes	Option
Q3	1	General Purpose Transistor NPN	BC817−16	–	SOT−23	ON semiconductors	BC817−16LT1G	No	Yes	

BILL OF MATERIALS FOR THE SINGLE LAYER EVALUATION BOARD (NCL30100ASLDGEVB)

Des-ignat-or	Qty	Descrip-tion	Value	Tol	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Pb−Free	Com-ments
Q3	1	Power MOSFET	NU	−	SOT−23	ON semiconductors	NTS4001NT1G	No	Yes	Option
R1	1	Resistor	1.5 M	1%	0603	Rohm Semiconductor	MCR03EZPFX1504	Yes	Yes	
R2	1	Resistor	300 R	1%	0603	Rohm Semiconductor	MCR03EZPFX3000	Yes	Yes	
R3	1	Resistor	30 k	1%	0603	Rohm Semiconductor	MCR03EZPFX3002	Yes	Yes	
R4	1	Resistor	0.1 R	1%	0805	Welwyn	LRCS0805−0R1FT5	Yes	Yes	
R5	1	Resistor	2.7 k	1%	0603	Rohm Semiconductor	MCR03EZPFX2701	Yes	Yes	
R8	1	Resistor	10 k	1%	0603	Rohm Semiconductor	MCR03EZPFX1002	Yes	Yes	
R9	1	Resistor	5.6 k	1%	0603	Rohm Semiconductor	MCR03EZPFX5601	Yes	Yes	

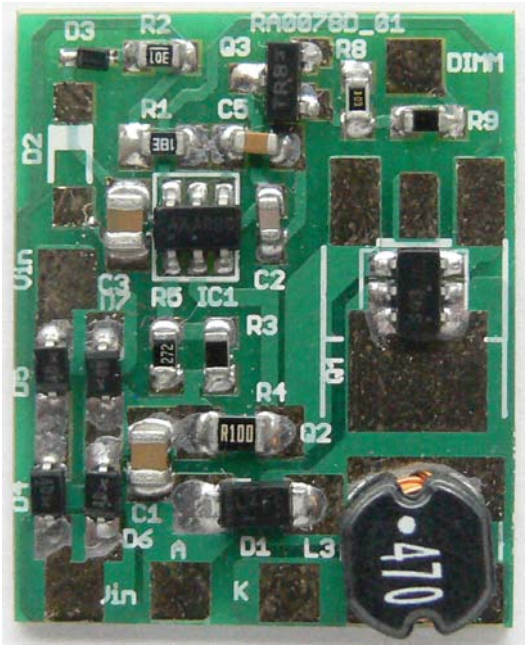


Figure 31. Completed PCB with Devices

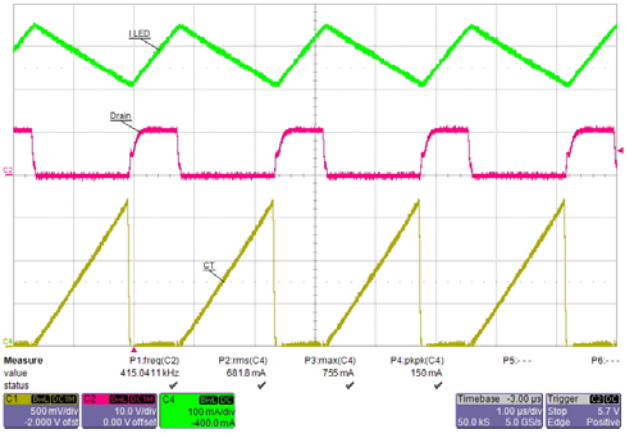


Figure 32. Snapshot of CT Pin Voltage, Driver and ILED

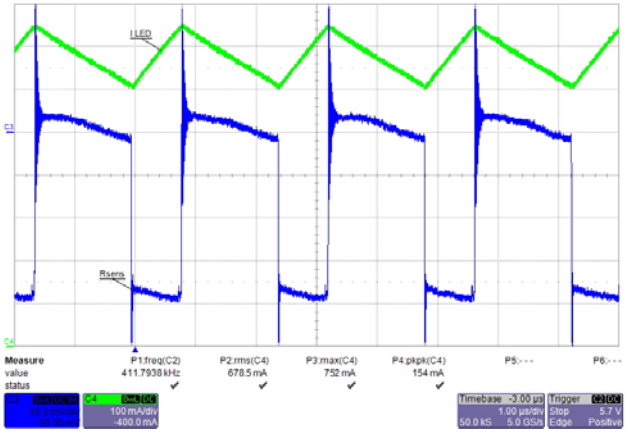


Figure 33. Voltage Measured on R_{CS} (R4)

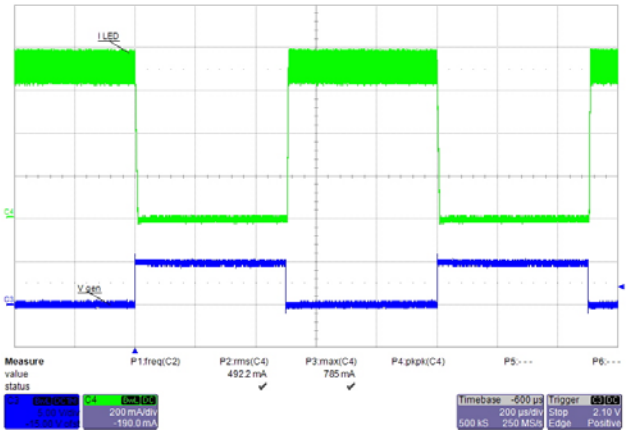


Figure 34. Current Through LED if 50% Dimming at 1 kHz is Applied

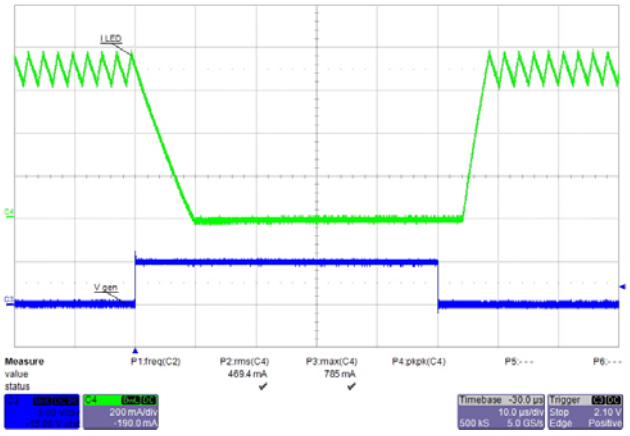


Figure 35. The Dimming Detail at 95%. No Overshoot in LED Current is Observed

Figures 36 and 37 illustrate leading edge and trailing edge waveforms from a chopped AC source. For proper dimming control, the bulk capacitance must be reduced to a relatively small value to achieve best dimming range. Performance in real world application is dependent on the characteristics of the actual dimmer and the electronic transformer used to generated to chopped AC waveform

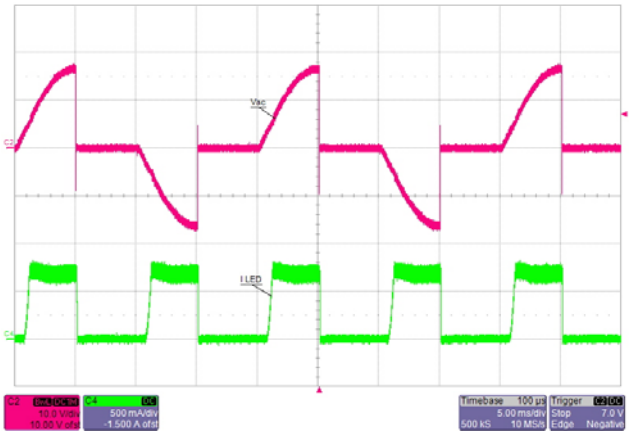


Figure 36. Trailing Edge Dimming

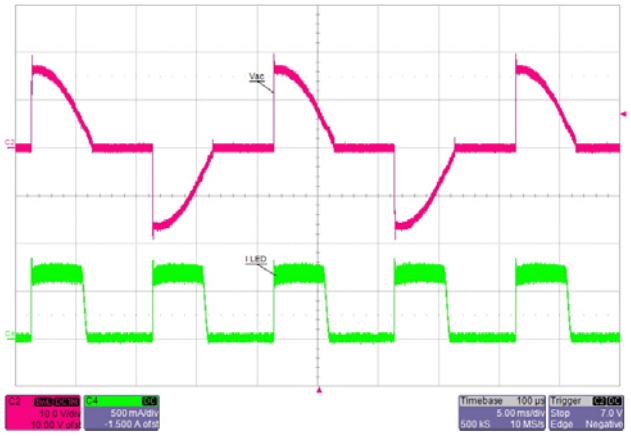


Figure 37. Leading Edge (Triac) Regulation. Small Overshoot is Seen on the Leading Edge, this is Based on the Abrupt Chopping of the Low Voltage AC Waveform

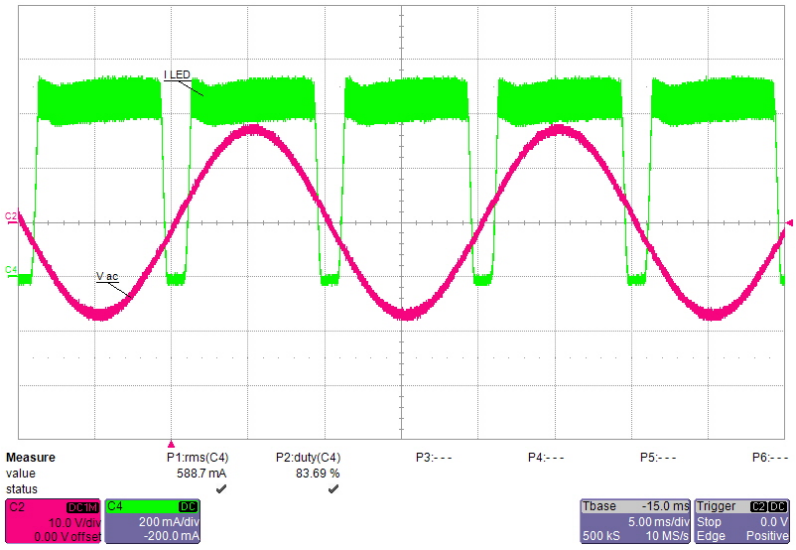


Figure 38. ILED and Vin Waveform if No Dimming is Used

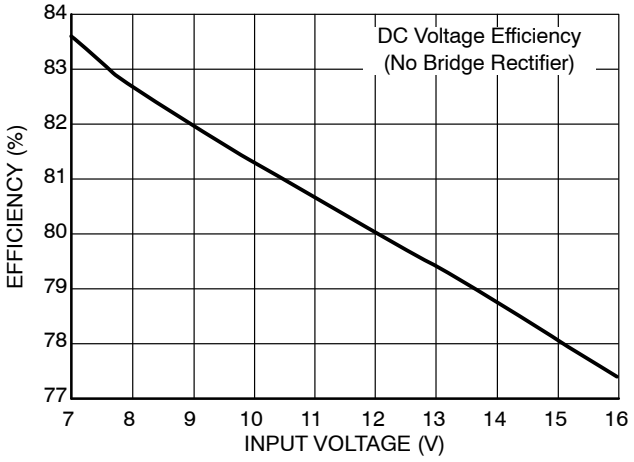


Figure 39. Efficiency Measurement for the Demoboard (V_f = 3.2 Nominal)

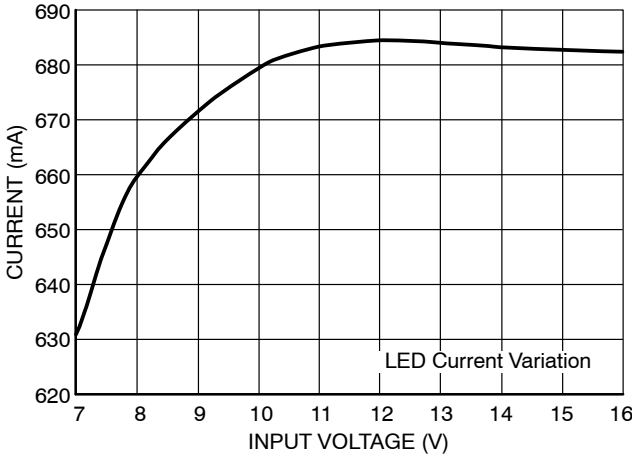


Figure 40. I_{LED} Current Dependence on Input DC Voltage (No Bridge Rectifier is Used)

Figure 39 represents the efficiency of the converter driving a single LED at a nominal current of 690 mA. The addition of the AC bridge rectifier contributes addition losses into the circuit and it is recommended to us low forward voltage schottky rectifiers to minimize power dissipation in the AC rectification stage.

MR 16 Evaluation Board Information

A specific two sided demo board was designed to fit with the MR 16 form factor. The schematic is almost the same for both, but the PWM dimming control circuitry has been removed. If the same components are used, the operation frequency will be slightly higher due to the lower pin capacitance because the dimming transistor contribution is removed.

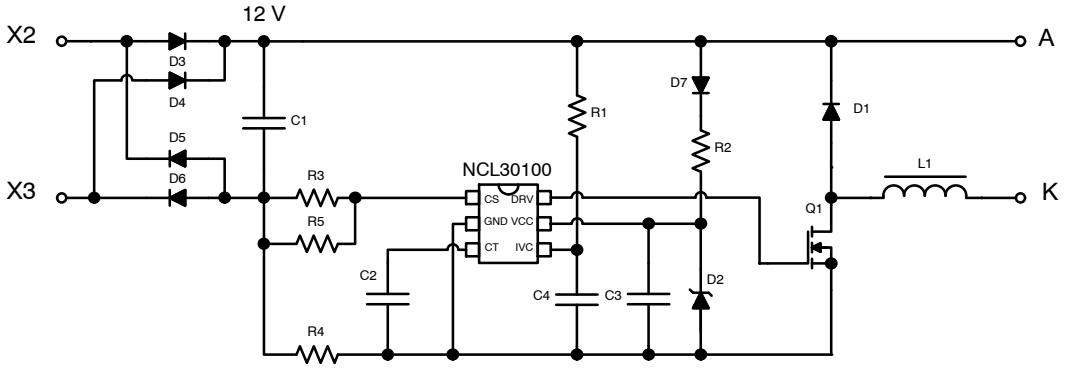


Figure 41. Schematic MR 16 Application

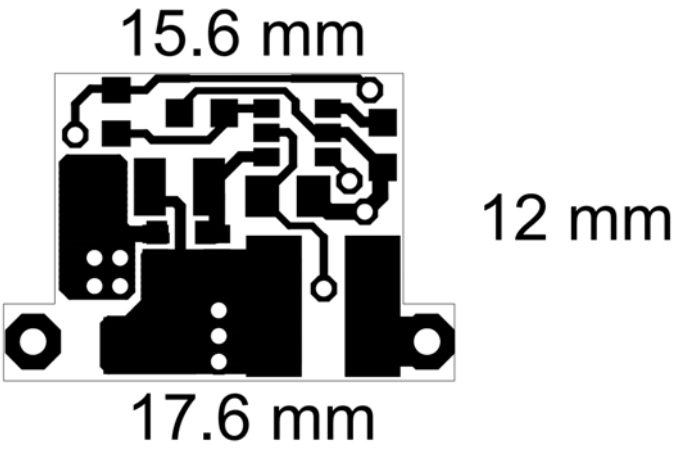


Figure 42. PCB Top Side MR 16 Application

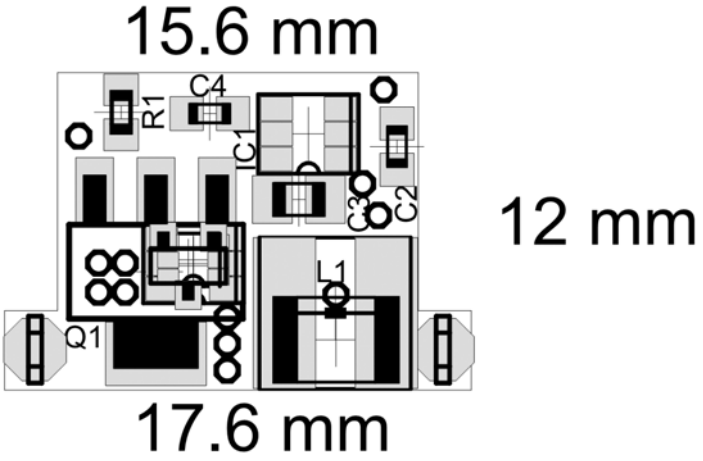


Figure 43. PCB Top Side Devices Placement

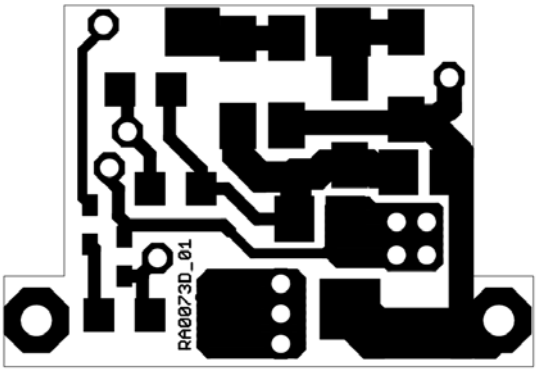


Figure 44. PCB Bottom Side MR 16 Application

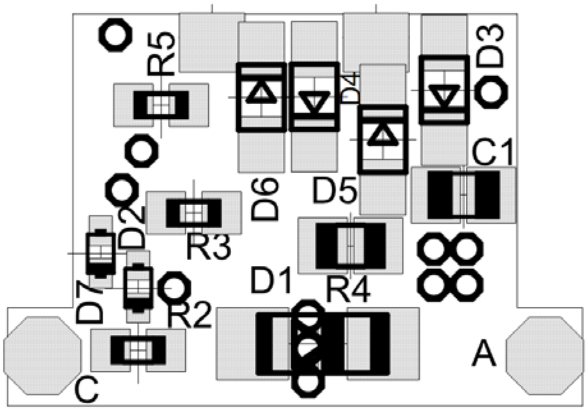


Figure 45. PCB Bottom Side Devices Placement

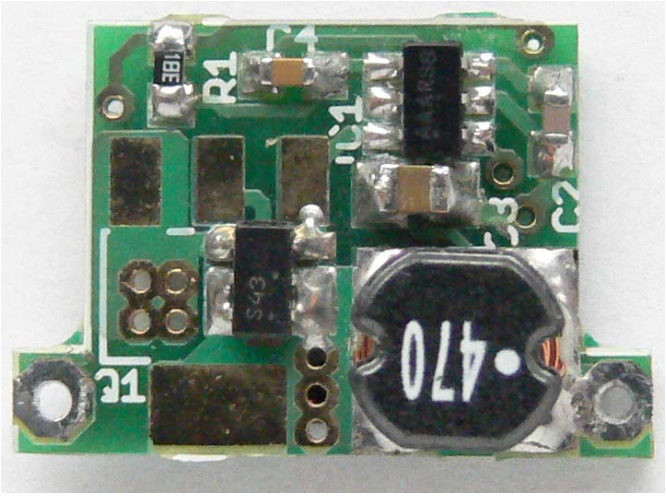


Figure 46. Top Side Photo

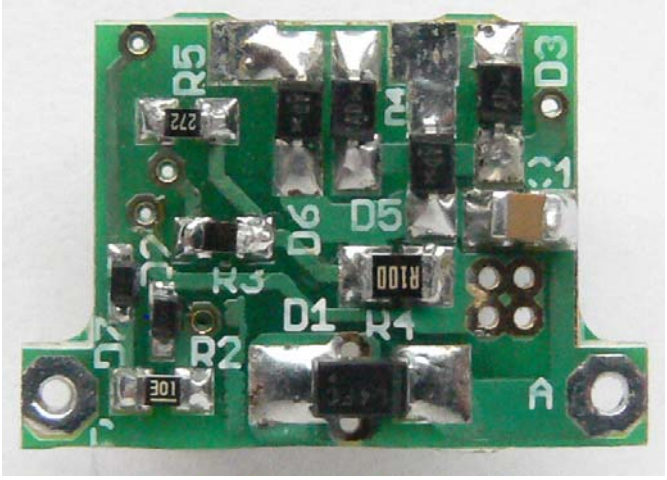


Figure 47. Bottom Side Photo

BILL OF MATERIALS FOR THE MR 16 EVALUATION BOARD (NCL30100ADLMGEVB)

Des-ignat-or	Qty	Descrip-tion	Value	Tol	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Pb−Free	Com-ments
C1	1	Capacitor	2.2 μF / 25 V	10%	0805	AVX	08053C225KAT2A	Yes	Yes	
C2	1	Capacitor	33 pF	5%	0603	Kemet	C0603C330J5GACTU	Yes	Yes	
C3	1	Capacitor	4.7 μF / 25 V	10%	0805	AVX	08053D475KAT2A	Yes	Yes	
C4	1	Capacitor	1 nF	10%	0603	Kemet	C0603C104K5RACTU	Yes	Yes	
D1	1	Surface Mount Schottky Power Rectifier	MBR130T3G	−	SOD−123	ON Semiconductor	MBR130T3G	No	Yes	
D2	1	Zener Diode	16 V	5%	SOD−523	ON Semiconductor	MM5Z16VT1G	No	Yes	
D3, D4, D5, D6	4	Schottky Diode	NSR0340HT1G	−	SOD−323	ON Semiconductor	NSR0340HT1G	No	Yes	
D7	1	Schottky Diode	NSR0520V2T1G	−	SOD−523	ON Semiconductor	NSR0520V2T1G	No	Yes	
IC1	1	LED Driver	NCL30100	−	TSOP−6	ON Semiconductor	NCL30100SNT1G	No	Yes	
L1	1	Inductors	47 μH	10%	WE−PD2_M	Wurth Electronik	744774147	No	Yes	
Q1	1	Power MOSFET	NTGS4141NT1G	−	TSOP−6	ON Semiconductor	NTGS4141NT1G	No	Yes	
Q1	1	Power MOSFET	NU	−	SOT−223	ON Semiconductor	NTF3055−100T1G	No	Yes	Option
Q1	1	Power MOSFET	NU	−	SOT−363	ON Semiconductor	NTJS4160NT1G	No	Yes	Option
Q1	1	Power MOSFET	NU	−	SOT−23	ON Semiconductor	NTR4170NT1G	No	Yes	Option
R1	1	Resistor	1.5 M	1%	0603	Rohm Semiconductor	MCR03EZPFX1504	Yes	Yes	
R2	1	Resistor	300 R	1%	0603	Rohm Semiconductor	MCR03EZPFX3000	Yes	Yes	
R3	1	Resistor	30 k	1%	0603	Rohm Semiconductor	MCR03EZPFX3002	Yes	Yes	
R4	1	Resistor	0.1 R	1%	0805	Welwyn	LRCS0805−0R1FT5	Yes	Yes	
R5	1	Resistor	2.7 k	1%	0603	Rohm Semiconductor	MCR03EZPFX2701	Yes	Yes	

Application Design Example for an Offline (115 Vac) Buck Application:

In addition to traditional DC−DC applications, the NCL30100 can also be used in offline applications, a schematic and PCB layout are provided to illustrate a typical circuit configuration.

- Input voltage: V_{in} − 115 Vac
- Nominal LED current: 700 mA (rms)
- LED_{ripple}: 120 mA (peak−to−peak)
- V_{LED}: 3.2 V
- Freewheel diode V_f: 0.5 V
- Target Switching Frequency: 50 kHz

Dimming using PWM signal 1 kHz with duty cycle 0 – 99%

In this application example, there is schematic and PCB only. The design steps are the same as above mentioned.

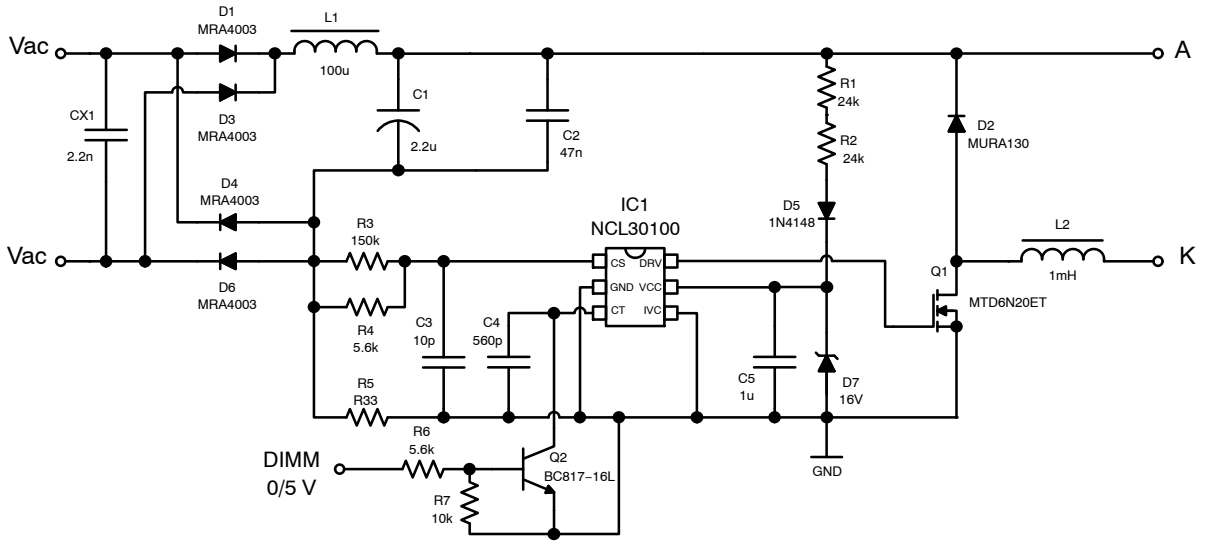


Figure 48. Design Example Schematic of 115 Vac Converter

The input voltage in range 85−140 Vac is rectified by bridge rectifier D1, D3, D4 and D6. To limit current peaks generated during on time period, capacitor C1 is used. CX1, C2 and L1 are an EMI filter to protect mains against current spikes mainly generated by D2 if Q1 is turned on. The NCL30100 is powered through resistors R1 and R2. The Vcc voltage is limited by D7. Maximum LED current is set by resistors R3, R4 and R5. In this case Rsense is 0.33 Ω to reach higher accuracy. A small capacitor C3 is used to filter out spikes which are generated during the turn off of diode D2. It is recommended to use L2 with low series resistance since current is flowing through the inductor continuously and D2 should be selected for low forward voltage drop and fast reverse recovery time.

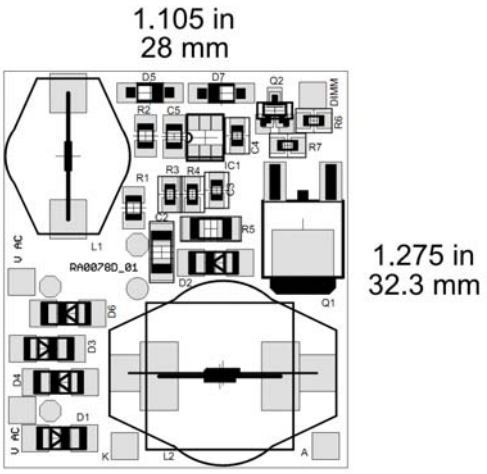


Figure 49. Component Side

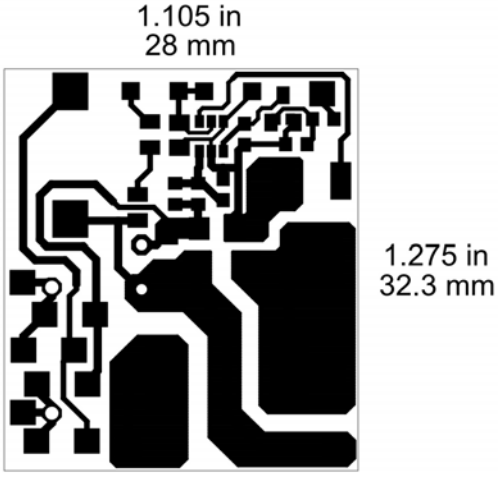


Figure 50. Single Layer PCB Design for this Application

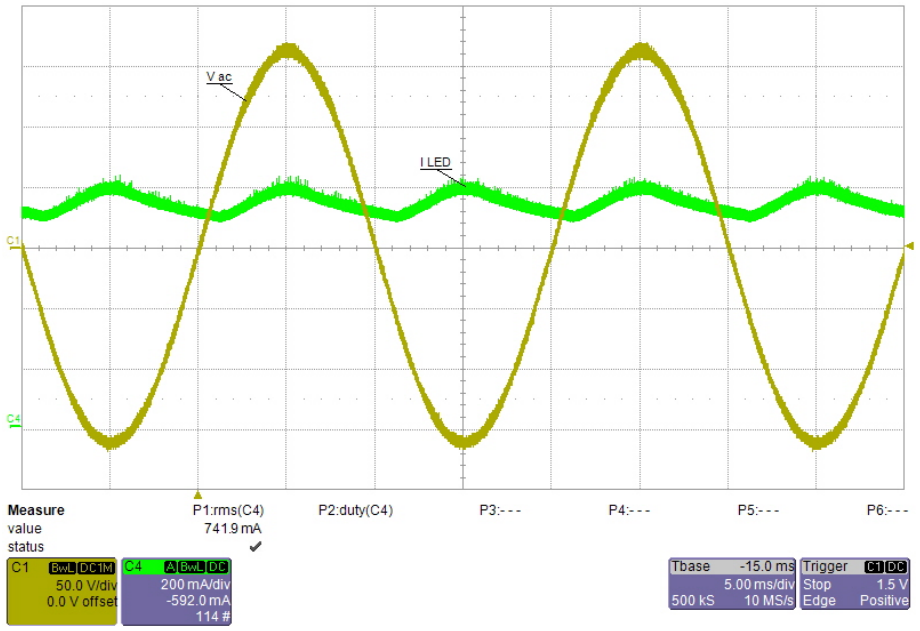


Figure 51. ILED and V_{in} Waveform

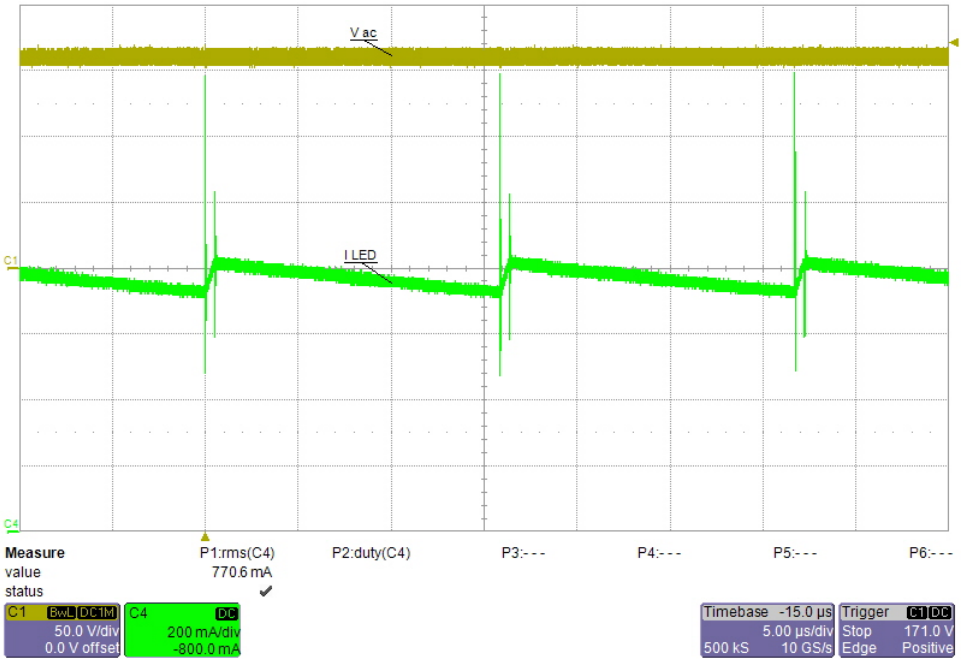


Figure 52. ILED at the Peak of Sinusoidal Voltage

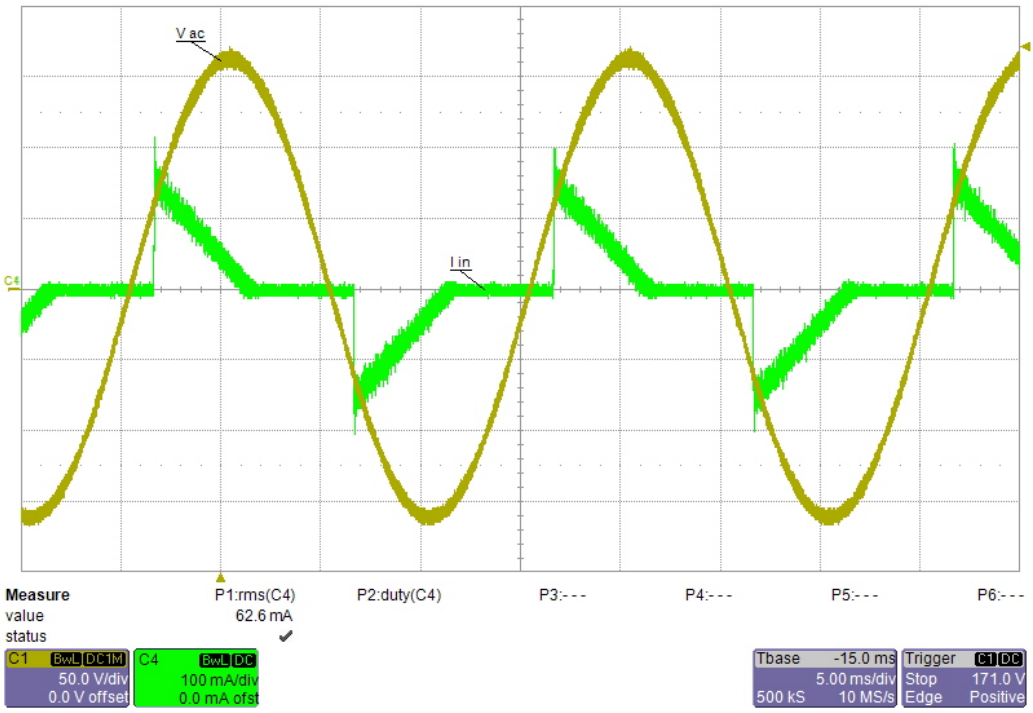
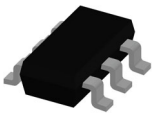


Figure 53. Input Voltage and Input Current

BILL OF MATERIALS FOR THE NCL30100 115 Vac

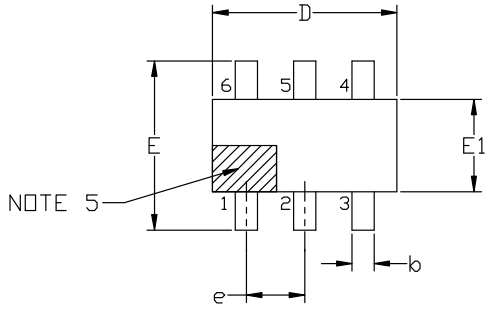
Des-ignat-or	Qty	Description	Value	Tol	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Pb−Free	Com-ments
C1	1	Capacitor	2.2 μF / 200 V	10%	E3.5−8	Koshin	KR1 2.2u 200V 8X11.5	Yes	Yes	
C2	1	Capacitor	47 nF	10%	1206	Yageo	CC1206KKX7RABB473	Yes	Yes	
C3	1	Capacitor	10 pF	5%	0603	Kemet	C0603C100J5GACTU	Yes	Yes	
C4	1	Capacitor	560 pF	5%	0603	Kemet	C0603C561J5GACTU	Yes	Yes	
C5	1	Capacitor	1 μF / 25 V	10%	0805	AVX	08053D105KAT2A	Yes	Yes	
D1, D3, D4, D6	4	Standard Recovery Power Rectifier	MRA4003T3G	−	SMA	ON Semiconductor	MRA4003T3G	No	Yes	
D2	1	Ultrafast Power Rectifier	MURA130T3G	−	SMA	ON Semiconductor	MURA130T3G	No	Yes	
D5	1	Standard Diode	MMSD4148	−	SOD−123	ON Semiconductor	MMSD4148T1G	No	Yes	
D7	1	Zener Diode	16 V	5%	SOD−123	ON Semiconductor	MMSZ16VT1G	No	Yes	
IC1	1	LED Driver	NCL30100	−	TSOP−6	ON Semiconductor	NCL30100SNT1G	No	Yes	
L1	1	Inductors	100 μH	10%	WE−PD4_L	Wurth Electronik	7445620	No	Yes	
L2	1	Inductors	1 mH	10%	WE−PD_XXL	Wurth Electronik	7447709102	No	Yes	
Q1	1	Power MOSFET	MTD6N20	−	DPAK	ON Semiconductor	MTD6N20ET4G	No	Yes	
Q2	1	General Purpose Transistor NPN	BC817−16	−	SOT−23	ON Semiconductor	BC817−16LT1G	No	Yes	
Q2	1	Power MOSFET	NU	−	SOT−23	ON Semiconductor	NTS4001NT1G	No	Yes	Option
R1, R2	2	Resistor	24 k	1%	0806	Rohm Semiconductor	MCR06EZPFX2402	Yes	Yes	
R3	1	Resistor	150 k	1%	0603	Rohm Semiconductor	MCR03EZPFX1503	Yes	Yes	
R4, R6	2	Resistor	5.6 k	1%	0603	Rohm Semiconductor	MCR03EZPFX5601	Yes	Yes	
R5	1	Resistor	0.33 R	1%	0805	Welwyn	LRCS0805−0R33FT5	Yes	Yes	
R7	1	Resistor	10 k	1%	0603	Rohm Semiconductor	MCR03EZPFX1002	Yes	Yes	
CX1	1	EMI Suppression Capacitor	2.2 nF / 300 V	20%	XC10B5	Epcos	B32021A3222M289	Yes	Yes	

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

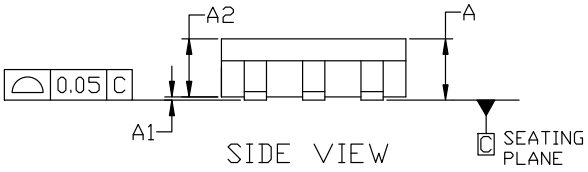


TSOP−6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

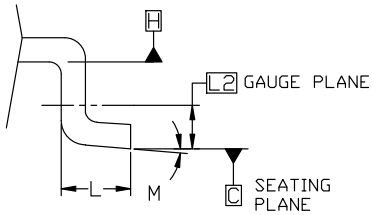
DATE 26 FEB 2024



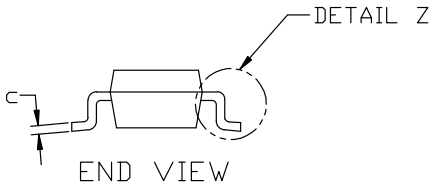
TOP VIEW



SIDE VIEW



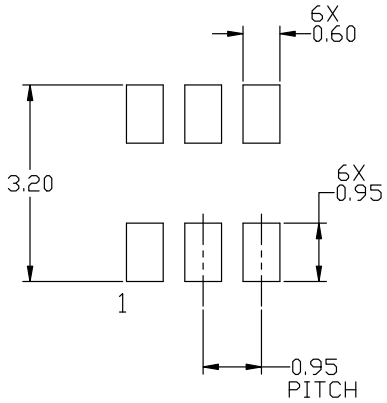
DETAIL Z
SCALE 3:1



END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

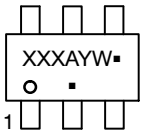
*For additional information on our Pb-Free strategy and soldering details, please download th e ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98ASB14888C**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**TSOP−6 3.00x1.50x0.90, 0.95P**		**PAGE 1 OF 2**

TSOP−6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

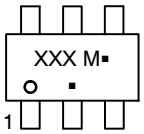
DATE 26 FEB 2024

GENERIC
MARKING DIAGRAM*



IC

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package



STANDARD

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

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