

3.3 V Differential Multipoint Low Voltage M-LVDS Driver Receiver

NB3N201S, NB3N206S



SOIC-8
 D SUFFIX
 CASE 751

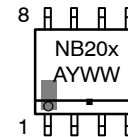
Description

The NB3N20xS Series are pure 3.3 V supply differential Multipoint Low Voltage (M-LVDS) line Drivers and Receivers. Devices NB3N201S and NB3N206S are TIA/EIA-899 compliant. NB3N201S offers the Type 1 receiver threshold at 0.0 V. NB3N206S offers the Type 2 receiver threshold at 0.1 V.

These devices have Type-1 and Type-2 receivers that detect the bus state with as little as 50 mV of differential input voltage over a common-mode voltage range of -1 V to 3.4 V. The Type-1 receivers have near zero thresholds (± 50 mV) and exhibit 25 mV of differential input voltage hysteresis to prevent output oscillations with slowly changing signals or loss of input. Type-2 receivers include an offset threshold to provide a detectable voltage under open-circuit, idle-bus, and other faults conditions.

NB3N201S and NB3N206S support Simplex or Half Duplex bus configurations.

MARKING DIAGRAM



- NB20x = Specific Device Code
- x = 1, 6
- A = Assembly Location
- Y = Year
- WW = Work Week
- G or ■ = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 18 of this data sheet.

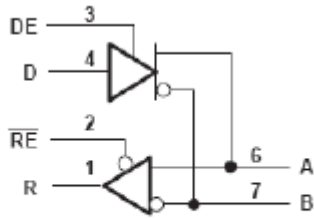
Features

- Low-Voltage Differential 30 Ω to 55 Ω Line Drivers and Receivers for Signaling Rates Up to 200 Mbps
- Type-1 Receivers Incorporate 25 mV of Hysteresis
- Type-2 Receivers Provide an Offset (100 mV) Threshold to Detect Open-Circuit and Idle-Bus Conditions
- Meets or Exceeds the M-LVDS Standard TIA/EIA-899 for Multipoint Data Interchange
- Controlled Driver Output Voltage Transition Times for Improved Signal Quality
- -1 V to 3.4 V Common-Mode Voltage Range Allows Data Transfer With up to 2 V of Ground Noise
- Bus Pins High Impedance When Disabled or $V_{CC} \leq 1.5$ V
- M-LVDS Bus Power Up/Down Glitch Free
- Operating range: $V_{CC} = 3.3 \pm 10\%$ V (3.0 to 3.6 V)
- Operation from -40°C to 85°C.
- These are Pb-Free Devices

Applications

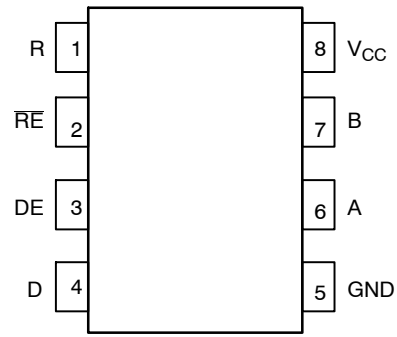
- Low-Power High-Speed Short-Reach Alternative to TIA/EIA-485
- Backplane or Cabled Multipoint Data and Clock Transmission
- Cellular Base Stations
- Central-Office Switches
- Network Switches and Routers

NB3N201S, NB3N206S



**SOIC 8:
NB3N201S, NB3N206S**

Figure 1. Logic Diagram



SOIC-8
NB3N201S, NB3N206S

Figure 2. Pinout Diagram
(Top View)

Table 1. PIN DESCRIPTION

| Number | Name | I/O Type | Open Default | Description |
|--------|------|----------------------|--------------|---|
| 1 | R | LVC MOS Output | | Receiver Output Pin |
| 2 | RE | LVC MOS Input | High | Receiver Enable Input Pin (LOW = Active, HIGH = High Z Output) |
| 3 | DE | LVC MOS Input | Low | Driver Enable Input Pin (LOW = High Z Output, HIGH=Active) |
| 4 | D | LVC MOS Input | | Driver Input Pin |
| 5 | GND | | | Ground Supply pin. Pin must be connected to power supply to guarantee proper operation. |
| 6 | A | M-LVDS Input /Output | | Transceiver True Input /Output Pin |
| 7 | B | M-LVDS Input /Output | | Transceiver Invert Input /Output Pin |
| 8 | VCC | | | Power Supply pin. Pin must be connected to power supply to guarantee proper operation. |

NB3N201S, NB3N206S

Table 2. DEVICE FUNCTION TABLE

| | | | | |
|--|---|-----------------|---------------|--------------|
| TYPE 1 Receiver (NB3N201/NB3N203) | Inputs | | Output | |
| | $V_{ID} = V_A - V_B$ | \overline{RE} | R | |
| | $V_{ID} \geq 50 \text{ mV}$ | L | H | |
| | $-50 \text{ mV} < V_{ID} < 50 \text{ mV}$ | L | ? | |
| | $V_{ID} \leq -50 \text{ mV}$ | L | L | |
| | X | H | Z | |
| | X | Open | Z | |
| | Open | L | ? | |
| TYPE 2 Receiver (NB3N206/NB3N207) | Inputs | | Output | |
| | $V_{ID} = V_A - V_B$ | \overline{RE} | R | |
| | $V_{ID} \geq 150 \text{ mV}$ | L | H | |
| | $50 \text{ mV} < V_{ID} < 150 \text{ mV}$ | L | ? | |
| | $V_{ID} \leq 50 \text{ mV}$ | L | L | |
| | X | H | Z | |
| | X | Open | Z | |
| | Open | L | L | |
| DRIVER | Input | Enable | Output | |
| | D | DE | A / Y | B / Z |
| | L | H | L | H |
| | H | H | H | L |
| | Open | H | L | H |
| | X | Open | Z | Z |
| | X | L | Z | Z |

H = High, L = Low, Z = High Impedance, X = Don't Care, ? = Indeterminate

NB3N201S, NB3N206S

Table 3. ATTRIBUTES (Note 1)

| Characteristics | | | Value |
|---|--|------------------------|-----------------------------------|
| ESD Protection | Human Body Model (JEDEC Standard 22, Method A114-A) | A, B, Y, Z All Pins | ±6 kV ±2 kV |
| | Machine Model | All Pins | ±200 V |
| | Charged –Device Model (JEDEC Standard 22, Method C101) | All Pins | ±1500 V |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | | | Level 1 |
| Flammability Rating Oxygen Index | | | UL-94 code V-0 A 1/8” 28 to 34 |
| Transistor Count | | | 917 Devices |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | | |

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 2)

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|------------------|--|-----------------|------------------------------|--|-------------------|
| V _{CC} | Supply Voltage | | | -0.5 ≤ V _{CC} ≤ 4.0 | V |
| V _{IN} | Input Voltage | D, DE, RE | | -0.5 ≤ V _{IN} ≤ 4.0 | V |
| | | A, B (201, 206) | | -1.8 ≤ V _{IN} ≤ 4.0 | |
| I _{OUT} | Output Voltage | R A, B | | -0.3 ≤ I _{OUT} ≤ 4.0 -1.8 ≤ I _{OUT} ≤ 4.0 | V |
| T _A | Operating Temperature Range, Industrial | | | -40 to ≤ +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm | SOIC-8 | 190 | °C/W °C/W |
| | | 500 lfpm | | 130 | |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | (Note 3) | SOIC-8 | 41 to 44 | °C/W |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm | SOIC-14 | 80 | °C/W °C/W |
| | | 500 lfpm | | | |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | (Note 3) | SOIC-14 | 36 | °C/W |
| T _{sol} | Wave Solder | | | 265 | °C |
| P _D | Power Dissipation (Continuous) | | T _A = 25°C | 725 | mW mW/°C mW |
| | | | 25°C < T _A < 85°C | 5.8 | |
| | | | T _A = 85°C | 377 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously.

If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.

3. JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

NB3N201S, NB3N206S

Table 5. DC CHARACTERISTICS $V_{CC} = 3.3 \pm 10\% V$ (3.0 to 3.6 V), $GND = 0 V$, $T_A = -40^\circ C$ to $+85^\circ C$ (See Notes 4, 5)

| Symbol | Characteristic | Min | Typ | Max | Unit | |
|-----------|---|------|---------------|---------------------|------|----|
| ICC | Power Supply Current Receiver Disabled Driver Enabled \overline{RE} and DE at V_{CC} , $R_L = 50 \Omega$, All others open Driver and Receiver Disabled RE at V_{CC} , DE at 0 V, $R_L =$ No Load, All others open Driver and Receiver Enabled RE at 0 V, DE at V_{CC} , $R_L = 50 \Omega$, All others open Receiver Enabled Driver Disabled RE at 0 V, DE at 0 V, $R_L = 50 \Omega$, All others open | | 13 1 16 | 22 4 24 13 | | mA |
| V_{IH} | Input HIGH Voltage | 2 | | V_{CC} | V | |
| V_{IL} | Input LOW Voltage | GND | | 0.8 | V | |
| V_{BUS} | Voltage at any bus terminal VA, VB, VY or VZ | -1.4 | | 3.8 | V | |
| VID | Magnitude of differential input voltage | 0.05 | | V_{CC} | | |

DRIVER

| | | | | | |
|---------------------|---|---------------|--|--------------|---------|
| $ V_{AB} $ | Differential output voltage magnitude (see Figure 4) | 480 | | 650 | mV |
| $\Delta V_{AB} $ | Change in Differential output voltage magnitude between logic states (see Figure 4) | -50 | | 50 | mV |
| $V_{OS(SS)}$ | Steady state common mode output voltage (see Figure 5) | 0.8 | | 1.2 | V |
| $\Delta V_{OS(SS)}$ | Change in Steady state common mode output voltage between logic states (see Figure 5) | -50 | | 50 | mV |
| $V_{OS(PP)}$ | Peak-to-peak common-mode output voltage (see Figure 5) | | | 150 | mV |
| V_{AOC} | Maximum steady-state open-circuit output voltage (see Figure 9) | 0 | | 2.4 | V |
| V_{BOC} | Maximum steady-state open-circuit output voltage (see Figure 9) | 0 | | 2.4 | V |
| $V_{P(H)}$ | Voltage overshoot, low-to-high level output (see Figure 7) | | | $1.2 V_{SS}$ | V |
| $V_{P(L)}$ | Voltage overshoot, high-to-low level output (see Figure 7) | $-0.2 V_{SS}$ | | | V |
| I_{IH} | High-level input current (D, DE) $V_{IH} = 2 V$ | 0 | | 10 | μA |
| I_{IL} | Low-level input current (D, DE) $V_{IL} = 0.8 V$ | 0 | | 10 | μA |
| I_{OSJ} | Differential short-circuit output current magnitude (see Figure 6) | | | 24 | mA |
| I_{OZ} | High-impedance state output current (driver only) $-1.4 V \leq (VA \text{ or } VB) \leq 3.8 V$, other output at 1.2 V | -15 | | 10 | μA |
| $I_{O(OFF)}$ | Power-off output current ($0 V \leq V_{CC} \leq 1.5 V$) $-1.4 V \leq (VA \text{ or } VB) \leq 3.8 V$, other output at 1.2 V | -10 | | 10 | μA |

RECEIVER

| | | | | | |
|-------------|--|-----------|---------|-----------|---------|
| V_{IT+} | Positive-going Differential Input voltage Threshold (See Figure 11 & Tables 8 and 9) Type 1 Type 2 | | | 50 150 | mV |
| V_{IT-} | Negative-going Differential Input voltage Threshold (See Figure 11 & Tables 8 and 9) Type 1 Type 2 | -50 50 | | | mV |
| V_{HYS} | Differential Input Voltage Hysteresis (See Figure 11 and Table 2) Type 1 Type 2 | | 25 0 | | mV |
| VOH | High-level output voltage ($I_{OH} = -8 \text{ mA}$) | 2.4 | | | V |
| VOL | Low-level output voltage ($I_{OL} = 8 \text{ mA}$) | | | 0.4 | V |
| I_{IH} | \overline{RE} High-level input current ($V_{IH} = 2 V$) | -10 | | 0 | μA |
| I_{IL} | \overline{RE} Low-level input current ($V_{IL} = 0.8 V$) | -10 | | 0 | μA |
| I_{OZ} | High-impedance state output current ($V_O = 0 V$ of 3.6 V) | -10 | | 15 | μA |
| C_A / C_B | Input Capacitance $V_I = 0.4 \sin(30E^6\pi t) + 0.5 V$, other outputs at 1.2 V using HP4194A impedance analyzer (or equivalent) | | 3 | | pF |
| C_{AB} | Differential Input Capacitance $V_{AB} = 0.4 \sin(30E^6\pi t) V$, other outputs at 1.2 V using HP4194A impedance analyzer (or equivalent) | | | 2.5 | pF |
| $C_{A/B}$ | Input Capacitance Balance, (C_A/C_B) | 99 | | 101 | % |

NB3N201S, NB3N206S

Table 5. DC CHARACTERISTICS VCC = 3.3 ±10% V (3.0 to 3.6 V), GND = 0 V, TA = -40°C to +85°C (See Notes 4, 5)

| Symbol | Characteristic | Min | Typ (Note 5) | Max | Unit |
|-----------------------------|---|-----------------|--------------|---------------|------|
| BUS INPUT AND OUTPUT | | | | | |
| IA | Input Current Receiver or Transceiver with Driver Disabled VA = 3.8 V, VB = 1.2 V VA = 0.0 V or 2.4 V, VB = 1.2 V VA = -1.4 V, VB = 1.2 V | 0 -20 -32 | | 32 20 0 | uA |
| IB | Input Current Receiver or Transceiver with Driver Disabled VB = 3.8 V, VA = 1.2 V VB = 0.0 V or 2.4 V, VA = 1.2 V VB = -1.4 V, VA = 1.2 V | 0 -20 -32 | | 32 20 0 | uA |
| IAB | Differential Input Current Receiver or Transceiver with driver disabled (IA-IB) VA = VB, -1.4 ≤ VA ≤ 3.8 V | -4 | | 4 | uA |
| IA(OFF) | Input Current Receiver or Transceiver Power Off 0V ≤ VCC ≤ 1.5 and: VA = 3.8 V, VB = 1.2 V VA = 0.0 V or 2.4 V, VB = 1.2 V VA = -1.4 V, VB = 1.2 V | 0 -20 -32 | | 32 20 0 | uA |
| IB(OFF) | Input Current Receiver or Transceiver Power Off 0V ≤ VCC ≤ 1.5 and: VB = 3.8 V, VA = 1.2 V VB = 0.0 V or 2.4 V, VA = 1.2 V VB = -1.4 V, VA = 1.2 V | 0 -20 -32 | | 32 20 0 | uA |
| IAB(OFF) | Receiver Input or Transceiver Input/Output Power Off Differential Input Current; (IA-IB) VA = VB, 0 ≤ VCC ≤ 1.5 V, -1.4 ≤ VA ≤ 3.8 V | -4 | | 4 | uA |
| CA | Transceiver Input Capacitance with Driver Disabled VA = 0.4 sin(30E6πt) + 0.5 V using HP4194A impedance analyzer (or equivalent); VB = 1.2 V | | 5 | | pF |
| CB | Transceiver Input Capacitance with Driver Disabled VB = 0.4 sin(30E6πt) + 0.5 V using HP4194A impedance analyzer (or equivalent); VA = 1.2 V | | 5 | | pF |
| CAB | Transceiver Differential Input Capacitance with Driver Disabled VA = 0.4 sin(30E6πt) + 0.5 V using HP4194A impedance analyzer (or equivalent); VB = 1.2 V | | | 3.0 | pF |
| CA/B | Transceiver Input Capacitance Balance with Driver Disabled, (CA/CB) | 99 | | 101 | % |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

4. See Figure 3. DC Measurements reference.
5. Typ value at 25°C and 3.3 VCC supply voltage.

Table 6. DRIVER AC CHARACTERISTICS VCC = 3.3 ±10% V (3.0 to 3.6 V), GND = 0 V, TA = -40°C to +85°C (Note 6)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|-------------|--|-----|-----|-----|------|
| tPLH / tPHL | Propagation Delay (See Figure 7) | 1.0 | 1.5 | 2.4 | ns |
| tPHZ / tPLZ | Disable Time HIGH or LOW state to High Impedance (See Figure 8) | | | 7 | ns |
| tPZH / tPZL | Enable Time High Impedance to HIGH or LOW state (See Figure 8) | | | 7 | ns |
| tSK(P) | Pulse Skew (tPLH - tPHL) (See Figure 7) | | 0 | 100 | ps |
| tSK(PP) | Device to Device Skew similar path and conditions (See Figure 7) | | | 1 | ns |
| tJIT(PER) | Period Jitter RMS, 100 MHz (Source tr/tf 0.5 ns, 10 and 90 % points, 30k samples. Source jitter de-embedded from Output values) (See Figure 10) | | 2 | 3 | ps |
| tJIT(PP) | Peak-to-peak Jitter, 200 Mbps 2 ¹⁵ -1 PRBS (Source tr/tf 0.5 ns, 10 and 90% points, 100k samples. Source jitter de-embedded from Output values) (See Figure 10) | | 30 | 130 | ps |
| tr / tf | Differential Output rise and fall times (See Figure 7) | 1 | | 1.6 | ns |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

6. Typ value at 25°C and 3.3 VCC supply voltage.

NB3N201S, NB3N206S

Table 7. RECEIVER AC CHARACTERISTICS VCC = 3.3 ±10% V(3.0 to 3.6 V), GND = 0 V, TA = -40°C to +85°C (Note 7)

| Symbol | Characteristic | Min | Typ | Max | Unit | |
|-------------------------------------|--|-----|------------------|------------|------------|----|
| t _{PLH} / t _{PHL} | Propagation Delay (See Figure 12) | 2 | 4 | 6 | ns | |
| t _{PHZ} / t _{PLZ} | Disable Time HIGH or LOW state to High Impedance (See Figure 13) | | | 10 | ns | |
| t _{PZH} / t _{PZL} | Enable Time High Impedance to HIGH or LOW state (See Figure 13) | | | 15 | ns | |
| t _{SK(P)} | Pulse Skew ((t _{PLH} - t _{PHL})) (See Figure 14) C _L = 5 pF | | Type 1 Type 2 | 100 300 | 300 500 | ps |
| t _{SK(PP)} | Device to Device Skew similar path and conditions (See Figure 12) C _L = 5 pF | | | 1 | | ns |
| t _{JIT(PER)} | Period Jitter RMS, 100 MHz (Source: VID = 200 mV _{pp} for 201 and 203, VID = 400 mV _{pp} for 206 and 207, V _{CM} = 1 V, tr/tf 0.5 ns, 10 and 90 % points, 30k samples. Source jitter de-embedded from Output values) (See Figure 14) | | 4 | 7 | | ps |
| t _{JIT(PP)} | Peak-to-peak Jitter, 200 Mbps 2 ¹⁵ -1 PRBS (Source tr/tf 0.5 ns, 10% and 90% points, 100k samples. Source jitter de-embedded from Output values) (See Figure 14) | | Type 1 Type 2 | 300 450 | 700 800 | ps |
| tr / tf | Differential Output rise and fall times (See Figure 14) C _L = 15 pF | 1 | | 2.3 | | ns |

7. Typ value at 25°C and 3.3 VCC supply voltage. .

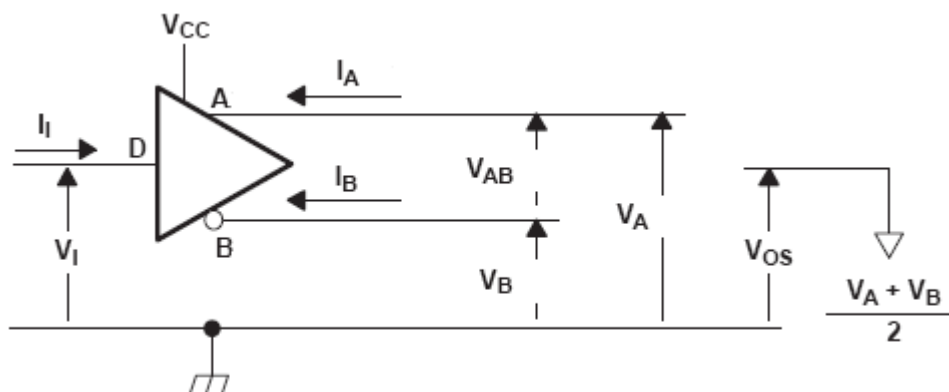
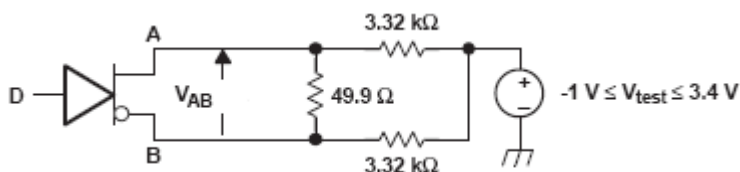


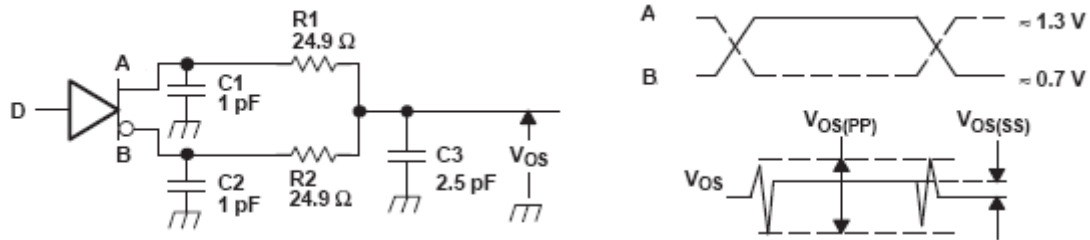
Figure 3. Driver Voltage and Current Definitions



A. All resistors are 1% tolerance.

Figure 4. Differential Output Voltage Test Circuit

NB3N201S, NB3N206S



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse frequency = 500 kHz, duty cycle = $50 \pm 5\%$.
- B. C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are 20% tolerance.
- C. R1 and R2 are metal film, surface mount, 1% tolerance, and located within 2 cm of the D.U.T.
- D. The measurement of $V_{OS(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 5. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

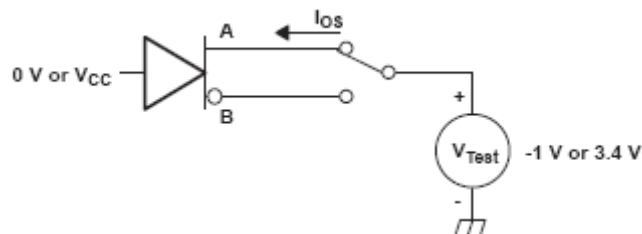


Figure 6. Driver Short-Circuit Test Circuit



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, frequency = 500 kHz, duty cycle = $50 \pm 5\%$.
- B. C1, C2, and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are 20%.
- C. R1 is a metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
- D. The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 7. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

NB3N201S, NB3N206S



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, frequency = 500 kHz, duty cycle = $50 \pm 5\%$.
- B. C1, C2, C3, and C4 includes instrumentation and fixture capacitance within 2 cm of the D.U.T. and are 20%.
- C. R1 and R2 are metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
- D. The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 8. Driver Enable and Disable Time Circuit and Definitions

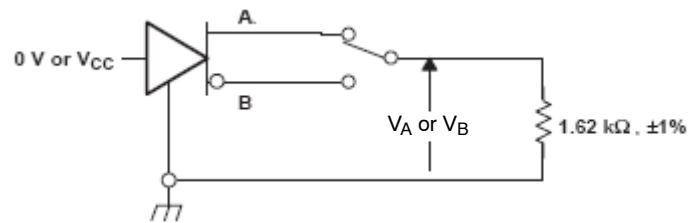
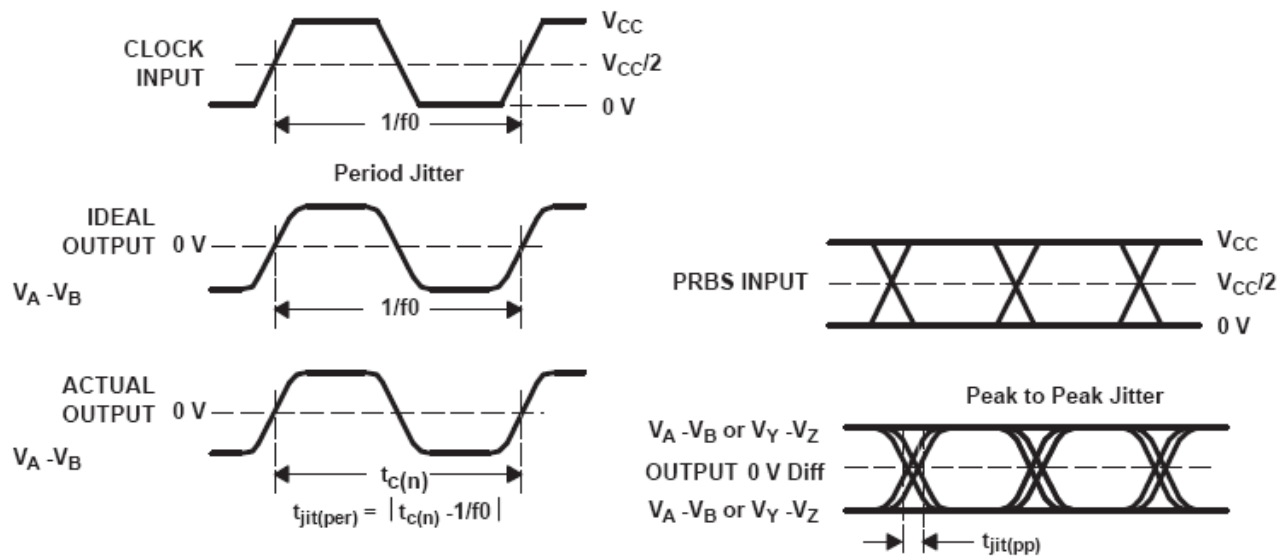


Figure 9. Maximum Steady State Output Voltage

NB3N201S, NB3N206S



- A. All input pulses are supplied by an Agilent 8304A Stimulus System.
- B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
- C. Period jitter is measured using a 100 MHz 50 ±1% duty cycle clock input.
- D. Peak-to-peak jitter is measured using a 200 Mbps 215-1 PRBS input.

Figure 10. Driver Jitter Measurement Waveforms

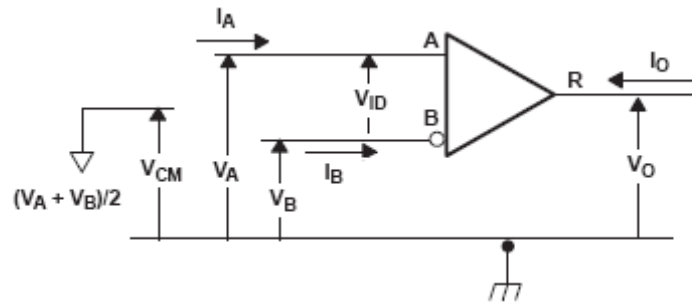
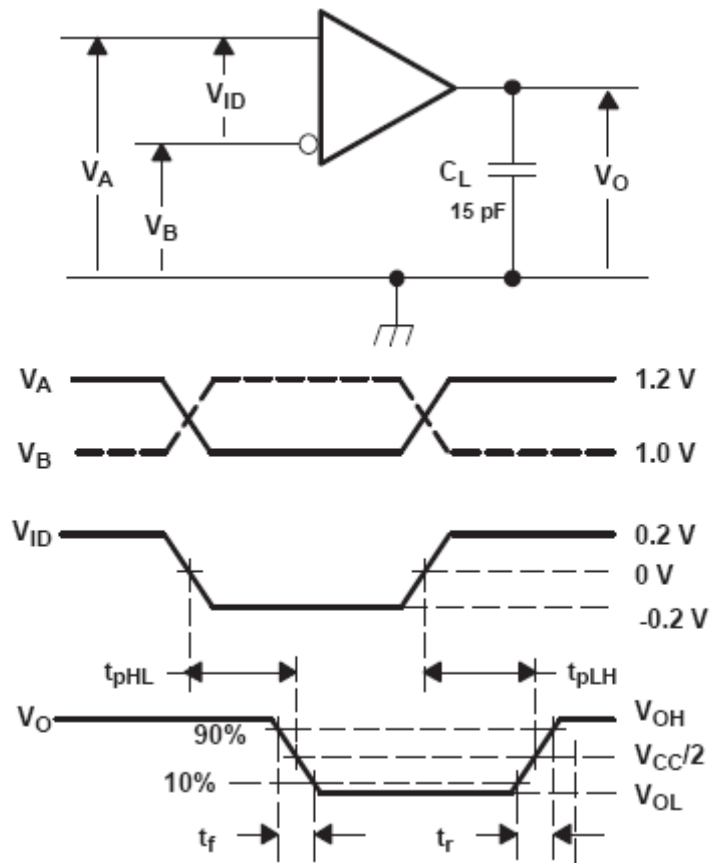


Figure 11. Receiver Voltage and Current Definitions

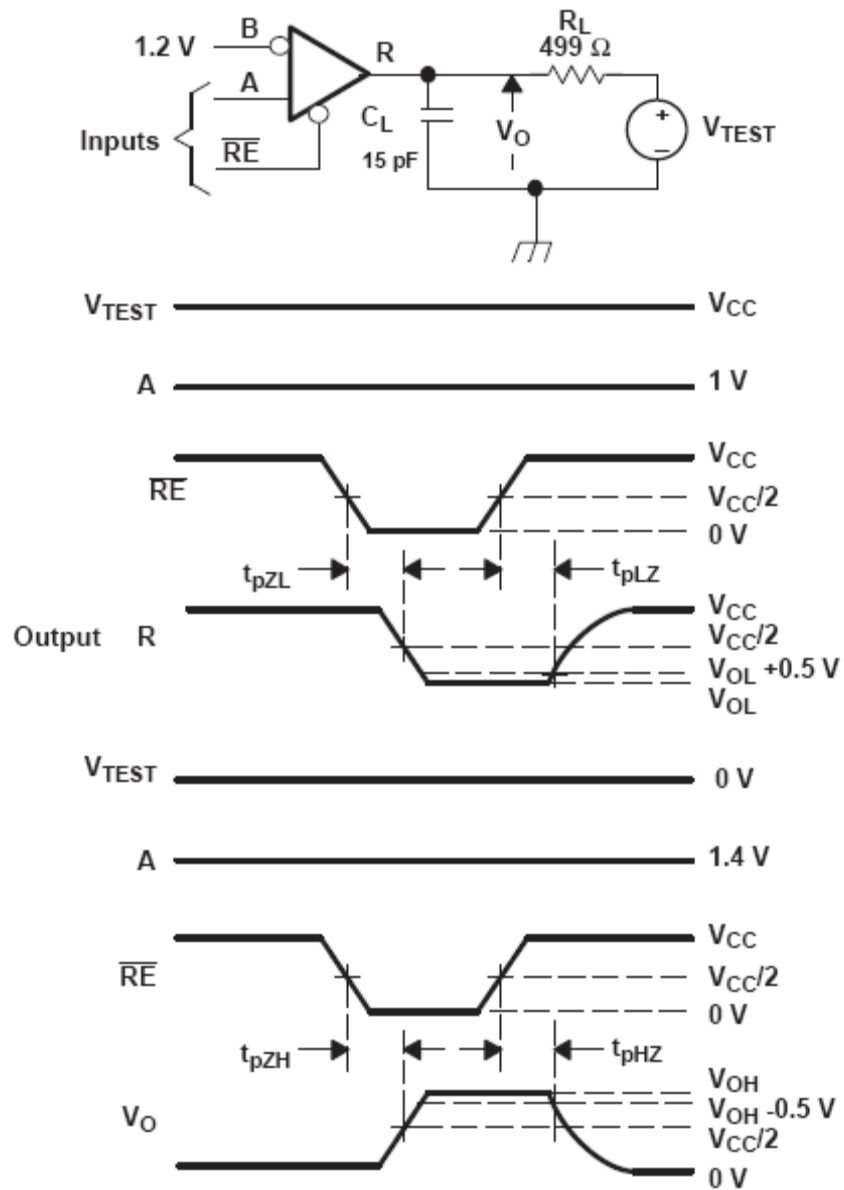
NB3N201S, NB3N206S



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1 \text{ ns}$, frequency = 50 MHz , duty cycle = $50 \pm 5\%$. C_L is a combination of a 20%–tolerance, low–loss ceramic, surface–mount capacitor and fixture capacitance within 2 cm of the D.U.T.
- B. The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz .

Figure 12. Receiver Timing Test Circuit and Waveforms

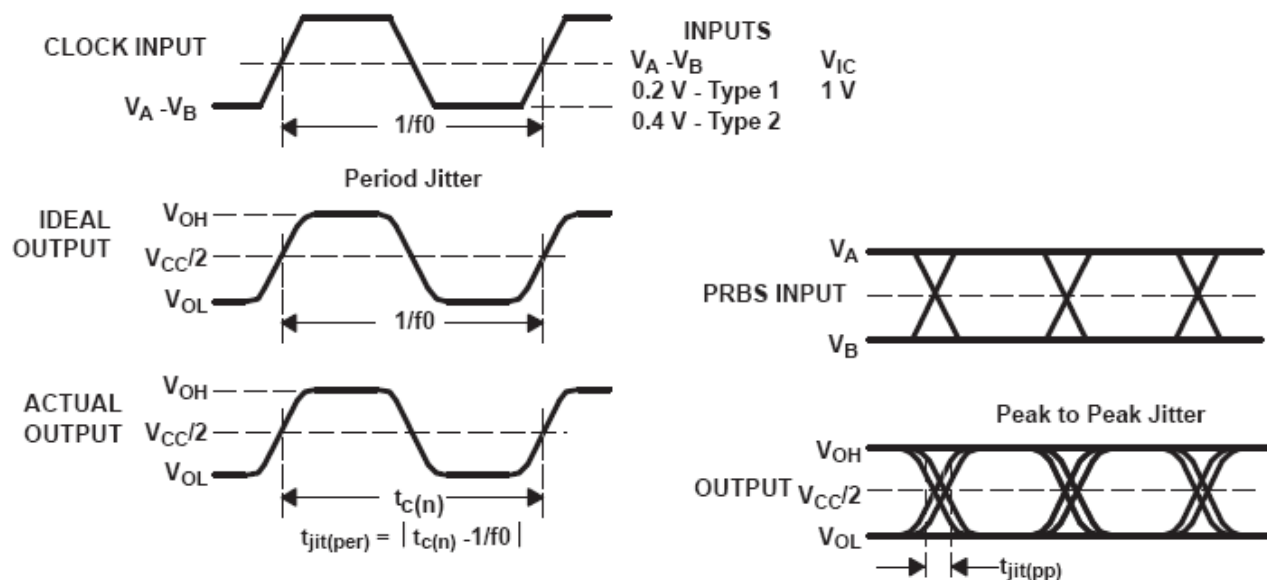
NB3N201S, NB3N206S



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, frequency = 500 kHz, duty cycle = 50 \pm 5%.
- B. R_L is 1% tolerance, metal film, surface mount, and located within 2 cm of the D.U.T.
- C. C_L is the instrumentation and fixture capacitance within 2 cm of the DUT and 20%.

Figure 13. Receiver Enable/Disable Time Test Circuit and Waveforms

NB3N201S, NB3N206S



- A. All input pulses are supplied by an Agilent 8304A Stimulus System.
- B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
- C. Period jitter is measured using a 100 MHz 50 ±1% duty cycle clock input.
- D. Peak-to-peak jitter is measured using a 200 Mbps 2¹⁵-1 PRBS input.

Figure 14. Receiver Jitter Measurement Waveforms

Table 8. TYPE-1 RECEIVER INPUT THRESHOLD TEST VOLTAGES

| Applied Voltages | | Resulting Differential Input Voltage | Resulting Common-Mode Input Voltage | Receiver Output |
|------------------|--------|--------------------------------------|-------------------------------------|-----------------|
| VIA | VIB | VID | VIC | |
| 2.400 | 0.000 | 2.400 | 1.200 | H |
| 0.000 | 2.400 | -2.400 | 1.200 | L |
| 3.800 | 3.750 | 0.050 | 3.775 | H |
| 3.750 | 3.800 | -0.050 | 3.775 | L |
| -1.350 | -1.400 | 0.050 | -1.375 | H |
| -1.400 | -1.350 | -0.050 | -1.375 | L |

H = high level, L = low level, output state assumes receiver is enabled (RE = L)

Table 9. TYPE-2 RECEIVER INPUT THRESHOLD TEST VOLTAGES

| Applied Voltages | | Resulting Differential Input Voltage | Resulting Common-Mode Input Voltage | Receiver Output (Note) |
|------------------|--------|--------------------------------------|-------------------------------------|-------------------------|
| VIA | VIB | VID | VIC | |
| 2.400 | 0.000 | 2.400 | 1.200 | H |
| 0.000 | 2.400 | -2.400 | 1.200 | L |
| 3.800 | 3.650 | 0.150 | 3.725 | H |
| 3.800 | 3.750 | 0.050 | 3.775 | L |
| -1.250 | -1.400 | 0.150 | -1.325 | H |
| -1.350 | -1.400 | 0.050 | -1.375 | L |

H = high level, L = low level, output state assumes receiver is enabled (RE = L)

NB3N201S, NB3N206S

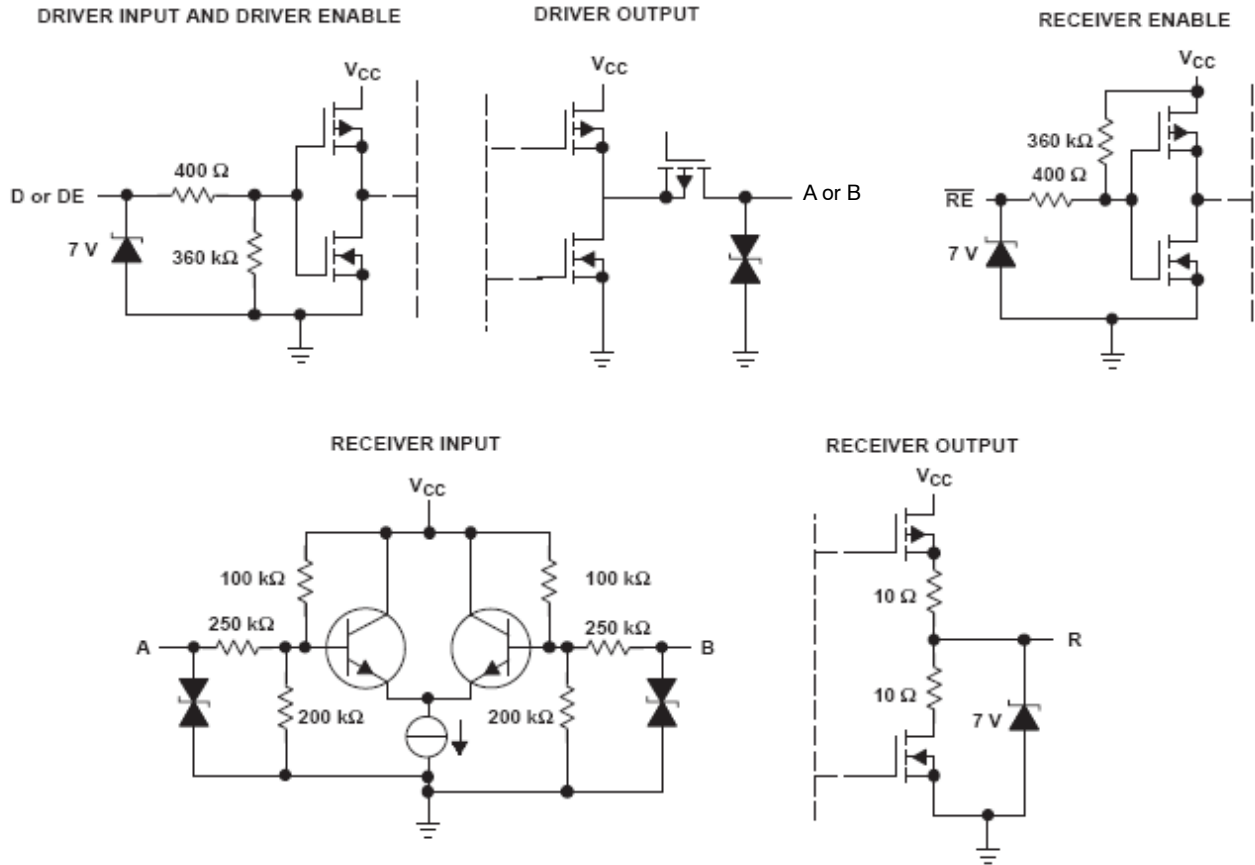


Figure 15. Equivalent Input and Output Schematic Diagrams

APPLICATION INFORMATION

Receiver Input Threshold (Failsafe)

The MLVDS standard defines a type 1 and type 2 receiver. Type 1 receivers include no provisions for failsafe and have their differential input voltage thresholds near zero volts.

Type 2 receivers have their differential input voltage thresholds offset from zero volts to detect the absence of a voltage difference. The impact to receiver output by the offset input can be seen in Table 10 and Figure 16.

Table 10. RECEIVER INPUT VOLTAGE THRESHOLD REQUIREMENTS

| Receiver Type | Output Low | Output High |
|---------------|---|---|
| Type 1 | $-2.4 \text{ V} \leq \text{VID} \leq -0.05 \text{ V}$ | $0.05 \text{ V} \leq \text{VID} \leq 2.4 \text{ V}$ |
| Type 2 | $-2.4 \text{ V} \leq \text{VID} \leq 0.05 \text{ V}$ | $0.15 \text{ V} \leq \text{VID} \leq 2.4 \text{ V}$ |

NB3N201S, NB3N206S

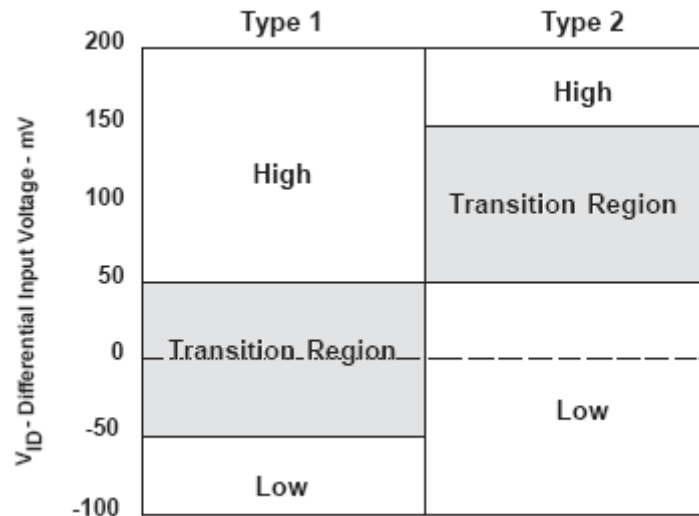


Figure 16. Receiver Differential Input Voltage Showing Transition Regions by Type

LIVE INSERTION/GLITCH-FREE POWER UP/DOWN

The NB3N201/206 family of products provides a glitch-free power up/down feature that prevents the M-LVDS outputs of the device from turning on during a power up or power down event. This is especially important in live insertion applications, when a device is physically connected to an M-LVDS multipoint bus and V_{CC} is ramping.

While the M-LVDS interface for these devices is glitch free on power up/down, the receiver output structure is not. Figure 17 shows the performance of the receiver output pin, R (CHANNEL 2), as V_{CC} (CHANNEL 1) is ramped. The glitch on the R pin is independent of the RE voltage. Any complications or issues from this glitch are easily resolved in power sequencing or system requirements that suspend operation until V_{CC} has reached a steady state value.

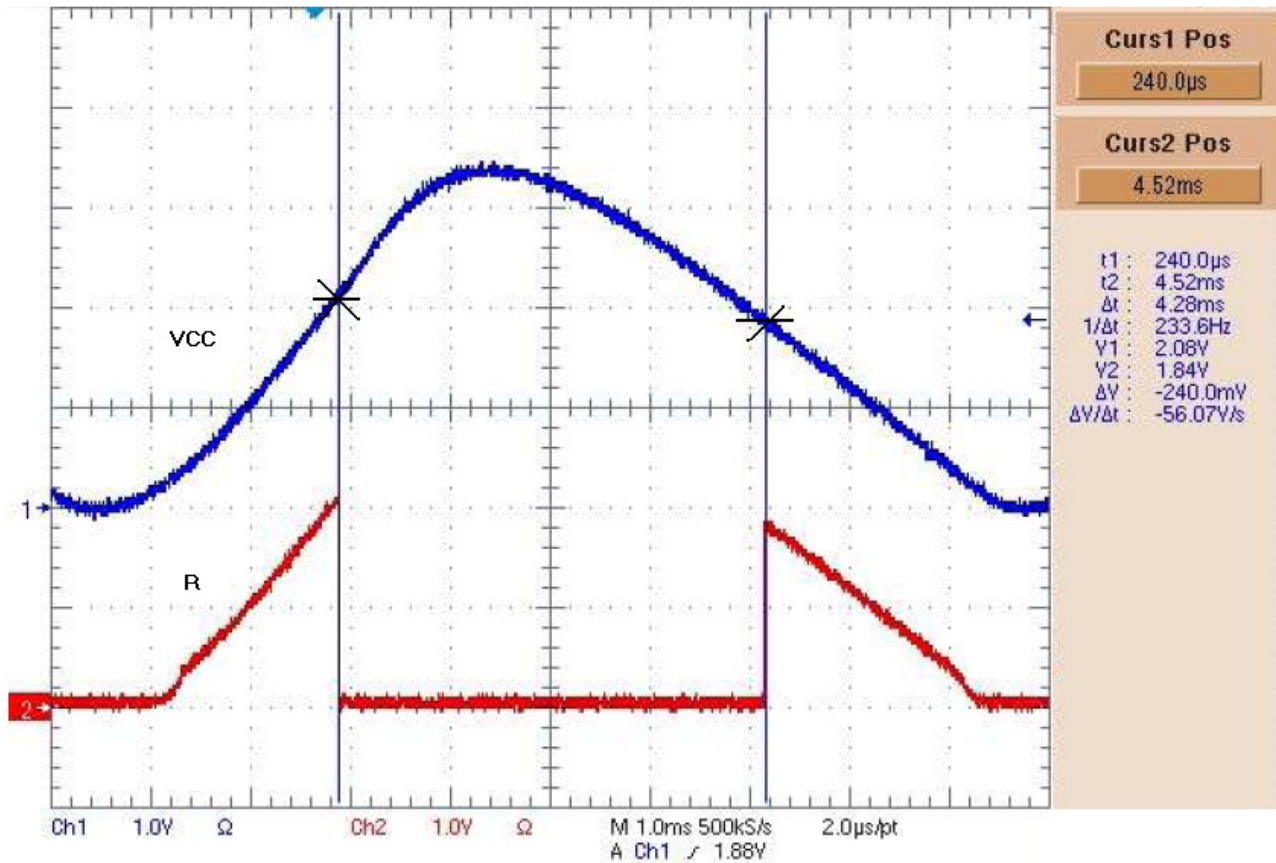


Figure 17. M-LVDS Receiver Output: VCC (CHANNEL 1), R Pin (CHANNEL 2)

Simplex Theory Configurations: Data flow is unidirectional and Point-to-Point from one Driver to one Receiver. NB3N201SDG and NB3N206SDG devices provide a high signal current allowing long drive runs and high noise immunity. Single terminated interconnects yield

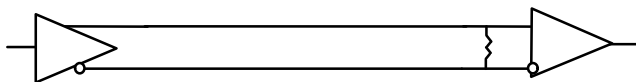


Figure 18. Point-to-Point Simplex Single Termination

high amplitude levels. Parallel terminated interconnects yield typical MLVDS amplitude levels and minimizes reflections. See Figures 18 and 19. A NB3N201SDG and NB3N206SDG can be used as the driver or as a receiver.

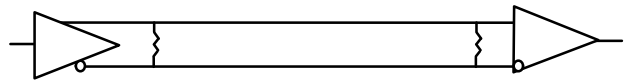


Figure 19. Parallel-Terminated Simplex

Simplex Multidrop Theory Configurations: Data flow is unidirectional from one Driver with one or more Receivers. Multiple boards required. Single terminated interconnects yield high amplitude levels. Parallel terminated interconnects yield typical MLVDS amplitude levels and

minimizes reflections. On the Evaluation Test Board, Headers P1, P2, and P3 may be used as need to interconnect transceivers to a each other or a bus. See Figures 20 and 21. A NB3N201SDG and NB3N206SDG can be used as the driver or as a receiver.

NB3N201S, NB3N206S

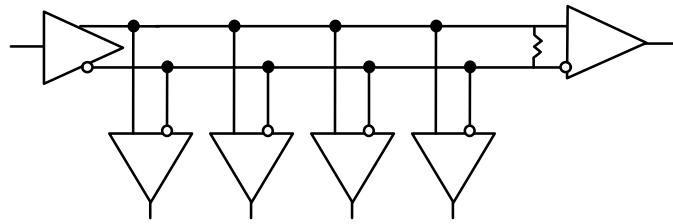


Figure 20. Multidrop or Distributed Simplex with Single Termination

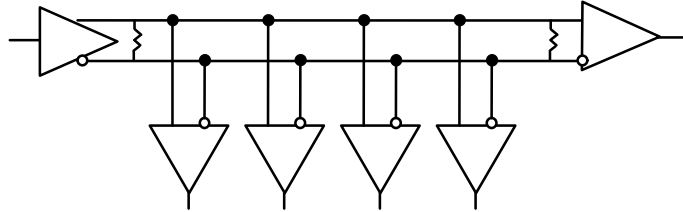


Figure 21. Multidrop or Distributed Simplex with Double Termination

Half Duplex Multinode Multipoint Theory Configurations: Data flow is unidirectional and selected from one of multiple possible Drivers to multiple Receivers. One “Two Node” multipoint connection can be accomplished with a single evaluation test board. More than Two Nodes requires multiple evaluation test boards. Parallel terminated interconnects yield typical MLVDS amplitude

levels and minimizes reflections. Parallel terminated interconnects yield typical LMVDS amplitude levels and minimizes reflections. On the Test Board, Headers P1, P2, and P3 may be used as need to interconnect transceivers to each other or a bus. See Figure 22. A NB3N206SDG can be used as the driver or as a receiver.

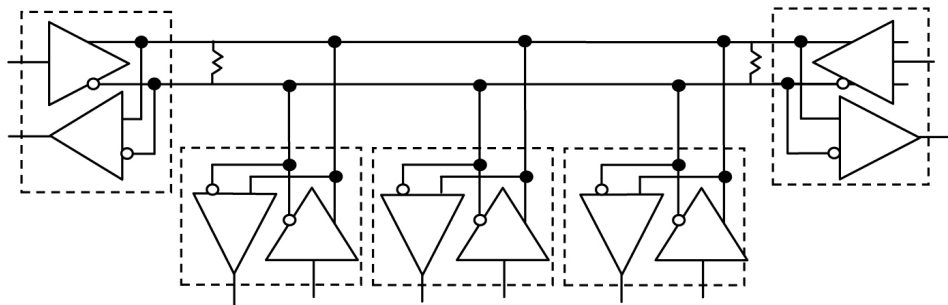


Figure 22. Multinode Multipoint Half Duplex (requires Double Termination)

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Figure 23.

NB3N201S, NB3N206S

ORDERING INFORMATION

| Device | Receiver | Pin 1 Quadrant | Package | Shipping† |
|--------------|----------|----------------|-----------------------|--------------------|
| NB3N201SDR2G | Type 1 | Q1 | SOIC – 8 (Pb-Free) | 2500 / Tape & Reel |
| NB3N206SDR2G | Type 2 | Q1 | SOIC – 8 (Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ■ = Pb-Free Package

XXXXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|---|--|--|--|
| <p>STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER</p> | <p>STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1</p> | <p>STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1</p> | <p>STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE</p> |
| <p>STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE</p> | <p>STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE</p> | <p>STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd</p> | <p>STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1</p> |
| <p>STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON</p> | <p>STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND</p> | <p>STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1</p> | <p>STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> | <p>STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN</p> | <p>STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON</p> | <p>STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC</p> | <p>STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE</p> | <p>STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1</p> | <p>STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6</p> | <p>STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND</p> | <p>STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT</p> | <p>STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT</p> | <p>STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC</p> | <p>STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN</p> | <p>STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN</p> |
| <p>STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1</p> | <p>STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1</p> | | |

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