

# MMJT9435

Preferred Device

## Bipolar Power Transistors

### PNP Silicon

#### Features

- Pb-Free Packages are Available
- Collector –Emitter Sustaining Voltage –  
 $V_{CEO(sus)} = 30 \text{ Vdc (Min) @ } I_C = 10 \text{ mAdc}$
- High DC Current Gain –  
 $h_{FE} = 125 \text{ (Min) @ } I_C = 0.8 \text{ Adc}$   
 $= 90 \text{ (Min) @ } I_C = 3.0 \text{ Adc}$
- Low Collector –Emitter Saturation Voltage –  
 $V_{CE(sat)} = 0.275 \text{ Vdc (Max) @ } I_C = 1.2 \text{ Adc}$   
 $= 0.55 \text{ Vdc (Max) @ } I_C = 3.0 \text{ Adc}$
- SOT-223 Surface Mount Packaging
- Epoxy Meets UL 94, V-0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B; > 8000 V  
Machine Model, C; > 400 V



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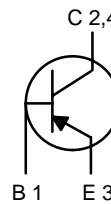
<http://onsemi.com>

#### POWER BJT

**$I_C = 3.0 \text{ AMPERES}$**

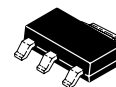
**$BV_{CEO} = 30 \text{ VOLTS}$**

**$V_{CE(sat)} = 0.275 \text{ VOLTS}$**

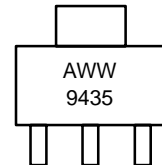


Schematic

#### MARKING DIAGRAM

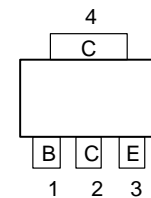


SOT-223  
CASE 318E  
STYLE 1



9435 = Specific Device Code  
A = Assembly Location  
WW = Work Week

#### PIN ASSIGNMENT



Top View Pinout

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

**Preferred** devices are recommended choices for future use and best overall value.

# MMJT9435

## MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V <sub>CEO</sub>	30	Vdc
Collector–Base Voltage	V <sub>CB</sub>	45	Vdc
Emitter–Base Voltage	V <sub>EB</sub>	6.0	Vdc
Base Current – Continuous	I <sub>B</sub>	1.0	Adc
Collector Current – Continuous – Peak	I <sub>C</sub>	3.0 5.0	Adc
Total Power Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C Total P <sub>D</sub> @ T <sub>A</sub> = 25°C mounted on 1" sq. (645 sq. mm) Collector pad on FR–4 bd material Total P <sub>D</sub> @ T <sub>A</sub> = 25°C mounted on 0.012" sq. (7.6 sq. mm) Collector pad on FR–4 bd material	P <sub>D</sub>	3.0 24 1.56 0.72	W mW/°C W
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	–55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case – Junction–to–Ambient on 1" sq. (645 sq. mm) Collector pad on FR–4 bd material – Junction–to–Ambient on 0.012" sq. (7.6 sq. mm) Collector pad on FR–4 bd material	R <sub>θJC</sub> R <sub>θJA</sub> R <sub>θJA</sub>	42 80 174	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T <sub>L</sub>	260	°C

## ORDERING INFORMATION

Device	Package	Shipping†
MMJT9435T1	SOT–223	1000 / Tape & Reel
MMJT9435T1G	SOT–223 (Pb–Free)	1000 / Tape & Reel
MMJT9435T3	SOT–223	4000 / Tape & Reel
MMJT9435T3G	SOT–223 (Pb–Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MMJT9435

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 10 mA, I <sub>B</sub> = 0 A)	V <sub>CEO(sus)</sub>	30	–	–	Vdc
Emitter–Base Voltage (I <sub>E</sub> = 50 μA, I <sub>C</sub> = 0 A)	V <sub>EBO</sub>	6.0	–	–	Vdc
Collector Cutoff Current (V <sub>CE</sub> = 25 Vdc, R <sub>BE</sub> = 200 Ω) (V <sub>CE</sub> = 25 Vdc, R <sub>BE</sub> = 200 Ω, T <sub>J</sub> = 125°C)	I <sub>CER</sub>	–	–	20 200	μA
Emitter Cutoff Current (V <sub>BE</sub> = 5.0 Vdc)	I <sub>EBO</sub>	–	–	10	μA

### ON CHARACTERISTICS (Note 1)

Collector–Emitter Saturation Voltage (I <sub>C</sub> = 0.8 A, I <sub>B</sub> = 20 mA) (I <sub>C</sub> = 1.2 A, I <sub>B</sub> = 20 mA) (I <sub>C</sub> = 3.0 A, I <sub>B</sub> = 0.3 A)	V <sub>CE(sat)</sub>	–	0.155	0.210 0.275 0.550	Vdc
Base–Emitter Saturation Voltage (I <sub>C</sub> = 3.0 A, I <sub>B</sub> = 0.3 A)	V <sub>BE(sat)</sub>	–	–	1.25	Vdc
Base–Emitter On Voltage (I <sub>C</sub> = 1.2 A, V <sub>CE</sub> = 4.0 Vdc)	V <sub>BE(on)</sub>	–	–	1.10	Vdc
DC Current Gain (I <sub>C</sub> = 0.8 A, V <sub>CE</sub> = 1.0 Vdc) (I <sub>C</sub> = 1.2 A, V <sub>CE</sub> = 1.0 Vdc) (I <sub>C</sub> = 3.0 A, V <sub>CE</sub> = 1.0 Vdc)	h <sub>FE</sub>	125 110 90	220	–	–

### DYNAMIC CHARACTERISTICS

Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0 A, f = 1.0 MHz)	C <sub>ob</sub>	–	100	150	pF
Input Capacitance (V <sub>EB</sub> = 8.0 Vdc)	C <sub>ib</sub>	–	135	–	pF
Current–Gain – Bandwidth Product (Note 2) (I <sub>C</sub> = 500 mA, V <sub>CE</sub> = 10 V, F <sub>test</sub> = 1.0 MHz)	f <sub>T</sub>	–	110	–	MHz

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. f<sub>T</sub> = |h<sub>FE</sub>| • f<sub>test</sub>

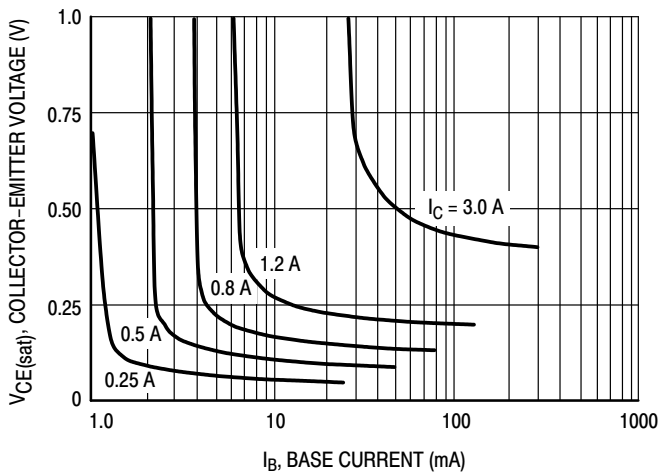


Figure 1. Collector Saturation Region

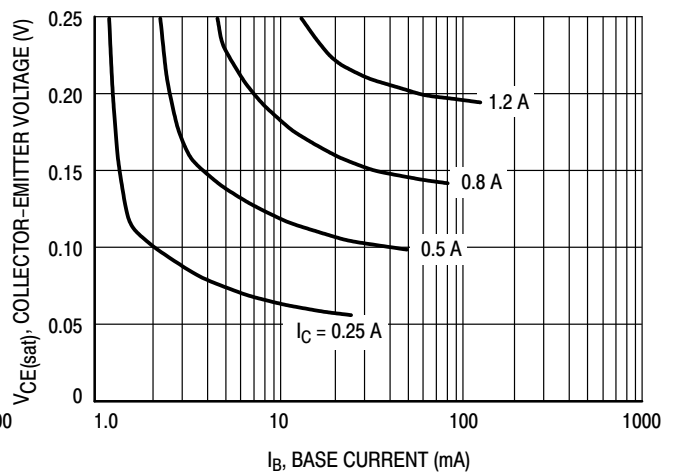


Figure 2. Collector Saturation Region

# MMJT9435

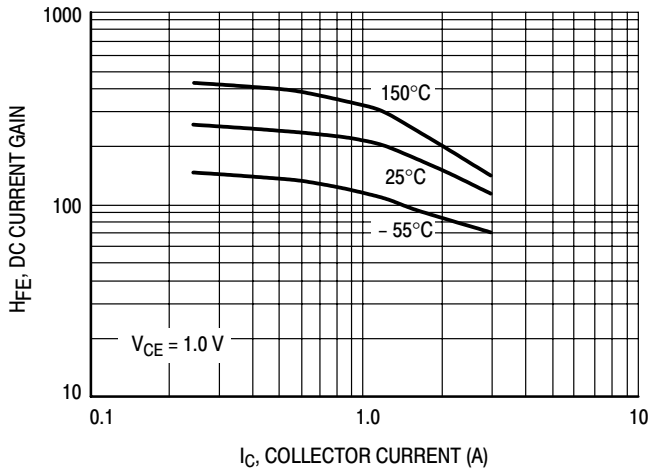


Figure 3. DC Current Gain

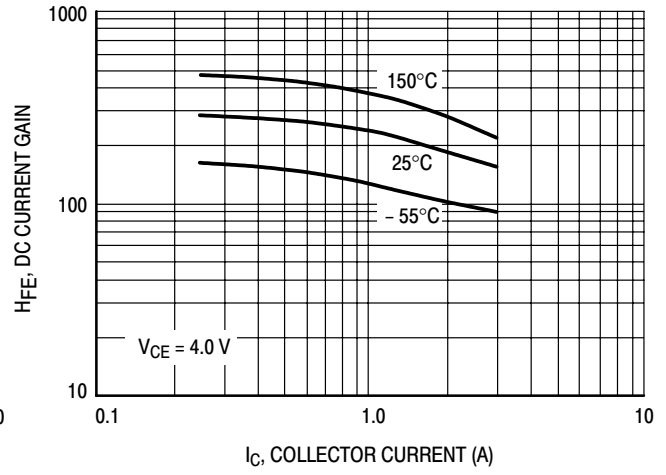


Figure 4. DC Current Gain

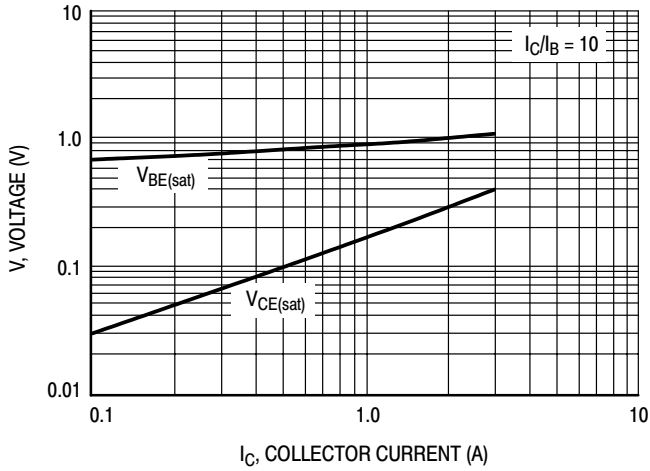


Figure 5. "On" Voltages

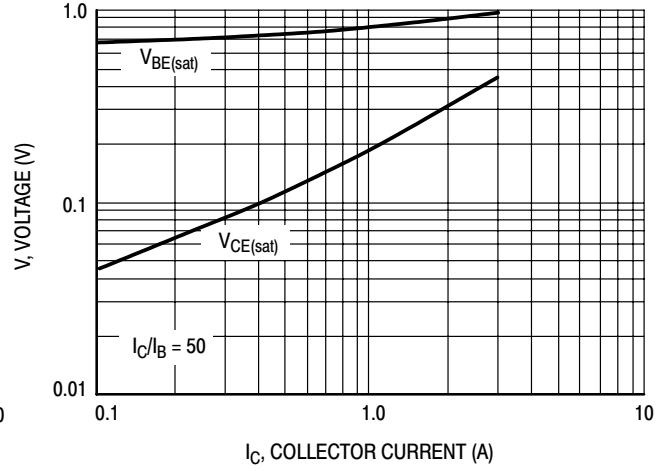


Figure 6. "On" Voltages

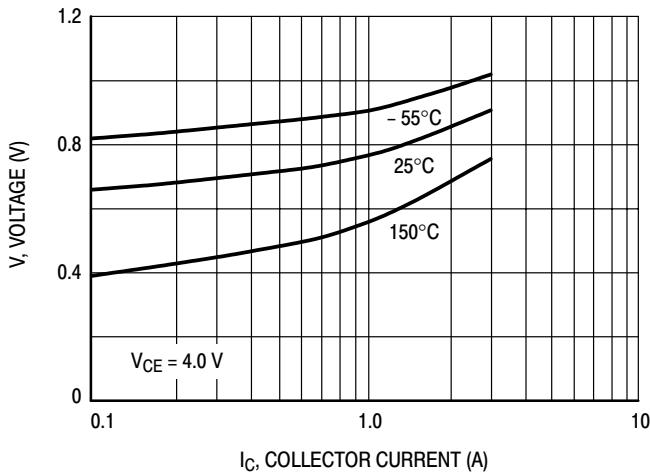


Figure 7.  $V_{BE(on)}$  Voltage

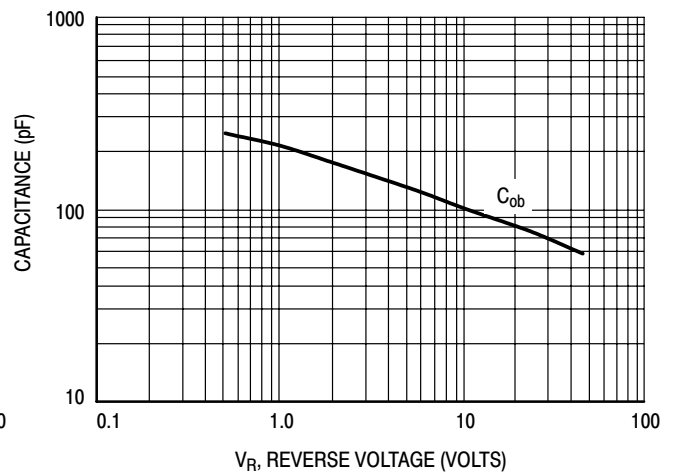


Figure 8. Output Capacitance

# MMJT9435

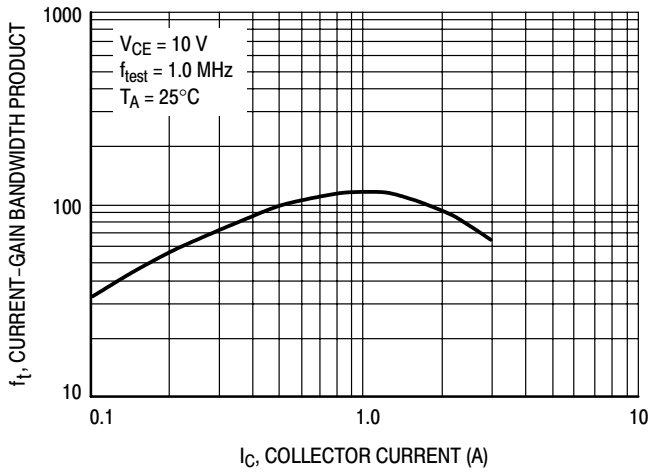


Figure 9. Current-Gain Bandwidth Product

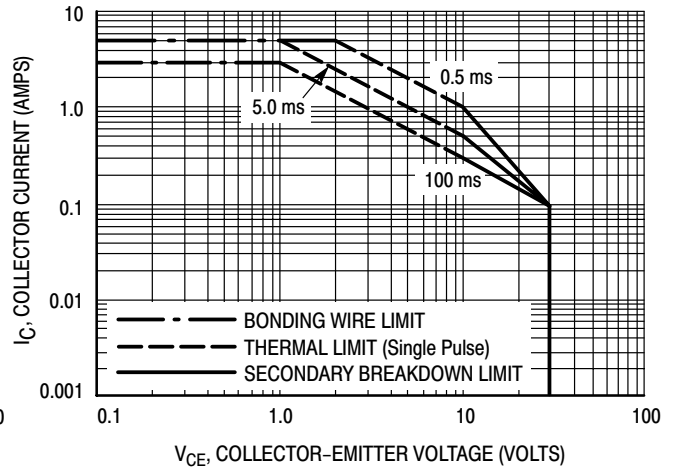


Figure 10. Active Region Safe Operating Area

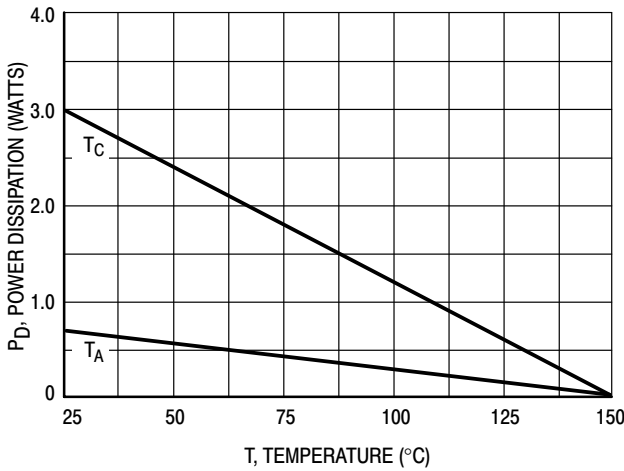


Figure 11. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

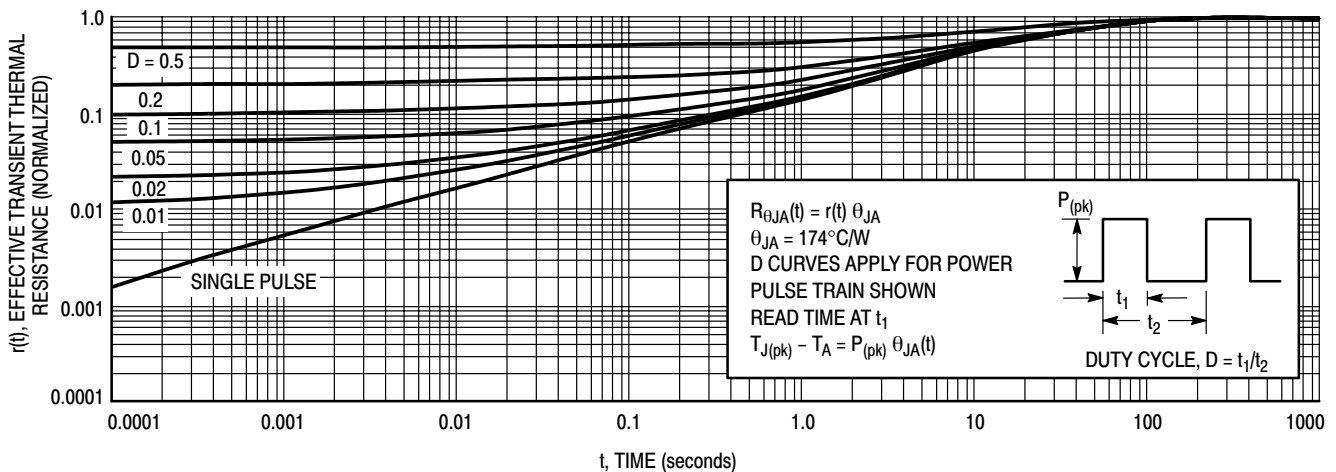


Figure 12. Thermal Response

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

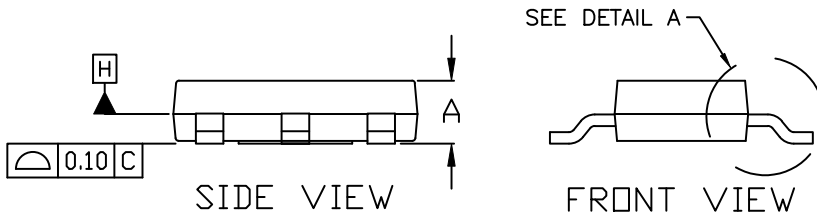
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SCALE 1:1

SOT-223 (TO-261)  
CASE 318E-04  
ISSUE R

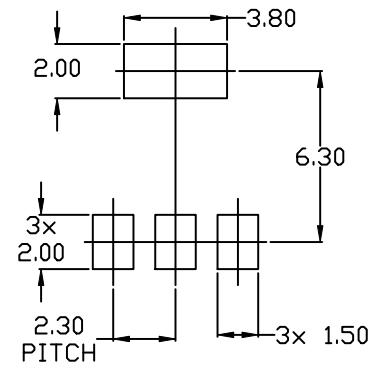
DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



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**SOT-223 (TO-261)**  
**CASE 318E-04**  
**ISSUE R**

DATE 02 OCT 2018

- |  |   |   |   |   |
|--|---|---|---|---|
| <b>STYLE 1:</b><br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 2:</b><br>PIN 1. ANODE<br>2. CATHODE<br>3. NC<br>4. CATHODE        | <b>STYLE 3:</b><br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN           | <b>STYLE 4:</b><br>PIN 1. SOURCE<br>2. DRAIN<br>3. GATE<br>4. DRAIN   | <b>STYLE 5:</b><br>PIN 1. DRAIN<br>2. GATE<br>3. SOURCE<br>4. GATE    |
| <b>STYLE 6:</b><br>PIN 1. RETURN<br>2. INPUT<br>3. OUTPUT<br>4. INPUT        | <b>STYLE 7:</b><br>PIN 1. ANODE 1<br>2. CATHODE<br>3. ANODE 2<br>4. CATHODE | <b>STYLE 8:</b><br>CANCELLED  | <b>STYLE 9:</b><br>PIN 1. INPUT<br>2. GROUND<br>3. LOGIC<br>4. GROUND | <b>STYLE 10:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE<br>4. ANODE |
| <b>STYLE 11:</b><br>PIN 1. MT 1<br>2. MT 2<br>3. GATE<br>4. MT 2             | <b>STYLE 12:</b><br>PIN 1. INPUT<br>2. OUTPUT<br>3. NC<br>4. OUTPUT         | <b>STYLE 13:</b><br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR |   |   |

**GENERIC  
 MARKING DIAGRAM\***



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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