

# MJL21195 (PNP), MJL21196 (NPN)

## Silicon Power Transistors

The MJL21195 and MJL21196 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

### Features

- Total Harmonic Distortion Characterized
- High DC Current Gain
- Excellent Gain Linearity
- High SOA
- Epoxy Meets UL 94, V-0 @ 0.125 in
- These Devices are Pb-Free and are RoHS Compliant\*

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	250	Vdc
Collector-Base Voltage	$V_{CBO}$	400	Vdc
Emitter-Base Voltage	$V_{EBO}$	5	Vdc
Collector-Emitter Voltage - 1.5 V	$V_{CEX}$	400	Vdc
Collector Current - Continuous	$I_C$	16	Adc
Collector Current - Peak (Note 1)	$I_{CM}$	30	Adc
Base Current - Continuous	$I_B$	5	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above $25^\circ\text{C}$	$P_D$	200 1.43	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$
ESD - Human Body Model	HBM	3B	V
ESD - Machine Model	MM	C	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Pulse Test: Pulse Width = 5.0  $\mu\text{s}$ , Duty Cycle  $\leq 10\%$ .

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.7	$^\circ\text{C}/\text{W}$

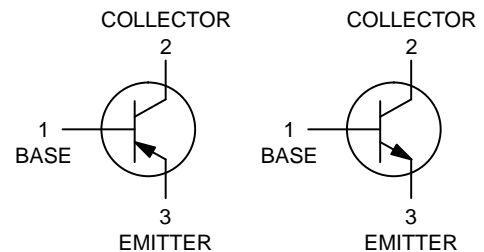


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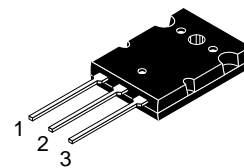
<http://onsemi.com>

## 16 A COMPLEMENTARY SILICON POWER TRANSISTORS 250 V, 200 W

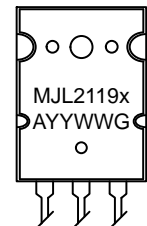
### COMPLEMENTARY



### MARKING DIAGRAM



**TO-264  
CASE 340G  
STYLE 2**



x = 5 or 6  
A = Assembly Location  
YY = Year  
WW = Work Week  
G = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping
MJL21195G	TO-264 (Pb-Free)	25 Units / Rail
MJL21196G	TO-264 (Pb-Free)	25 Units / Rail

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MJL21195 (PNP), MJL21196 (NPN)

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
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### OFF CHARACTERISTICS (Note 2)

Collector-Emitter Sustaining Voltage ( $I_C = 100\text{ mA}$ , $I_B = 0$ )	$V_{CEO(sus)}$	250	–	–	Vdc
Collector Cutoff Current ( $V_{CE} = 200\text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	–	–	100	$\mu\text{Adc}$

### OFF CHARACTERISTICS (Note 3)

Emitter Cutoff Current ( $V_{CE} = 5\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	–	100	$\mu\text{Adc}$
Collector Cutoff Current ( $V_{CE} = 250\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ )	$I_{CEX}$	–	–	100	$\mu\text{Adc}$

### SECOND BREAKDOWN (Note 3)

Second Breakdown Collector Current with Base Forward Biased ( $V_{CE} = 50\text{ Vdc}$ , $t = 1\text{ s}$ (Nonrepetitive)) ( $V_{CE} = 80\text{ Vdc}$ , $t = 1\text{ s}$ (Nonrepetitive))	$I_{S/b}$	4.0 2.25	– –	– –	Adc
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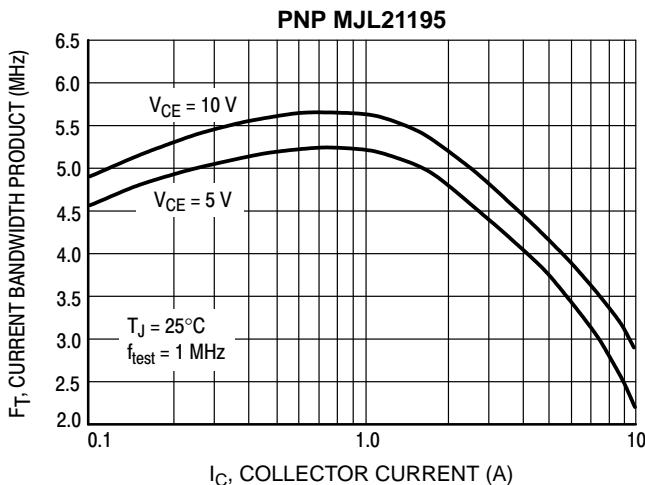
### ON CHARACTERISTICS (Note 3)

DC Current Gain ( $I_C = 8\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ ) ( $I_C = 16\text{ Adc}$ , $I_B = 5\text{ Adc}$ )	$h_{FE}$	25 8.0	– –	100 –	–
Base-Emitter On Voltage ( $I_C = 8\text{ Adc}$ , $V_{CE} = 5\text{ Vdc}$ )	$V_{BE(on)}$	–	–	2.2	Vdc
Collector-Emitter Saturation Voltage ( $I_C = 8\text{ Adc}$ , $I_B = 0.8\text{ Adc}$ ) ( $I_C = 16\text{ Adc}$ , $I_B = 3.2\text{ Adc}$ )	$V_{CE(sat)}$	– –	– –	1.4 4	Vdc

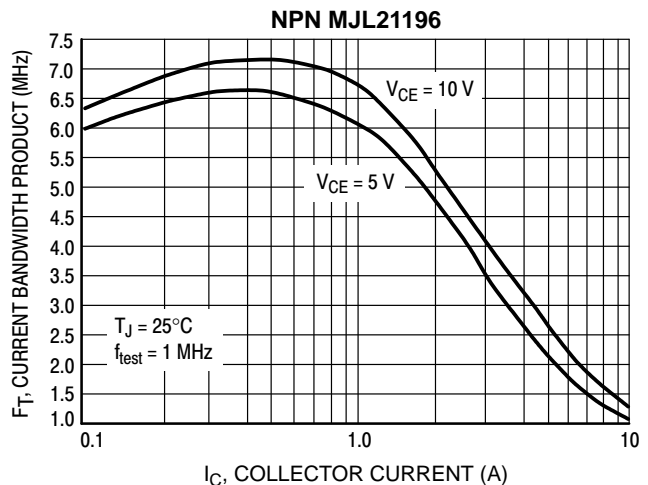
### DYNAMIC CHARACTERISTICS (Note 3)

Total Harmonic Distortion at the Output ( $V_{RMS} = 28.3\text{ V}$ , $f = 1\text{ kHz}$ , $P_{LOAD} = 100\text{ W}_{RMS}$ ) $h_{FE}$ unmatched (Matched pair $h_{FE} = 50 @ 5\text{ A}/5\text{ V}$ ) $h_{FE}$ matched	$T_{HD}$	– –	0.8 0.08	– –	%
Current Gain Bandwidth Product ( $I_C = 1\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 1\text{ MHz}$ )	$f_T$	4	–	–	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f_{test} = 1\text{ MHz}$ )	$C_{ob}$	–	–	500	pF

2. Pulse Test: Pulse Width =  $5.0\ \mu\text{s}$ , Duty Cycle  $\leq 10\%$ .
3. Pulse Test: Pulse Width =  $300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .



**Figure 1. Typical Current Gain Bandwidth Product**



**Figure 2. Typical Current Gain Bandwidth Product**

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## TYPICAL CHARACTERISTICS

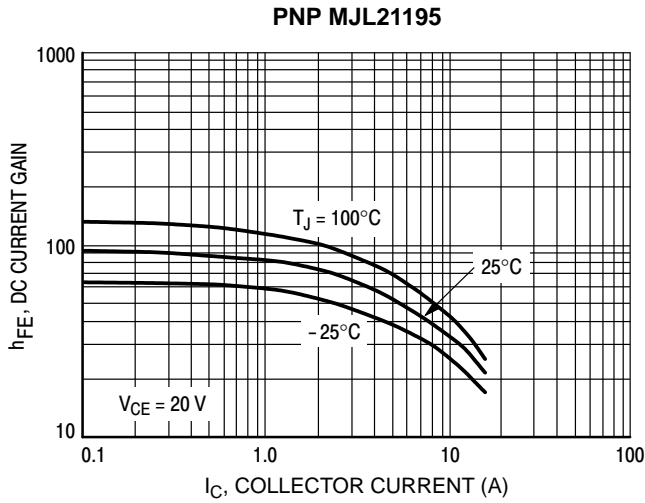


Figure 3. DC Current Gain,  $V_{CE} = 20\text{ V}$

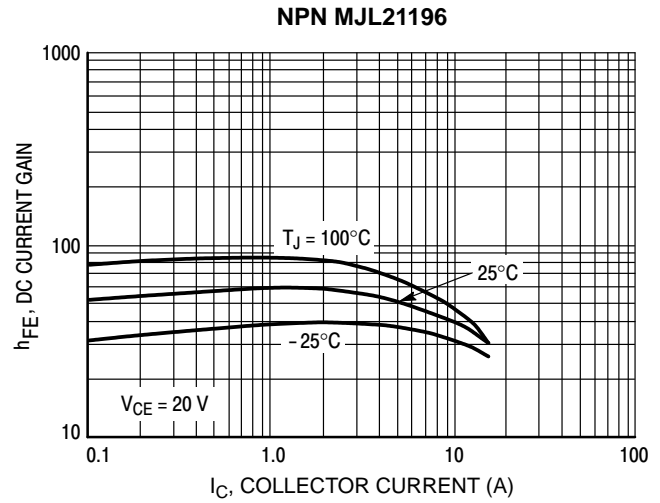


Figure 4. DC Current Gain,  $V_{CE} = 20\text{ V}$

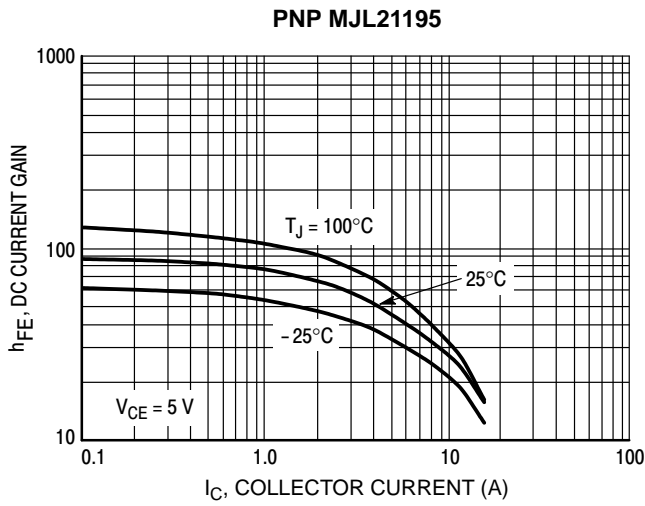


Figure 5. DC Current Gain,  $V_{CE} = 5\text{ V}$

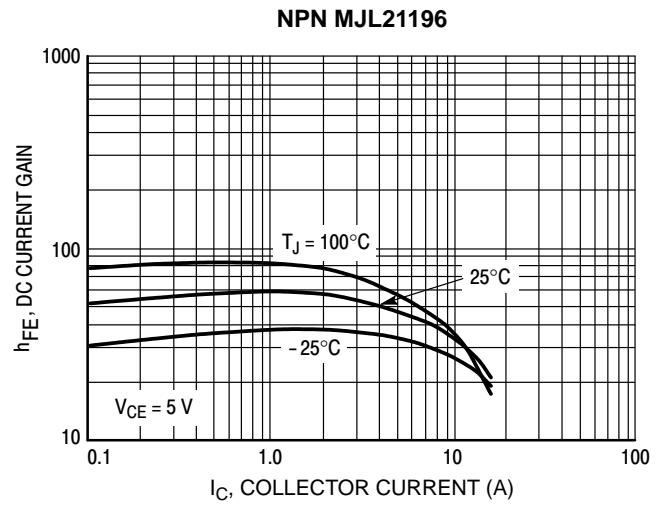


Figure 6. DC Current Gain,  $V_{CE} = 5\text{ V}$

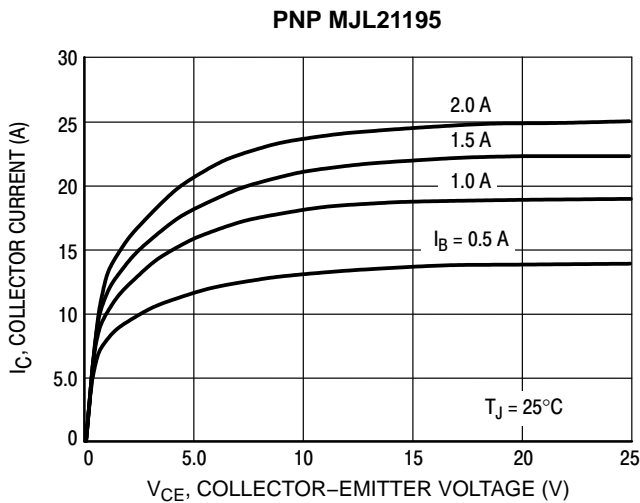


Figure 7. Typical Output Characteristics

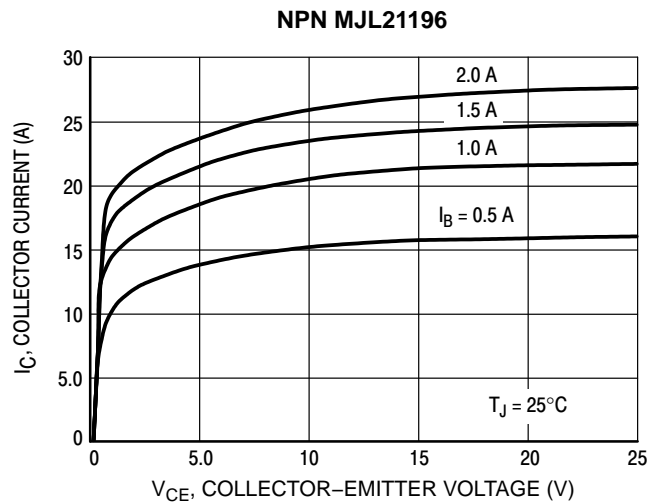
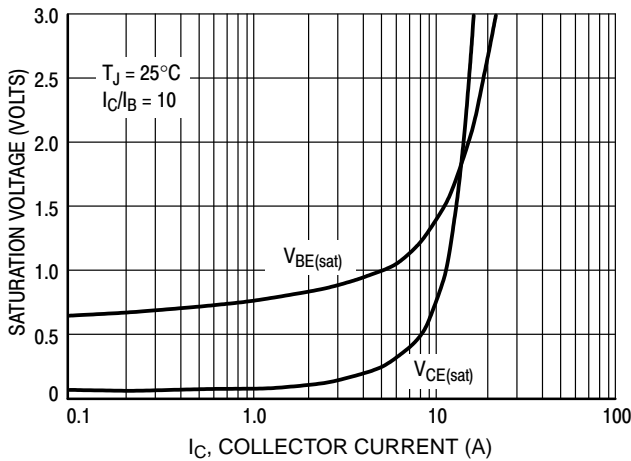


Figure 8. Typical Output Characteristics

# MJL21195 (PNP), MJL21196 (NPN)

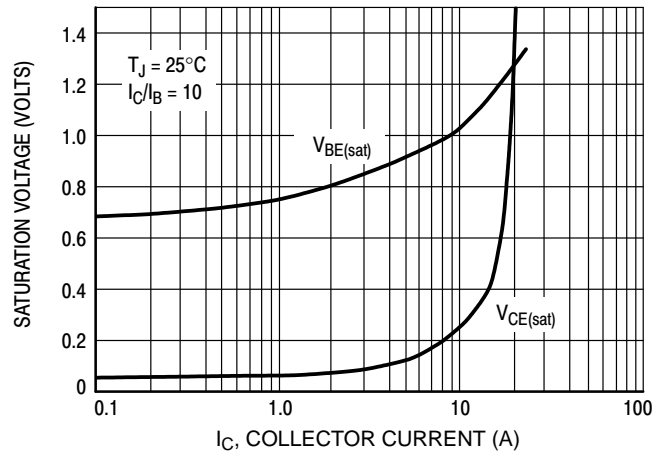
## TYPICAL CHARACTERISTICS

**PNP MJL21195**



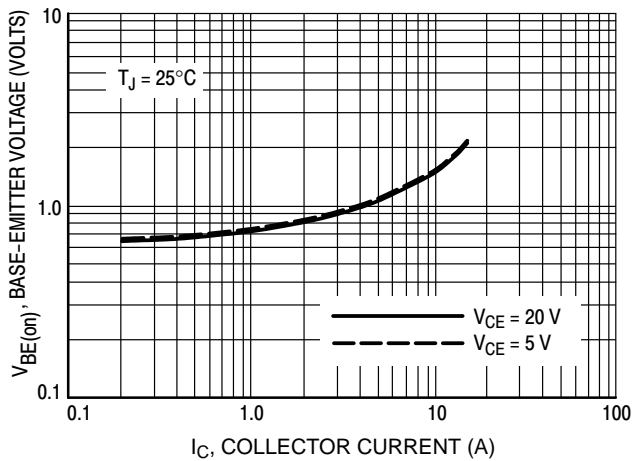
**Figure 9. Typical Saturation Voltages**

**NPN MJL21196**



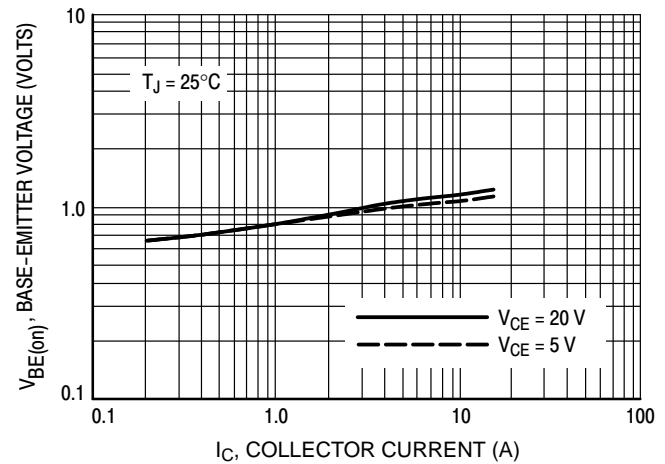
**Figure 10. Typical Saturation Voltages**

**PNP MJL21195**

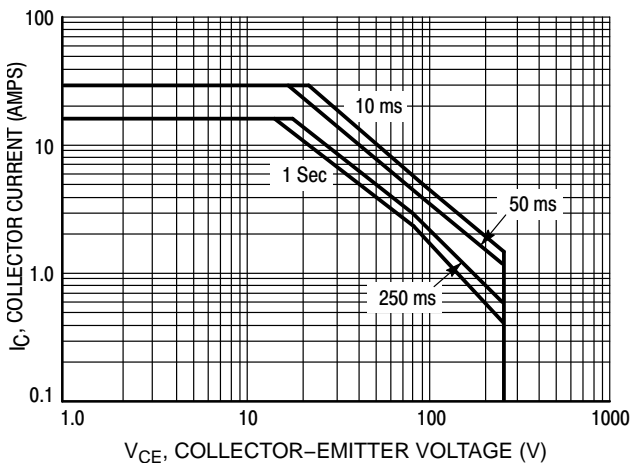


**Figure 11. Typical Base-Emitter Voltage**

**NPN MJL21196**



**Figure 12. Typical Base-Emitter Voltage**



**Figure 13. Active Region Safe Operating Area**

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

## MJL21195 (PNP), MJL21196 (NPN)

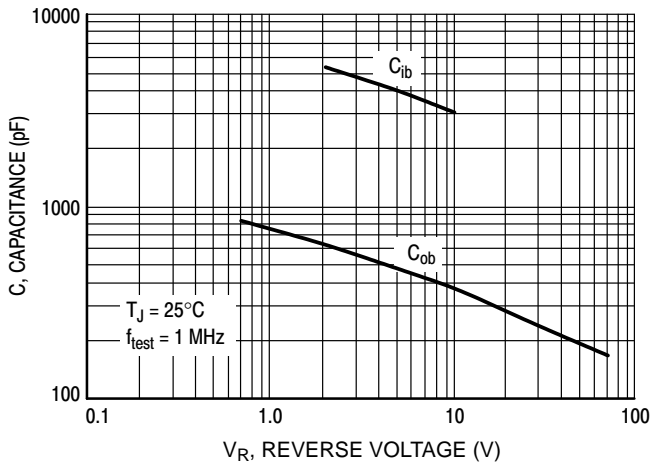


Figure 14. MJL21195 Typical Capacitance

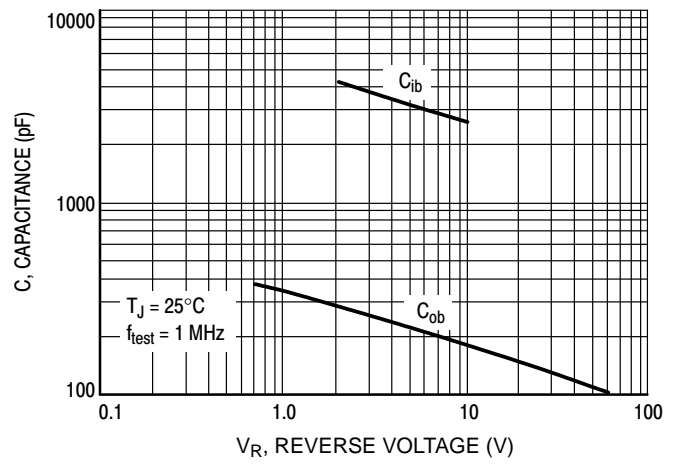


Figure 15. MJL21196 Typical Capacitance

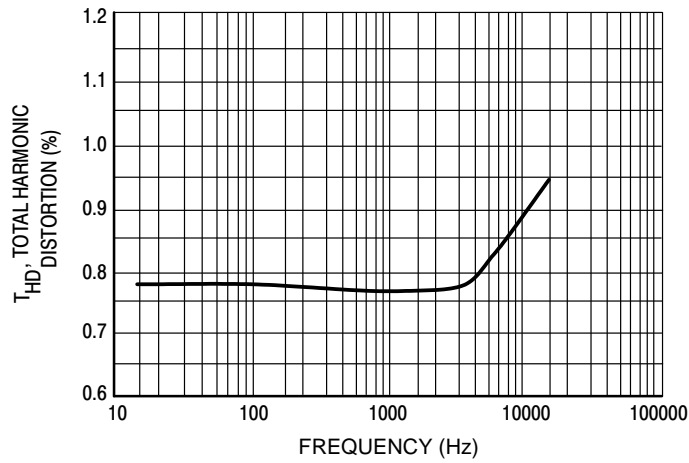


Figure 16. Typical Total Harmonic Distortion

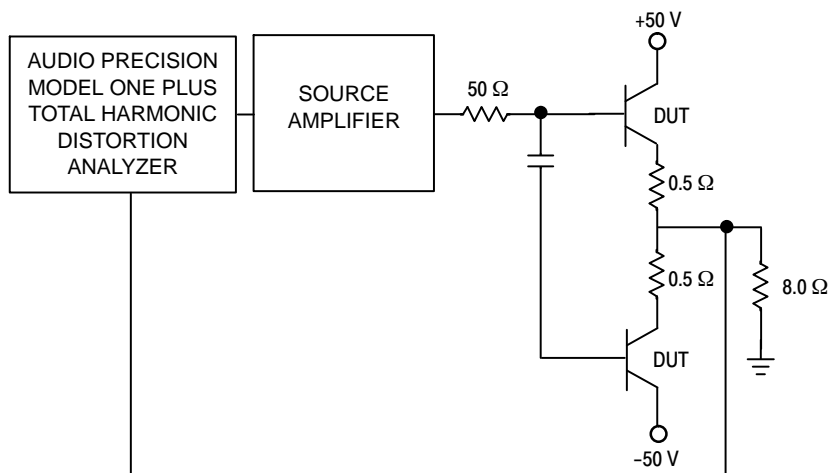
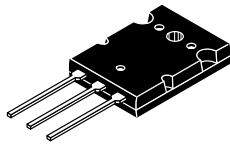


Figure 17. Total Harmonic Distortion Test Circuit

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

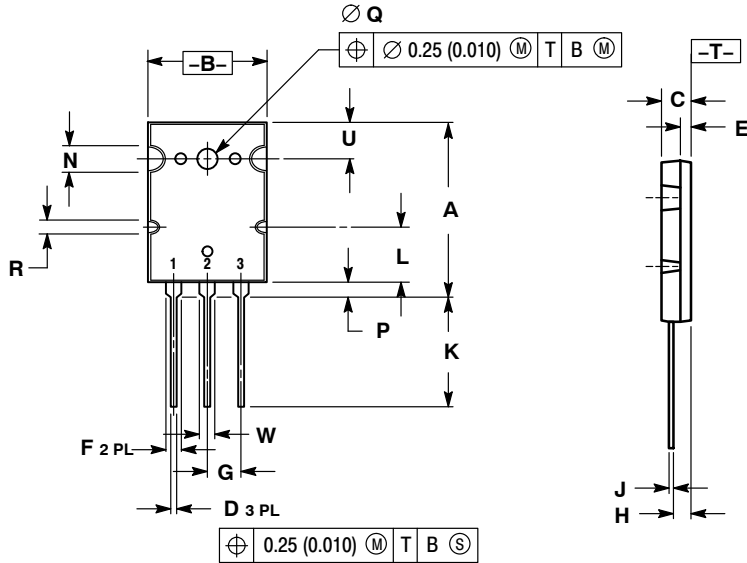
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TO-3BPL (TO-264)  
CASE 340G-02  
ISSUE J

DATE 17 DEC 2004

SCALE 1:2

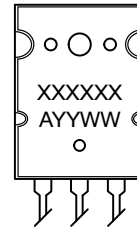


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	28.0	29.0	1.102	1.142
B	19.3	20.3	0.760	0.800
C	4.7	5.3	0.185	0.209
D	0.93	1.48	0.037	0.058
E	1.9	2.1	0.075	0.083
F	2.2	2.4	0.087	0.102
G	5.45 BSC		0.215 BSC	
H	2.6	3.0	0.102	0.118
J	0.43	0.78	0.017	0.031
K	17.6	18.8	0.693	0.740
L	11.2 REF		0.411 REF	
N	4.35 REF		0.172 REF	
P	2.2	2.6	0.087	0.102
Q	3.1	3.5	0.122	0.137
R	2.25 REF		0.089 REF	
U	6.3 REF		0.248 REF	
W	2.8	3.2	0.110	0.125

### GENERIC MARKING DIAGRAM\*

- |  |   |  |  |   |
|--|---|--|--|---|
| STYLE 1:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE | STYLE 2:<br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER | STYLE 3:<br>PIN 1. GATE<br>2. SOURCE<br>3. DRAIN | STYLE 4:<br>PIN 1. DRAIN<br>2. SOURCE<br>3. GATE | STYLE 5:<br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER |
|--|---|--|--|---|



- XXXXXX = Specific Device Code  
A = Location Code  
YY = Year  
WW = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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