

Negative Voltage Regulators

100 mA

MC79L00A Series

The MC79L00A Series negative voltage regulators are inexpensive, easy-to-use devices suitable for numerous applications requiring up to 100 mA. Like the higher powered MC7900 Series negative regulators, this series features thermal shutdown and current limiting, making them remarkably rugged. In most applications, no external components are required for operation.

The MC79L00A devices are useful for on-card regulation or any other application where a regulated negative voltage at a modest current level is needed. These regulators offer substantial advantage over the common resistor/Zener diode approach.

Features

- No External Components Required
- Internal Short Circuit Current Limiting
- Internal Thermal Overload Protection
- Low Cost
- Complementary Positive Regulators Offered (MC78L00 Series)
- Pb-Free Packages are Available



* Automotive temperature range selections are available with special test conditions and additional tests in 5, 12 and 15 V devices. Contact your local ON Semiconductor sales office for information.

Figure 1. Representative Schematic Diagram

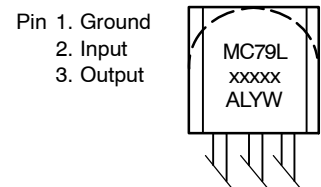
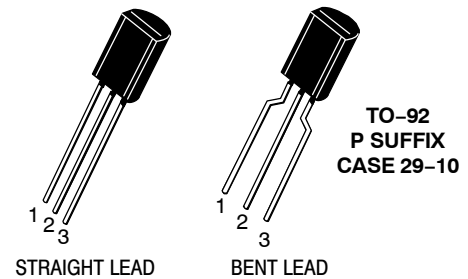


ON Semiconductor®

www.onsemi.com

THREE-TERMINAL LOW CURRENT NEGATIVE FIXED VOLTAGE REGULATORS

MARKING DIAGRAMS



- xxx = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- y = B or C

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

MC79L00A Series

MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (-5 V) (-12, -15, -18 V) (-24 V)	V_I	-30 -35 -40	Vdc
Power Dissipation Case 29 (TO-92 Type) $T_A = 25^\circ\text{C}$ Thermal Resistance, Junction-to-Ambient Thermal Resistance, Junction-to-Case	PD $R_{\theta JA}$ $R_{\theta JC}$	Internally Limited 160 83	W $^\circ\text{C/W}$ $^\circ\text{C/W}$
Case 751 (SOIC-8 Type) (Note 1) $T_A = 25^\circ\text{C}$ Thermal Resistance, Junction-to-Ambient Thermal Resistance, Junction-to-Case	PD $R_{\theta JA}$ $R_{\theta JC}$	Internally Limited 180 45	W $^\circ\text{C/W}$ $^\circ\text{C/W}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Junction Temperature	T_J	+150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. SOIC-8 Junction-to-Ambient Thermal Resistance is for minimum recommended pad size. Refer to Figure 9 for Thermal Resistance variation versus pad size.

*This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL_STD_883, Method 3015
Machine Model Method 200 V.

ELECTRICAL CHARACTERISTICS ($V_I = -10\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\ \mu\text{F}$, $C_O = 0.1\ \mu\text{F}$, $-40^\circ\text{C} < T_J < +125^\circ\text{C}$ (for MC79LXXAB), $0^\circ\text{C} < T_J < +125^\circ\text{C}$ (for MC79LXXAC)).

Characteristics	Symbol	MC79L05AC, AB			Unit
		Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-4.8	-5.0	-5.2	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$) -7.0 Vdc $\geq V_I \geq -20\text{ Vdc}$ -8.0 Vdc $\geq V_I \geq -20\text{ Vdc}$	Reg_{line}	-	-	150 100	mV
Load Regulation $T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$ $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	Reg_{load}	-	-	60 30	mV
Output Voltage -7.0 Vdc $\geq V_I \geq -20\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$ $V_I = -10\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$	V_O	-4.75 -4.75	-	-5.25 -5.25	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	-	-	6.0 5.5	mA
Input Bias Current Change -8.0 Vdc $\geq V_I \geq -20\text{ Vdc}$ $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	I_{IB}	-	-	1.5 0.1	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	-	40	-	μV
Ripple Rejection ($-8.0 \geq V_I \geq -18\text{ Vdc}$, $f = 120\text{ Hz}$, $T_J = +25^\circ\text{C}$)	RR	41	49	-	dB
Dropout Voltage ($I_O = 40\text{ mA}$, $T_J = +25^\circ\text{C}$)	$ V_I - V_O $	-	1.7	-	Vdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

MC79L00A Series

ELECTRICAL CHARACTERISTICS ($V_I = -19\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $-40^\circ\text{C} < T_J + 125^\circ\text{C}$ (for MC79LXXAB), $0^\circ\text{C} < T_J < +125^\circ\text{C}$ (for MC79LXXAC)).

Characteristics	Symbol	MC79L12AC, AB			Unit
		Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-11.5	-12	-12.5	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$) -14.5 Vdc $\geq V_I \geq -27\text{ Vdc}$ -16 Vdc $\geq V_I \geq -27\text{ Vdc}$	Reg_{line}	-	-	250 200	mV
Load Regulation $T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$ $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	Reg_{load}	-	-	100 50	mV
Output Voltage -14.5 Vdc $\geq V_I \geq -27\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$ $V_I = -19\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$	V_O	-11.4 -11.4	-	-12.6 -12.6	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	-	-	6.5 6.0	mA
Input Bias Current Change -16 Vdc $\geq V_I \geq -27\text{ Vdc}$ $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	I_{IB}	-	-	1.5 0.2	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	-	80	-	μV
Ripple Rejection ($-15 \leq V_I \leq -25\text{ Vdc}$, $f = 120\text{ Hz}$, $T_J = +25^\circ\text{C}$)	RR	37	42	-	dB
Dropout Voltage ($I_O = 40\text{ mA}$, $T_J = +25^\circ\text{C}$)	$ V_I - V_O $	-	1.7	-	Vdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ELECTRICAL CHARACTERISTICS ($V_I = -23\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $-40^\circ\text{C} < T_J + 125^\circ\text{C}$ (for MC79LXXAB), $0^\circ\text{C} < T_J < +125^\circ\text{C}$ (for MC79LXXAC)).

Characteristics	Symbol	MC79L15AC, AB			Unit
		Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-14.4	-15	-15.6	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$) -17.5 Vdc $\geq V_I \geq -30\text{ Vdc}$ -20 Vdc $\geq V_I \geq -30\text{ Vdc}$	Reg_{line}	-	-	300 250	mV
Load Regulation $T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$ $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	Reg_{load}	-	-	150 75	mV
Output Voltage -17.5 Vdc $\geq V_I \geq -\text{Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$ $V_I = -23\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$	V_O	-14.25 -14.25	-	-15.75 -15.75	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	-	-	6.5 6.0	mA
Input Bias Current Change -20 Vdc $\geq V_I \geq -30\text{ Vdc}$ $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	ΔI_{IB}	-	-	1.5 0.1	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	-	90	-	μV
Ripple Rejection ($-18.5 \leq V_I \leq -28.5\text{ Vdc}$, $f = 120\text{ Hz}$)	RR	34	39	-	dB
Dropout Voltage $I_O = 40\text{ mA}$, $T_J = +25^\circ\text{C}$	$ V_I - V_O $	-	1.7	-	Vdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

MC79L00A Series

ELECTRICAL CHARACTERISTICS ($V_I = -27\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $-40^\circ\text{C} < T_J < +125^\circ\text{C}$ (for MC79LXXAB), $0^\circ\text{C} < T_J < +125^\circ\text{C}$ (for MC79LXXAC), unless otherwise noted).

Characteristics	Symbol	MC79L18AC			Unit
		Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-17.3	-18	-18.7	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$) -20.7 Vdc $\geq V_I \geq -33\text{ Vdc}$ -21.4 Vdc $\geq V_I \geq -33\text{ Vdc}$ -22 Vdc $\geq V_I \geq -33\text{ Vdc}$ -21 Vdc $\geq V_I \geq -33\text{ Vdc}$	Reg _{line}	-	-	325 - - 275	mV
Load Regulation $T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$ $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	Reg _{load}	-	-	170 85	mV
Output Voltage -20.7 Vdc $\geq V_I \geq -33\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$ -21.4 Vdc $\geq V_I \geq -33\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$ $V_I = -27\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$	V_O	-17.1 - -17.1	- - -	-18.9 - -18.9	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	- -	- -	6.5 6.0	mA
Input Bias Current Change -21 Vdc $\geq V_I \geq -33\text{ Vdc}$ -27 Vdc $\geq V_I \geq -33\text{ Vdc}$ $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	I_{IB}	- - -	- - -	1.5 - 0.1	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	-	150	-	μV
Ripple Rejection ($-23 \leq V_I \leq -33\text{ Vdc}$, $f = 120\text{ Hz}$, $T_J = +25^\circ\text{C}$)	RR	33	48	-	dB
Dropout Voltage $I_O = 40\text{ mA}$, $T_J = +25^\circ\text{C}$	$ V_I - V_O $	-	1.7	-	Vdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ELECTRICAL CHARACTERISTICS ($V_I = -33\text{ V}$, $I_O = 40\text{ mA}$, $C_I = 0.33\text{ }\mu\text{F}$, $C_O = 0.1\text{ }\mu\text{F}$, $-40^\circ\text{C} < T_J < +125^\circ\text{C}$ (for MC79LXXAB), $0^\circ\text{C} < T_J < +125^\circ\text{C}$ (for MC79LXXAC), unless otherwise noted).

Characteristics	Symbol	MC79L24AC			Unit
		Min	Typ	Max	
Output Voltage ($T_J = +25^\circ\text{C}$)	V_O	-23	-24	-25	Vdc
Input Regulation ($T_J = +25^\circ\text{C}$) -27 Vdc $\geq V_I \geq -38\text{ Vdc}$ -27.5 Vdc $\geq V_I \geq -38\text{ Vdc}$ -28 Vdc $\geq V_I \geq -38\text{ Vdc}$	Reg _{line}	- - -	- - -	350 - 300	mV
Load Regulation $T_J = +25^\circ\text{C}$, $1.0\text{ mA} \leq I_O \leq 100\text{ mA}$ $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	Reg _{load}	- -	- -	200 100	mV
Output Voltage -27 Vdc $\geq V_I \geq -38\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$ -28 Vdc $\geq V_I \geq -38\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$ $V_I = -33\text{ Vdc}$, $1.0\text{ mA} \leq I_O \leq 70\text{ mA}$	V_O	-22.8 - -22.8	- - -	-25.2 - -25.2	Vdc
Input Bias Current ($T_J = +25^\circ\text{C}$) ($T_J = +125^\circ\text{C}$)	I_{IB}	- -	- -	6.5 6.0	mA
Input Bias Current Change -28 Vdc $\geq V_I \geq -38\text{ Vdc}$ $1.0\text{ mA} \leq I_O \leq 40\text{ mA}$	ΔI_{IB}	- -	- -	1.5 0.1	mA
Output Noise Voltage ($T_A = +25^\circ\text{C}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$)	V_n	-	200	-	μV
Ripple Rejection ($-29 \leq V_I \leq -35\text{ Vdc}$, $f = 120\text{ Hz}$, $T_J = +25^\circ\text{C}$)	RR	31	47	-	dB
Dropout Voltage $I_O = 40\text{ mA}$, $T_J = +25^\circ\text{C}$	$ V_I - V_O $	-	1.7	-	Vdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

MC79L00A Series

APPLICATIONS INFORMATION

Design Considerations

The MC79L00A Series of fixed voltage regulators are designed with Thermal Overload Protections that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire length, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good

high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

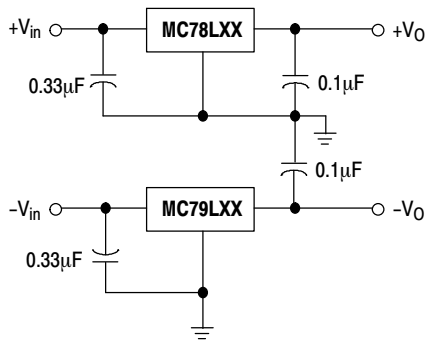
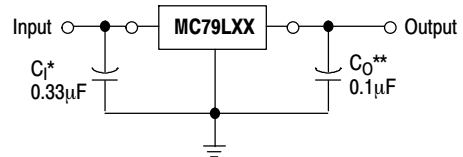


Figure 2. Positive and Negative Regulator



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the ripple voltage.

* C_I is required if regulator is located an appreciable distance from the power supply filter

** C_O improves stability and transient response.

Figure 3. Standard Application

MC79L00A Series

TYPICAL CHARACTERISTICS

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

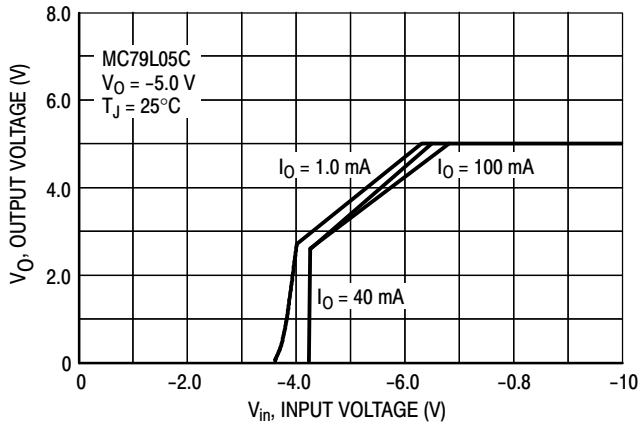


Figure 4. Dropout Characteristics

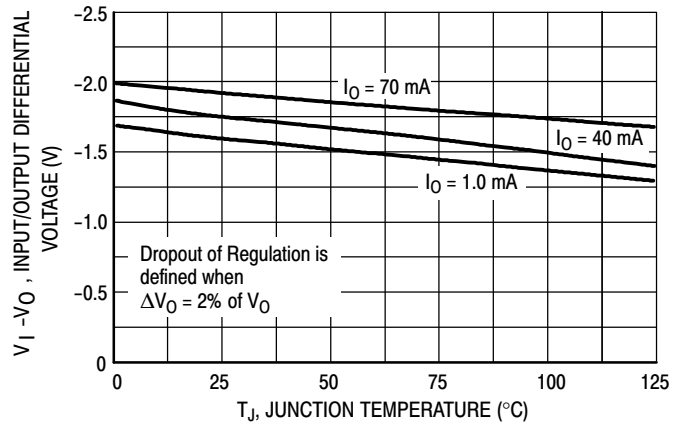


Figure 5. Dropout Voltage versus Junction Temperature

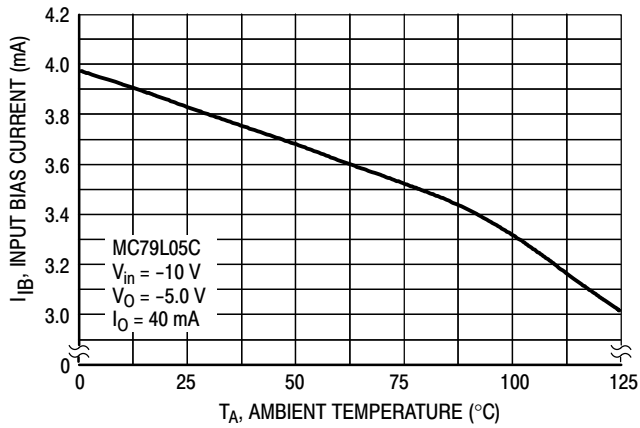


Figure 6. Input Bias Current versus Ambient Temperature

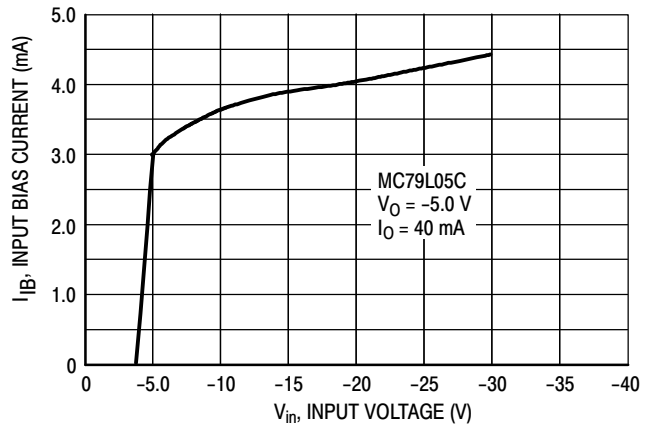


Figure 7. Input Bias Current versus Input Voltage

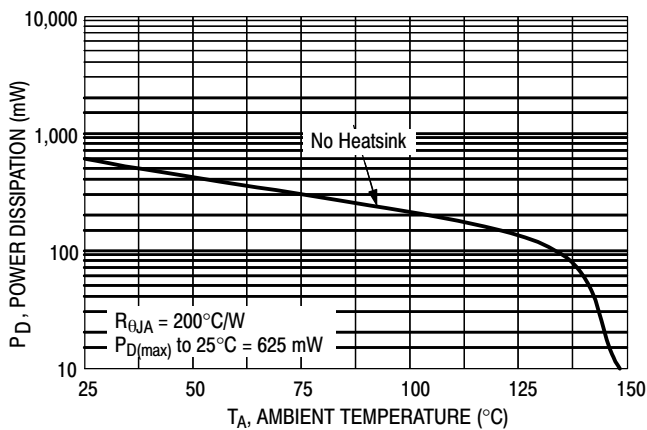


Figure 8. Maximum Average Power Dissipation versus Ambient Temperature (TO-92)

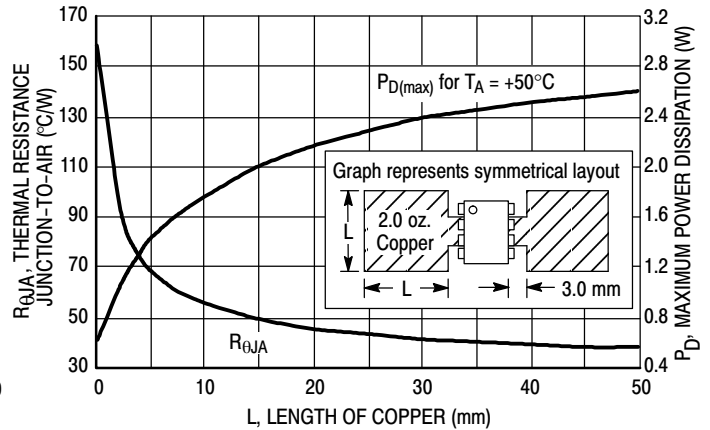


Figure 9. SOP-8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

MC79L00A Series

ORDERING INFORMATION

Device	Nominal Voltage	Operating Temperature Range	Package	Shipping [†]
MC79L05ABDG	-5.0 V	TJ = -40° to +125°C	SOIC-8 (Pb-Free)	98 Units / Rail
MC79L05ABDR2G			SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC79L05ABPG			TO-92 (Pb-Free)	2000 Units / Bag
MC79L05ABPRAG			TO-92 (Pb-Free)	2000 / Tape & Reel
MC79L05ACDG		TJ = 0° to +125°C	SOIC-8 (Pb-Free)	98 Units / Rail
MC79L05ACDR2G			SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC79L05ACPG			TO-92 (Pb-Free)	2000 Units / Bag
MC79L05ACPRAG			TO-92 (Pb-Free)	2000 / Tape & Reel
MC79L05ACPRMG			TO-92 (Pb-Free)	2000 / Tape & Ammo Box
MC79L05ACPRPG			TO-92 (Pb-Free)	2000 / Tape & Ammo Box
MC79L12ABDG	-12 V	TJ = -40° to +125°C	SOIC-8 (Pb-Free)	98 Units / Rail
MC79L12ABDR2G			SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC79L12ABPG			TO-92 (Pb-Free)	2000 Units / Bag
MC79L12ABPRAG			TO-92 (Pb-Free)	2000 / Tape & Reel
MC79L12ACDG	-12 V	TJ = 0° to +125°C	SOIC-8 (Pb-Free)	98 Units / Rail
MC79L12ACDR2G			SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC79L12ACPG			TO-92 (Pb-Free)	2000 Units / Bag
MC79L12ACPRAG			TO-92 (Pb-Free)	2000 / Tape & Reel
MC79L12ACPRPG			TO-92 (Pb-Free)	2000 / Tape & Ammo Box

MC79L00A Series

ORDERING INFORMATION (continued)

Device	Nominal Voltage	Operating Temperature Range	Package	Shipping†		
MC79L15ABDG	-15 V	TJ = -40° to +125°C	SOIC-8 (Pb-Free)	98 Units / Rail		
MC79L15ABDR2G			SOIC-8 (Pb-Free)	2500 / Tape & Reel		
MC79L15ABPG			TO-92 (Pb-Free)	2000 Units / Bag		
MC79L15ABPRPG			TO-92 (Pb-Free)	2000 / Tape & Ammo Box		
MC79L15ACDG	-15 V	TJ = 0° to +125°C	SOIC-8 (Pb-Free)	98 Units / Rail		
MC79L15ACDR2G			SOIC-8 (Pb-Free)	2500 / Tape & Reel		
MC79L15ACPG			TO-92 (Pb-Free)	2000 Units / Bag		
MC79L15ACPRAG			TO-92 (Pb-Free)	2000 / Tape & Reel		
MC79L15ACPREG			TO-92 (Pb-Free)	2000 / Tape & Reel		
MC79L15ACPRPG			TO-92 (Pb-Free)	2000 / Tape & Ammo Box		
MC79L18ABPRPG			-18 V	TJ = -40° to +125°C	TO-92 (Pb-Free)	2000 / Tape & Ammo Box
MC79L18ACPG				TJ = 0° to +125°C	TO-92 (Pb-Free)	2000 Units / Bag
MC79L24ABPG	-24 V	TJ = -40° to +125°C	TO-92 (Pb-Free)	2000 Units / Bag		
MC79L24ACPG		TJ = 0° to +125°C	TO-92 (Pb-Free)	2000 Units / Bag		
MC79L24ACPRMG			TO-92 (Pb-Free)	2000 / Tape & Ammo Box		
MC79L24ACPRPG			TO-92 (Pb-Free)	2000 / Tape & Ammo Box		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

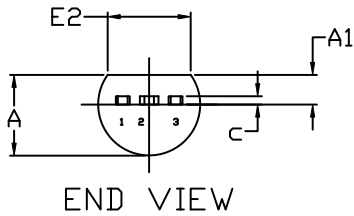
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



TO-92 (TO-226) 1 WATT
CASE 29-10
ISSUE D

DATE 05 MAR 2021

STRAIGHT LEAD



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	1.27 BSC		
L	13.80	14.00	14.20

STYLES AND MARKING ON PAGE 3

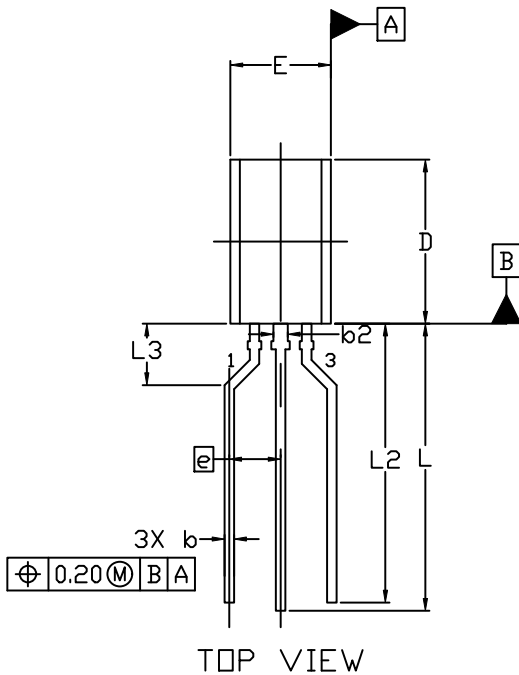
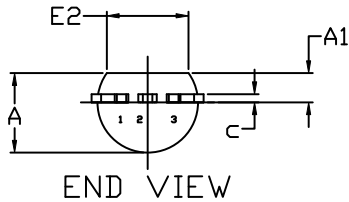
DOCUMENT NUMBER:	98AON52857E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TO-92 (TO-226) 1 WATT	PAGE 1 OF 3

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

TO-92 (TO-226) 1 WATT
CASE 29-10
ISSUE D

DATE 05 MAR 2021

FORMED LEAD




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	2.50 BSC		
L	13.80	14.00	14.20
L2	13.20	13.60	14.00
L3	3.00 REF		

STYLES AND MARKING ON PAGE 3

DOCUMENT NUMBER:	98AON52857E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TO-92 (TO-226) 1 WATT	PAGE 2 OF 3

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**TO-92 (TO-226) 1 WATT
CASE 29-10
ISSUE D**

DATE 05 MAR 2021

- | | | | | |
|---|--|--|---|---|
| STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR | STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR | STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE | STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE | STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE |
| STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN | STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE | STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE | STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2 | STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE |
| STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE | STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2 | STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2 | STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE | STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2 |
| STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE | STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER | STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED | STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE | STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE |
| STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE | STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN | STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN | STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE | STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2 |
| STYLE 26:
PIN 1. V _{CC}
2. GROUND 2
3. OUTPUT | STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT | STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE | STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE | STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE |
| STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE | STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER | STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT | STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC | STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER |

**GENERIC
MARKING DIAGRAM***



- XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON52857E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TO-92 (TO-226) 1 WATT	PAGE 3 OF 3

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

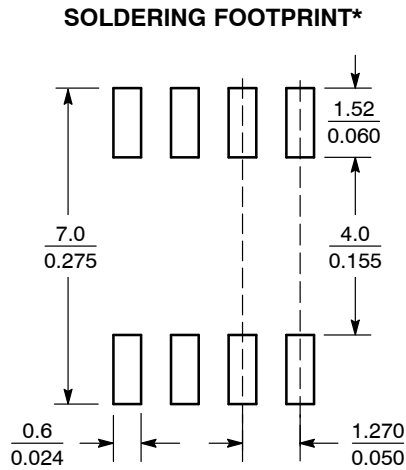
DATE 16 FEB 2011



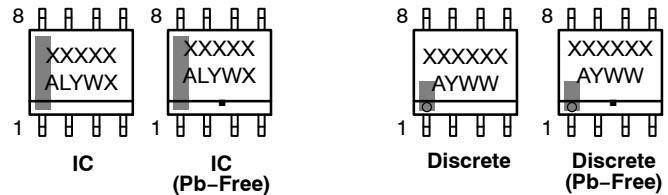
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC MARKING DIAGRAM*



SCALE 6:1 ($\frac{\text{mm}}{\text{inches}}$)



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

onsemi and ONsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|---|--|--|--|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC_OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 2 OF 2

onsemi and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales