MC74LV594A

8-Bit Shift Register with Output Register

The MC74LV594A is an 8−bit shift register designed for 2 V to 6.0 V V_{CC} operation. The device contain an 8−bit serial−in, parallel−out shift register that feeds an 8−bit D−type storage register. Separate clocks (RCLK, SRCLK) and direct overriding clear ($\overline{RCLR}$, $\overline{SRCLR}$) inputs are provided on the shift and storage registers. A serial output ($Q_{H'}$) is provided for cascading purposes.

The shift−register (SRCLK) and storage−register (RCLK) clocks are positive−edge triggered. If the clocks are tied together, the shift register always is one clock pulse ahead of the storage register.

Features

- 2.0 V to 6.0 V V_{CC} Operation
- Low Input Current: 1.0 μA
- Max t_{pd} of 6.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (V_{OH} Undershoot) > 2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- Support Mixed−Mode Voltage Operation on All Ports
- 8−Bit Serial−In, Parallel−Out Shift Registers With Storage
- Independent Direct Overriding Clears on Shift and Storage Registers
- Independent Clocks for Shift and Storage Registers
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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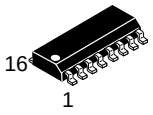
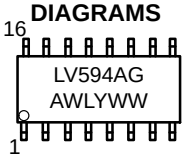
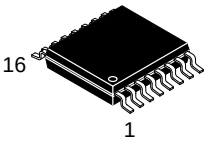
MARKING DIAGRAMS

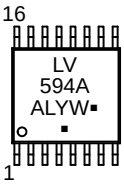


SOIC−16
D SUFFIX
CASE 751B





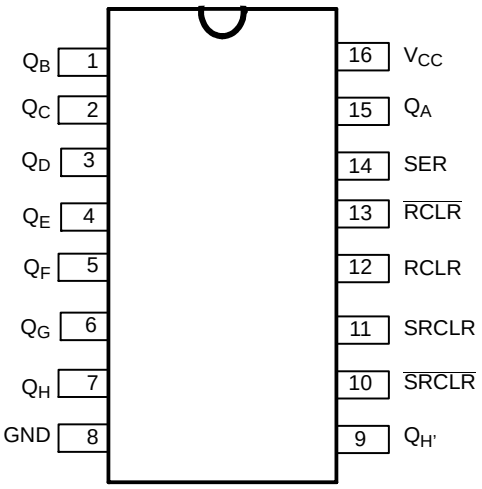
TSSOP−16
DT SUFFIX
CASE 948F



A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week
G or ▪	=	Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{RCLR}}$	
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of shift register goes high. Other stages store the data of previous stage, respectively.
L	↓	H	X	X	Shift register state is not changed.
X	X	X	X	L	Storage register is cleared.
X	X	X	↑	H	Shift register data is stored in the storage register.
X	X	X	↓	H	Storage register state is not changed.

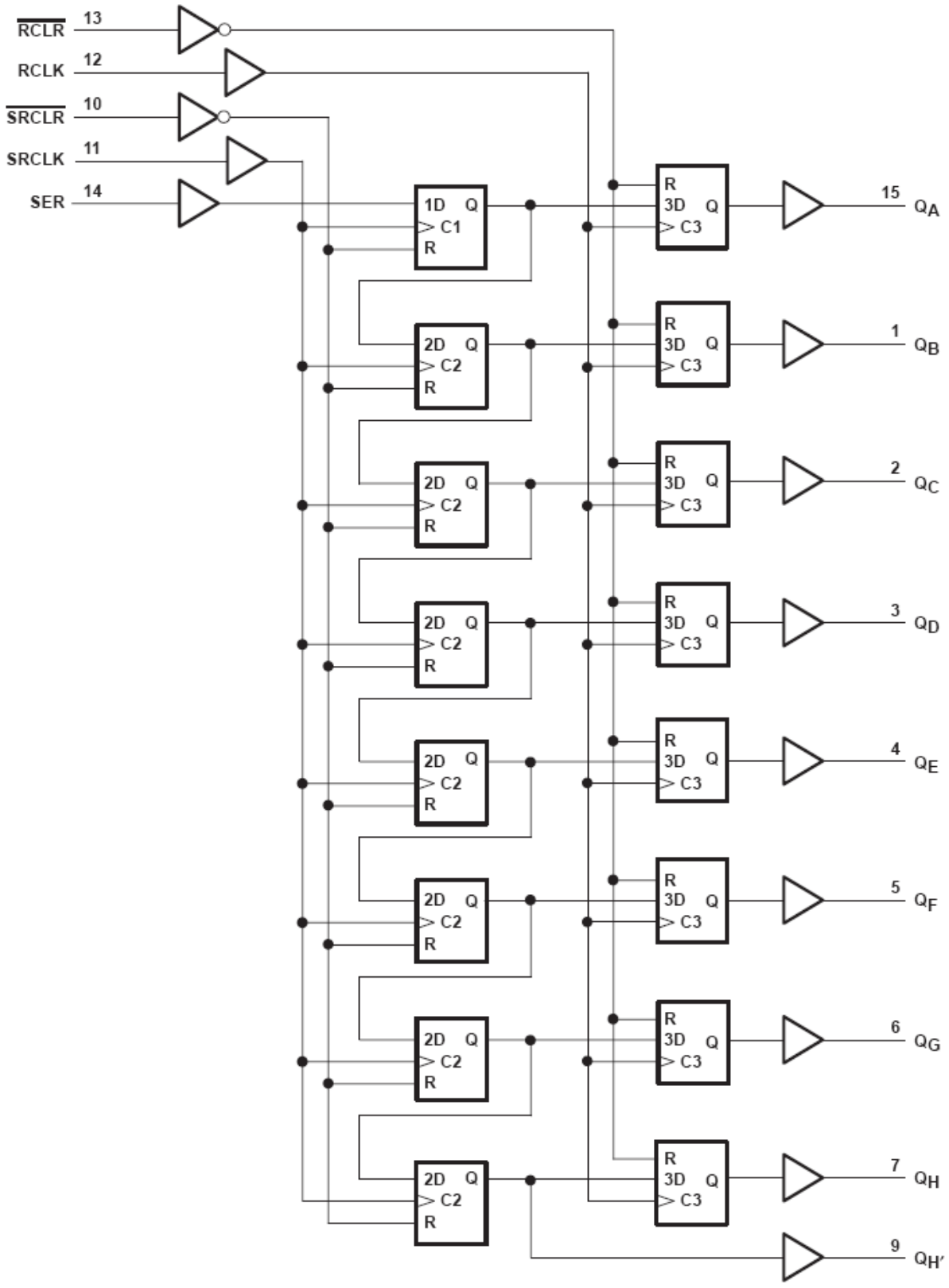


Figure 1. Logic Diagram

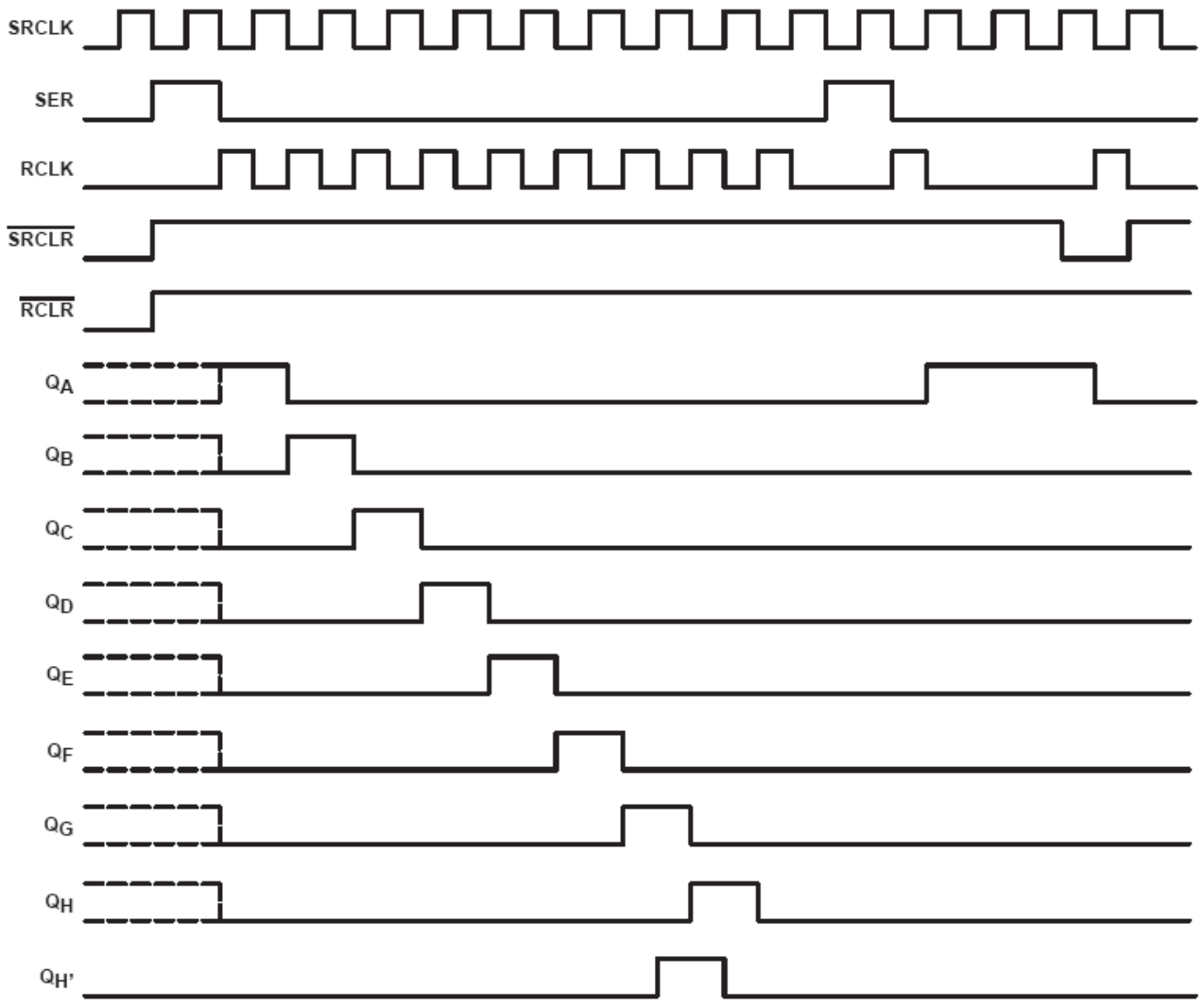


Figure 2. Timing Diagram

ORDERING INFORMATION

Device	Package	Shipping†
MC74LV594ADR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel
MC74LV594ADTR2G	TSSOP−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	−0.5 to +7.0	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage Active Mode (Note 1)	−0.5 to V_{CC} + 0.5	V
	High Impedance or Power−Off Mode	−0.5 to +7.0	
I_{IK}	DC Input Clamp Current	±20	mA
I_{OK}	DC Output Clamp Current	±35	mA
I_{IN}	DC Input Current	±20	mA
I_O	DC Output Source / Sink Current	±35	mA
I_{CC}	DC Supply Current per Supply Pin	±75	mA
I_{GND}	DC Ground Current per Ground Pin	±75	mA
T_{STG}	Storage Temperature Range	−65 to +150	°C
T_L	Lead temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction temperature under Bias	+150	°C
θ_{JA}	Thermal Resistance SOIC TSSOP	112 148	°C
P_D	Power Dissipation in Still Air at SOIC TSSOP	500 450	mW
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 30% − 35%	UL−94−VO (0.125 in)	
V_{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 3000 >400 N/A	V
$I_{Latchup}$	Latchup Performance Above V_{CC} and Below GND at 85°C (Note 5)	±300	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Tested to EIA/JESD22−A114−A.
3. Tested to EIA/JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS (Note 6)

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_I	DC Input Voltage (Referenced to GND)		0	V_{CC}	V
V_O	DC Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Free−Air Temperature		−55	+85	°C
t_r, t_f	Input Rise or Fall Rate	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	nS

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC}, (V)	Guaranteed Limits					Unit
				T_A = 25°C			T_A = −55°C to 125°C		
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High−Level Input Voltage		2.0	1.5			1.5		V
			2.3 – 6.0	0.7 x V_{CC}			0.7 x V_{CC}		
V_{IL}	Maximum Low−Level Input Voltage		2.0			0.5		0.5	V
			2.3 – 6.0			0.3 x V_{CC}		0.3 x V_{CC}	
V_{OH}	Minimum High−Level Output Voltage	V_{IN} = V_{IH} or V_{IL}							V
		I_{oH} = −50 μA	2.0 – 6.0	V_{CC} – 0.1			V_{CC} – 0.1		
		I_{oH} = −2 mA	2.3	2			2		
		I_{oH} = −6 mA	3.0	2.48			2.48		
		I_{oH} = −12 mA	4.5	3.8			3.8		
V_{OL}	Maximum Low−Level Output Voltage	V_{IN} = V_{IH} or V_{IL}							V
		I_{oH} = 50 μA	2.0 – 6.0			0.1		0.1	
		I_{oH} = 2 mA	2.3			0.4		0.4	
		I_{oH} = 6 mA	3.0			0.44		0.44	
		I_{oH} = 12 mA	4.5			0.55		0.55	
I_{IN}	Maximum Input Leakage Current	V_I = V_{CC} or GND	6.0		±0.1		±1		μA
I_{CC}	Maximum Supply Current	V_I = V_{CC} or GND, I_O = 0 A	6.0			8.0		80	μA
C_I	Input Capacitance	V_I = V_{CC} or GND	3.3		3.5				pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TIMING SPECIFICATIONS (See Figure 3)

Symbol	Parameter	Conditions	V_{CC}, (V)	T_A = 25°C		T_A = −55°C to 125°C		Unit
				Min	Max	Min	Max	
t_W	Pulse Duration	RCLK or SRCLK High or Low	2.3 – 2.7	7		7.5		ns
			3.0 – 3.6	5.5		5.5		
			4.5 – 5.5	5		5		
		$\overline{RCLR}$ or $\overline{SRCLR}$ Low	2.3 – 2.7	6		6.5		
			3.0 – 3.6	5		5		
			4.5 – 5.5	5.2		5.2		
t_{SU}	Setup Time	SER before SRCLK↑	2.3 – 2.7	5.5		5.5		ns
			3.0 – 3.6	3.5		3.5		
			4.5 – 5.5	3		3		
		SRCLK↑ before RCLK↑	2.3 – 2.7	8		9		
			3.0 – 3.6	8		8.5		
			4.5 – 5.5	5		5		
		$\overline{SRCLR}$ Low before RCLK↑	2.3 – 2.7	8.5		9.5		
			3.0 – 3.6	8		9		
			4.5 – 5.5	5		5		
		$\overline{SRCLR}$ High (Inactive) before SRCLK↑	2.3 – 2.7	6		6.8		
			3.0 – 3.6	4.2		4.8		
			4.5 – 5.5	2.9		3.3		
		$\overline{RCLR}$ High (Inactive) before RCLK↑	2.3 – 2.7	6.7		7.6		
			3.0 – 3.6	4.6		5.3		
			4.5 – 5.5	3.2		3.7		
t_H	Hold Time	SER after SRCLK↑	2.3 – 2.7	1.5		1.5		ns
			3.0 – 3.6	1.5		1.5		
			4.5 – 5.5	2		2		

AC CHARACTERISTICS (See Figure 3)

Symbol	Paraeter	Load Condi-tions	Input to Output	V_{CC}, (V)	Guaranteed Limits					Unit
					T_A = 25°C			T_A = −55°C to 125°C		
					Min	Typ	Max	Min	Max	
f_{MAX}		C_L = 15 pF		2.3 – 2.7	65	80		45		MHz
				3.0 – 3.6	80	120		70		
				4.5 – 5.5	135	170		115		
		C_L = 50 pF		2.3 – 2.7	50	51		40		
				3.0 – 3.6	70	74		55		
				4.5 – 5.5	115	120		90		
t_{PLH}	Propagation Delay Low to High	C_L = 15 pF	RCLK to Q_A–Q_H	2.3 – 2.7			27.5	1	32.5	ns
				3.0 – 3.6			18	1	22.5	
				4.5 – 5.5			12	1	15	
			SRCLK to $Q_{H'}$	2.3 – 2.7			27.5	1	32	
				3.0 – 3.6			18	1	22	
				4.5 – 5.5			12.5	1	12	
		C_L = 50 pF	RCLK to Q_A–Q_H	2.3 – 2.7		22.1	25.0	1	30.0	
				3.0 – 3.6		15.6	17.5	1	21.0	
				4.5 – 5.5		11.5	12.5	1	15.5	
			SRCLK to $Q_{H'}$	2.3 – 2.7		21.6	25.5	1	29.5	
				3.0 – 3.6		15.2	18.0	1	21.0	
				4.5 – 5.5		10.9	12.5	1	15.0	
t_{PHL}	Propagation Delay High to Low	C_L = 15 pF	RCLK to Q_A–Q_H	2.3 – 2.7			23	1	27.5	ns
				3.0 – 3.6			15.5	1	19	
				4.5 – 5.5			11	1	14	
			SRCLK to $Q_{H'}$	2.3 – 2.7			23.5	1	27	
				3.0 – 3.6			16	1	19	
				4.5 – 5.5			11	1	13.5	
			$\overline{RCLR}$ to Q_A–Q_H	2.3 – 2.7			20.5	1	25	
				3.0 – 3.6			14.5	1	17.5	
				4.5 – 5.5			10	1	12	
			$\overline{SRCLR}$ to $Q_{H'}$	2.3 – 2.7				1	23	
				3.0 – 3.6			13	1	16	
				4.5 – 5.5			9	1	11	
		C_L = 50 pF	RCLK to Q_A–Q_H	2.3 – 2.7		19.7	23.0	1	27.0	
				3.0 – 3.6		14.0	16.5	1	19.5	
				4.5 – 5.5		10.1	11.5	1	13.5	
			SRCLK to $Q_{H'}$	2.3 – 2.7		18.4	21.5	1	25.0	
				3.0 – 3.6		13.1	15.0	1	18.0	
				4.5 – 5.5		9.0	10.5	1	12.5	
			$\overline{RCLR}$ to Q_A–Q_H	2.3 – 2.7		25.7	30.0	1	35.0	
				3.0 – 3.6		17.6	20.0	1	24.5	
				4.5 – 5.5		12.2	13.5	1	17.0	
			$\overline{SRCLR}$ to $Q_{H'}$	2.3 – 2.7		25.3	30.0	1	34	
				3.0 – 3.6		17.3	20.0	1	24.0	
				4.5 – 5.5		11.9	14.0	1	16.5	

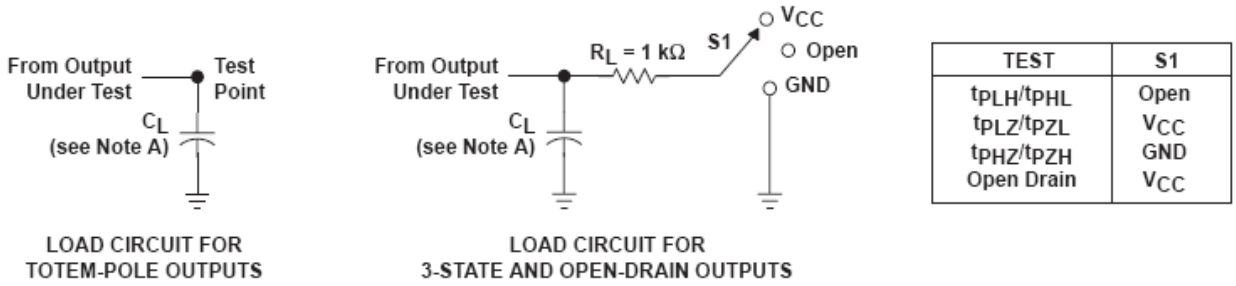
NOISE CHARACTERISTICS, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
$V_{OL(P)}$	Quiet Output, Maximum Dynamic V_{OL}		0.8	0.8	V
$V_{OL(V)}$	Quiet Output, Minimum Dynamic V_{OL}		−0.1	−0.8	V
$V_{OH(V)}$	Quiet Output, Minimum Dynamic V_{OH}		2.8		V
$V_{IH(D)}$	High−Level Dynamic Input Voltage	2.31			V
$V_{IL(D)}$	Low−Level Dynamic Input Voltage			0.99	V

POWER DISSIPATION CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	V_{CC} (V)	Typ	Unit
C_{PD}	Power Dissipation Capacitance	f = 10 MHz	3.3	93	pF
			5	112	

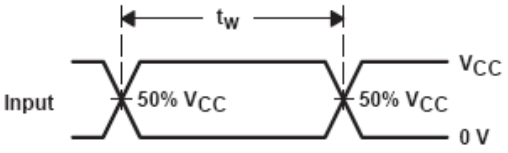
PARAMETER MEASUREMENT INFORMATION



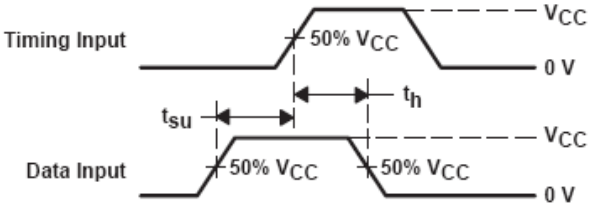
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

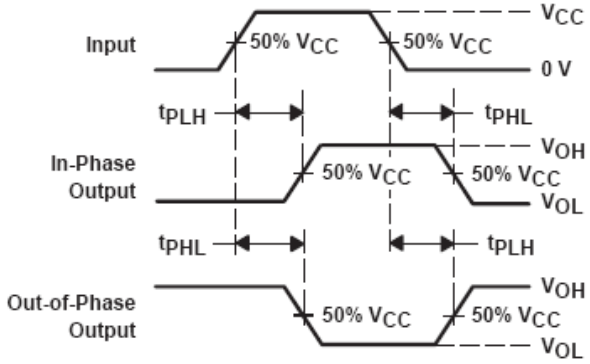
LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



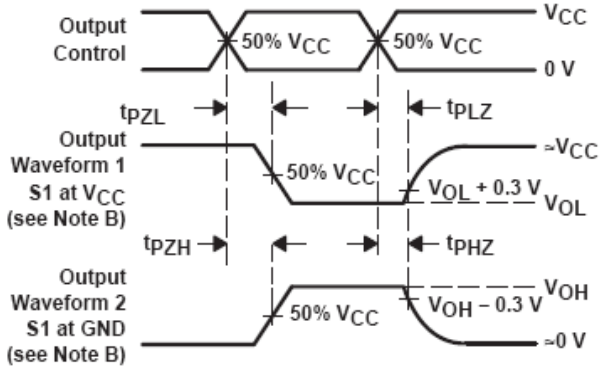
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

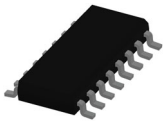


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

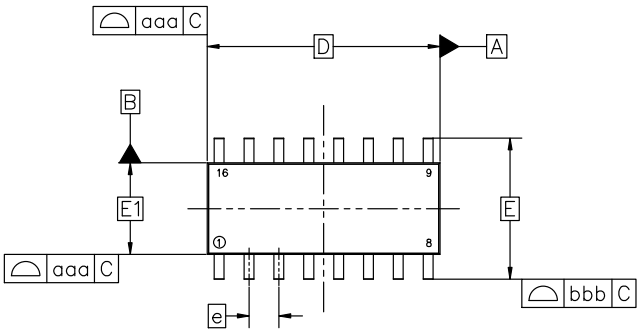
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



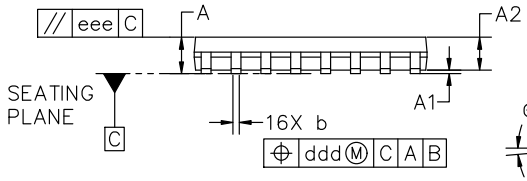
SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

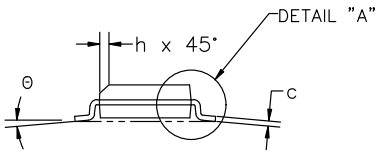
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



TOP VIEW

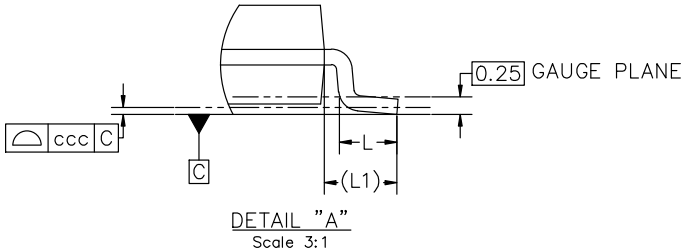


SIDE VIEW

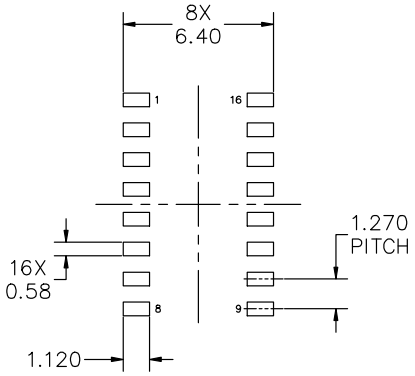


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



DETAIL "A"
Scale 3:1



RECOMMENDED MOUNTING FOOTPRINT

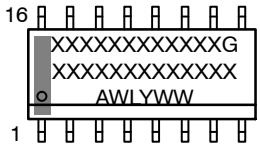
*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC−16 9.90X3.90X1.50 1.27P	PAGE 1 OF 2

SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

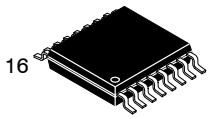
STYLE 1:		STYLE 2:		STYLE 3:		STYLE 4:	
PIN 1.	COLLECTOR	PIN 1.	CATHODE	PIN 1.	COLLECTOR, DYE #1	PIN 1.	COLLECTOR, DYE #1
2.	BASE	2.	ANODE	2.	BASE, #1	2.	COLLECTOR, #1
3.	EMITTER	3.	NO CONNECTION	3.	EMITTER, #1	3.	COLLECTOR, #2
4.	NO CONNECTION	4.	CATHODE	4.	COLLECTOR, #1	4.	COLLECTOR, #2
5.	EMITTER	5.	CATHODE	5.	COLLECTOR, #2	5.	COLLECTOR, #3
6.	BASE	6.	NO CONNECTION	6.	BASE, #2	6.	COLLECTOR, #3
7.	COLLECTOR	7.	ANODE	7.	EMITTER, #2	7.	COLLECTOR, #4
8.	COLLECTOR	8.	CATHODE	8.	COLLECTOR, #2	8.	COLLECTOR, #4
9.	BASE	9.	CATHODE	9.	COLLECTOR, #3	9.	BASE, #4
10.	EMITTER	10.	ANODE	10.	BASE, #3	10.	EMITTER, #4
11.	NO CONNECTION	11.	NO CONNECTION	11.	EMITTER, #3	11.	BASE, #3
12.	EMITTER	12.	CATHODE	12.	COLLECTOR, #3	12.	EMITTER, #3
13.	BASE	13.	CATHODE	13.	COLLECTOR, #4	13.	BASE, #2
14.	COLLECTOR	14.	NO CONNECTION	14.	BASE, #4	14.	EMITTER, #2
15.	EMITTER	15.	ANODE	15.	EMITTER, #4	15.	BASE, #1
16.	COLLECTOR	16.	CATHODE	16.	COLLECTOR, #4	16.	EMITTER, #1

STYLE 5:		STYLE 6:		STYLE 7:	
PIN 1.	DRAIN, DYE #1	PIN 1.	CATHODE	PIN 1.	SOURCE N-CH
2.	DRAIN, #1	2.	CATHODE	2.	COMMON DRAIN (OUTPUT)
3.	DRAIN, #2	3.	CATHODE	3.	COMMON DRAIN (OUTPUT)
4.	DRAIN, #2	4.	CATHODE	4.	GATE P-CH
5.	DRAIN, #3	5.	CATHODE	5.	COMMON DRAIN (OUTPUT)
6.	DRAIN, #3	6.	CATHODE	6.	COMMON DRAIN (OUTPUT)
7.	DRAIN, #4	7.	CATHODE	7.	COMMON DRAIN (OUTPUT)
8.	DRAIN, #4	8.	CATHODE	8.	SOURCE P-CH
9.	GATE, #4	9.	ANODE	9.	SOURCE P-CH
10.	SOURCE, #4	10.	ANODE	10.	COMMON DRAIN (OUTPUT)
11.	GATE, #3	11.	ANODE	11.	COMMON DRAIN (OUTPUT)
12.	SOURCE, #3	12.	ANODE	12.	COMMON DRAIN (OUTPUT)
13.	GATE, #2	13.	ANODE	13.	GATE N-CH
14.	SOURCE, #2	14.	ANODE	14.	COMMON DRAIN (OUTPUT)
15.	GATE, #1	15.	ANODE	15.	COMMON DRAIN (OUTPUT)
16.	SOURCE, #1	16.	ANODE	16.	SOURCE N-CH

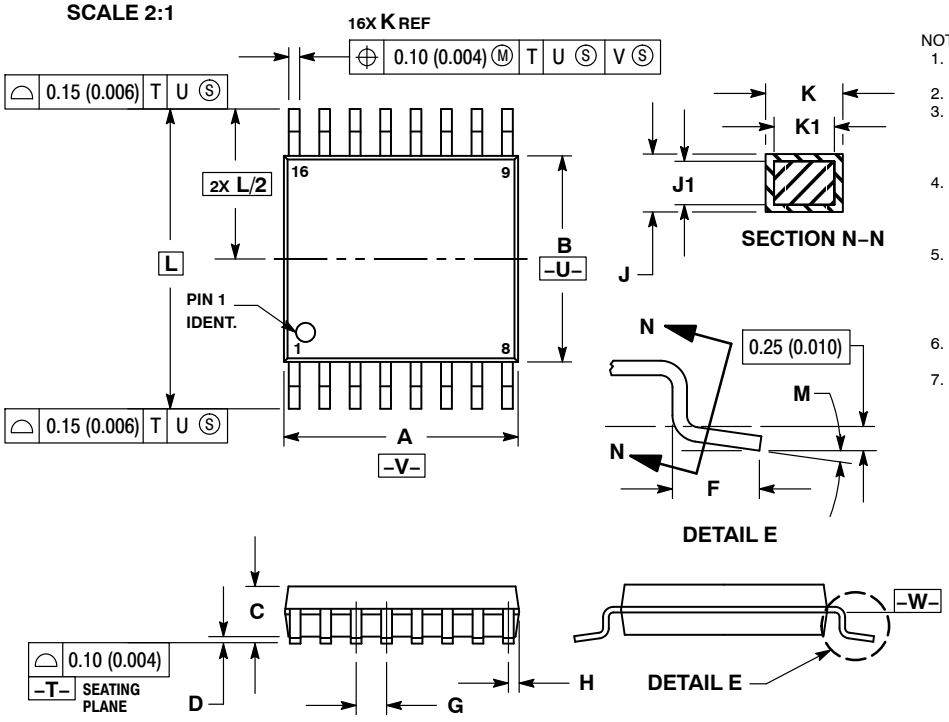
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TSSOP−16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006



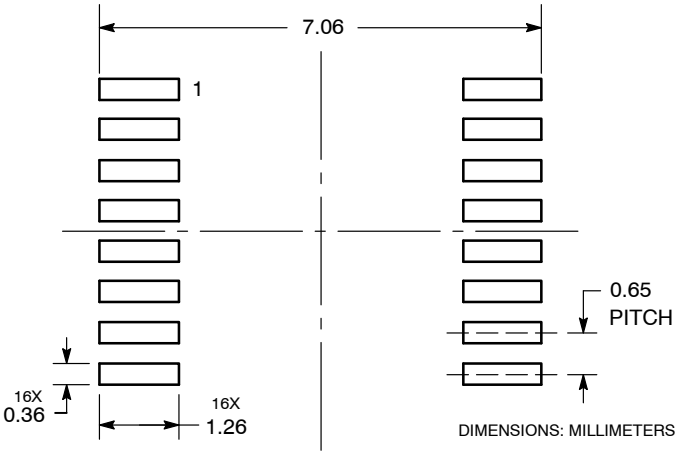
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

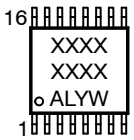
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
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L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSSOP−16**		**PAGE 1 OF 1**

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